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64-bit Efficient Adder

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Abstract

In this project, we are aimed to design an approximate 64- bit Carry Select Adder by improving full adder which is based on LUT structure. Now in our digital world that everything is based on the digital chips, based on that the electronic adders are also more important in that chips where it performs arithmetic calculations. Although there are so many techniques to minimize the delay & area that replacing of the ripple carry adder with Binary excess code converters and all. Here we proposed another way of building carry select adder with improved full adder using mux with power, area and delay minimization. We proposed Carry Select Adder which is more efficient than the conventional carry select adder.

Keywords: BEC, ripple carry adder, electronic adder, minimization of power, delay.

1. Introduction

This digital era in this world the usage of digital is also got equivalent need to human, as much as the population getting to increase the usage of digital equipment is also increasing. the speed in this is digital era is also important, to catch that speed the world needs in digital circuits.

This is the main cause which increases the value of the digital circuits. Still in these days the improvement in the digital circuits is marvelous, the day-by-day improvement in this digital circuits we tried to improve one of the most important circuit Adder. As much as the complexity increases the delay and effort in the circuits will also increases this is the catch in this field which makes most costly. So, with this in the consideration we tried to build the adder which is faster than the older circuits, also efficient and less powerconsumption.

2. Existing and proposed solutions

2.1 Existing solution

As we discussed in the introduction about the importance of the digital circuits, the main operation of the digital is circuits is arithmetic operations. These Arithmetic operations areinvolved everywhere in the digital process of the chip. As per the requirements there is a solution for the adder with this digital circuits like carry select adder, ripple adder, full adder. This worked very well in their era of digital but to match the latest speed of the digital world those have some limitations like some circuits can only be used to operate few bits of data and some of the circuits are becoming complex for the bigger circuits, this circuits need to be get improved with some techniques the drawback in the full adder is that it can only be used to limited bits of operation, coming to parallel adder it is simple in construction but the delay it causes depends on the number of bits we process .Carry –look ahead adder which is also a design which is faster than the parallel adder but the complexity is more in this design, then the design carry select adder which is the basefor our design, it has more flexibility and speed in the design but for up to some bits only. The base for the carry select adder is full adder. So, the delay in the full adder will cause the entire circuit to fail.

2.2 Proposed Solution

From the last discussion we have changed the entire full adder design with the help of mux and universal gates. If we just notice deeply about cells the is difference in the construction of each gate with transistors. The mux is designed with only two transistors, yes, it is possible that they use pass transistor logic to build that, and coming to xor gates these use more transistors to build that. So, foreach cell there is internal cell delay of its own which is completely independent on other factors. So if we design full adder with different gates means we can achieve the delay in the design

So we design the full adder with the different combinations of carry, in order to achieve the speed of the design we used multiplexers. For multiplexer there should bea selection input so we assume that the is put is carry

Now we use2:1 mux so we need to give two inputs to the mux, one will input trigger for the selection input 0, that means when thecarry is 0.

The other input triggers when the carry is 1. If you observe carefully means we will get the logic gates operations for output of full adder sum when carry is 0& 1. Like this we get the different logic for the carry too

The is a table format to understand this logic fully please take a look.

Cin	A	B	Sum		Carry	
0	0	0	0	XOR	0	AND
	0	1	1		0	
	1	0	1		0	
	1	1	0		1	
1	0	0	1	XNOR	0	OR
	0	1	0		1	
	1	0	0		1	
	1	1	1		1	

Table 2-1 truth table of Full Adder

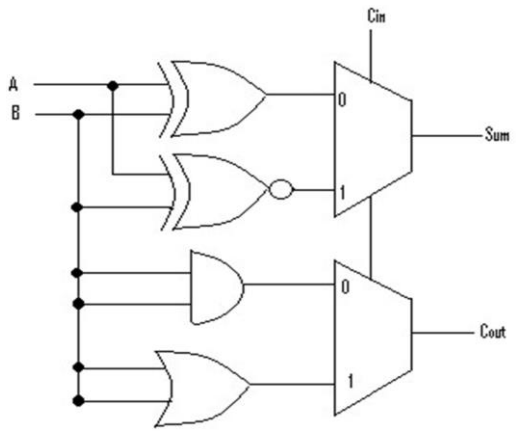

Figure 2-1 Full-Adder

Adder

As we discussed in the above section that there is a clear explanation about how the adder in the designs are important. So, thesede facto for the high bit adders, to build a 64- bit adder there are so many synthesizers will do that work. But the knowledge compared to human with computers will lose the competition so we did the structural way of building the carry select adder, you can see the block diagram of carry select adder which we designed.

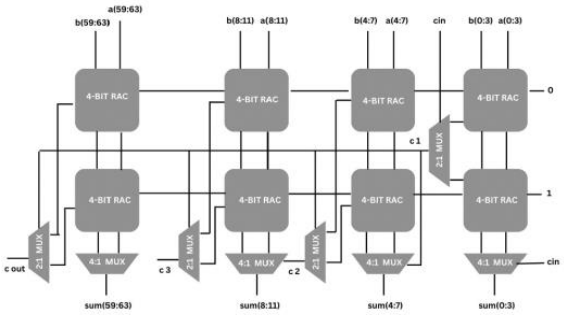

Figure 3-1 Block diagram of CSA

If we the architecture of the carry, select adder is completely different from the classic CSA. The input of the carry decides the whole output of the CSA and the full adder output are fed into the mux and the output of the mux depends up on the selection input that is carry for example if we take 4-bit adder as an example the carry will decide the output the carry and the sum as we designed this in the name of synthesizer.

Layout results

The layout results show how complex the designis and the circuit complexity.

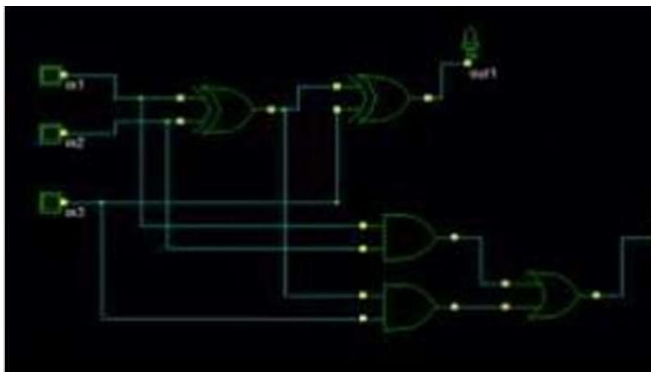

Figure 4. 1 Conventional 1bit Full Adder

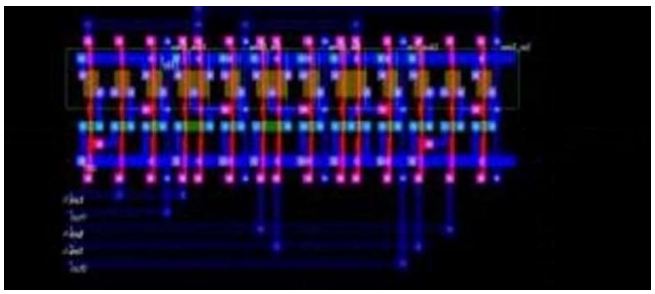

Figure 4. 2 Layout of Conventional 1bit Full Adder

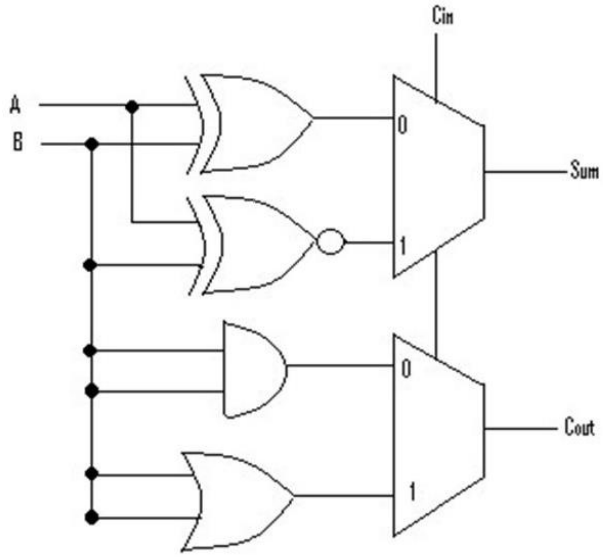

Figure 4. 3 MUX Based Full Adder

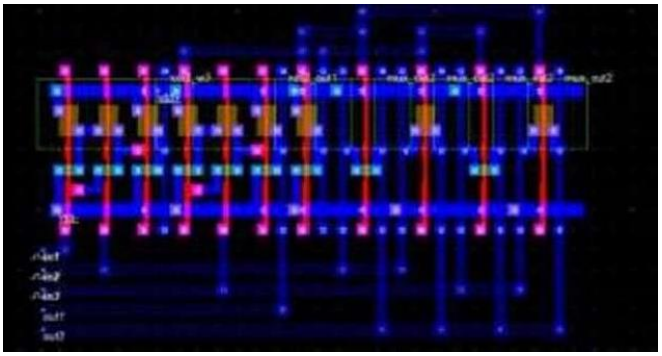

Figure 4. 4 Layout of MUX Based Full Adder

Simulation Results

The proposed technique takes the less delay if we compared to the old CSA then these are the results of the design. The simulation results of the design are shown in the below fig.

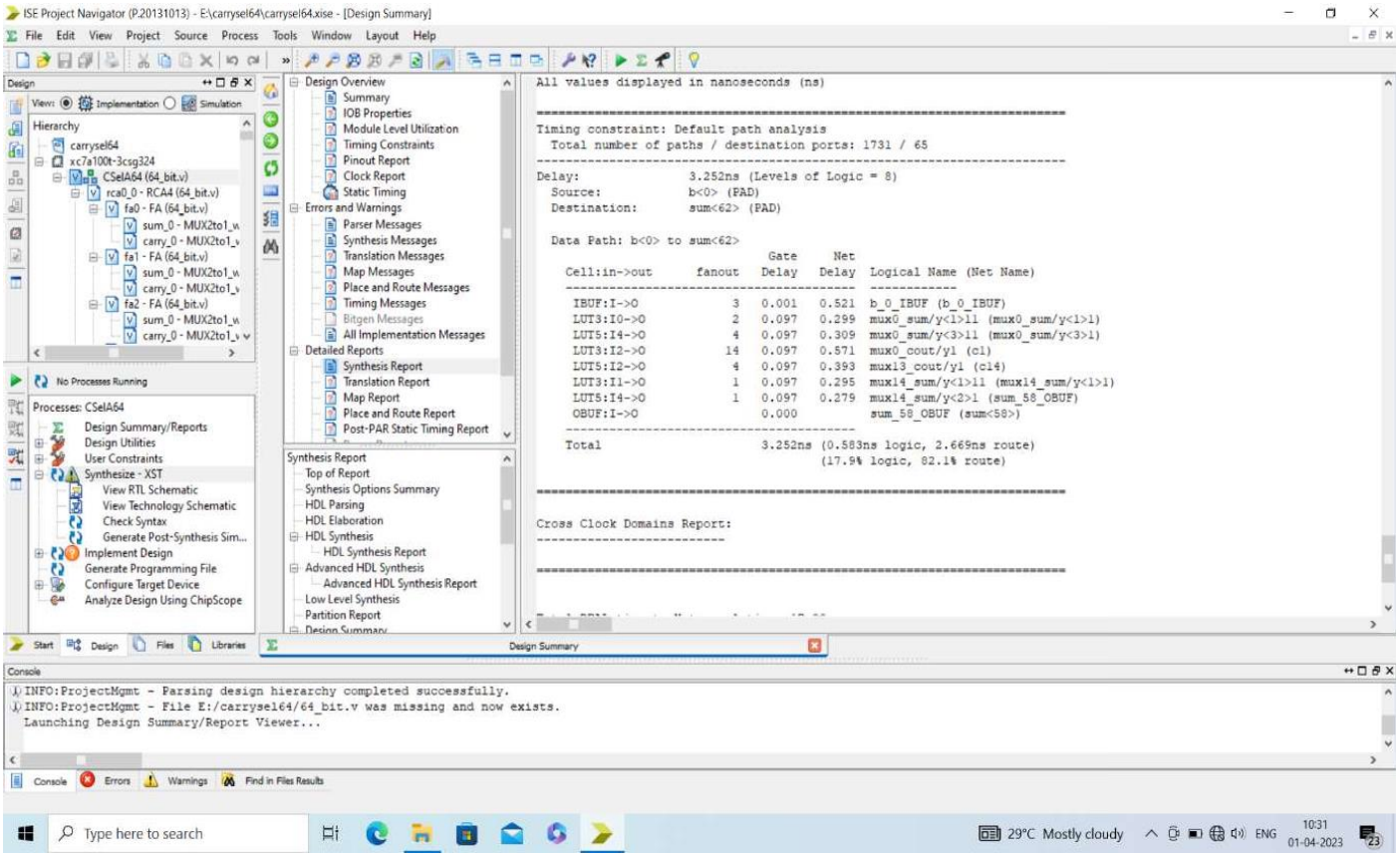

Figure 5. 1 Simulation results in Xilinx ISE

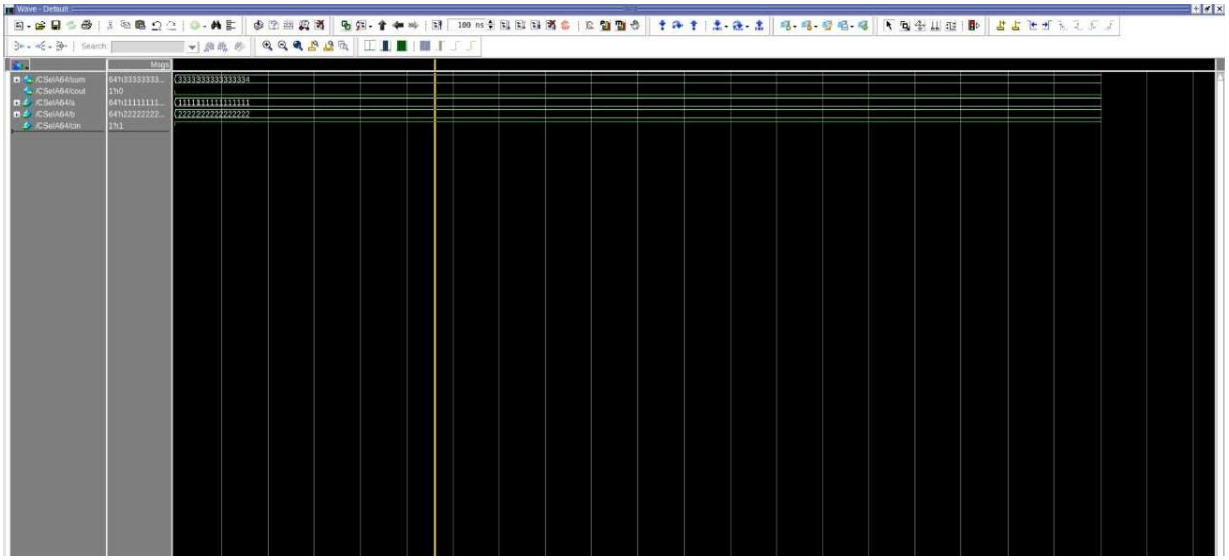

Figure 5. 2 simulation results in model Sim

Bit Size	Adder Scheme	Technology	Area(μm2)	Power(μW)	Delay(ns)
4-Bit	Conventional CSLA		669	33.56	1.36
	BK-Carry Select Adder	CMOS	293	15.35	1.26
	BE1C-Carry Select Adder	ASCI	532	27.10	1.81
	LF-Carry Select Adder		299	15.58	1.09
	KS-Carry Select Adder		466	21.12	1.12
	BE1C-Carry Select Adder	CMOS	253	12.62	0.62
	Proposed - Carry Select Adder	VLSI			
8-Bit	Conventional CSLA		978	54.29	1.76
	BK-Carry Select Adder	CMOS	815	46.79	1.88
	BE1C-Carry Select Adder	ASCI	931	53.61	2.15
	LF-Carry Select Adder		828	43.02	1.78
	KS-Carry Select Adder		1088	57.46	1.81
	BE1C-BK- Carry SelectAdder	VLSI			19.300
	BE1C-Carry Select Adder	CMOS	931	49.28	1.62
	Proposed - Carry Select Adder	VLSI			
16-Bit	Conventional CSLA		2315	131.36	3.07
	BK-Carry Select Adder	CMOS	1859	110.27	3.12
	BE1C-Carry Select Adder	ASCI	1979	116.89	3.61
	LF-Carry Select Adder		1879	104.38	2.99
	KS-Carry Select Adder		2325	130.10	3.02
	BEC-Carry Select Adder	CMOS	2056	115.11	2.83
	MCC-Carry Select Adder	CMOS		22.563	0.473965
64- Bit	Designed	VLSI	643	0.059	3.252

Table 5- 1 Comparison table of Adders

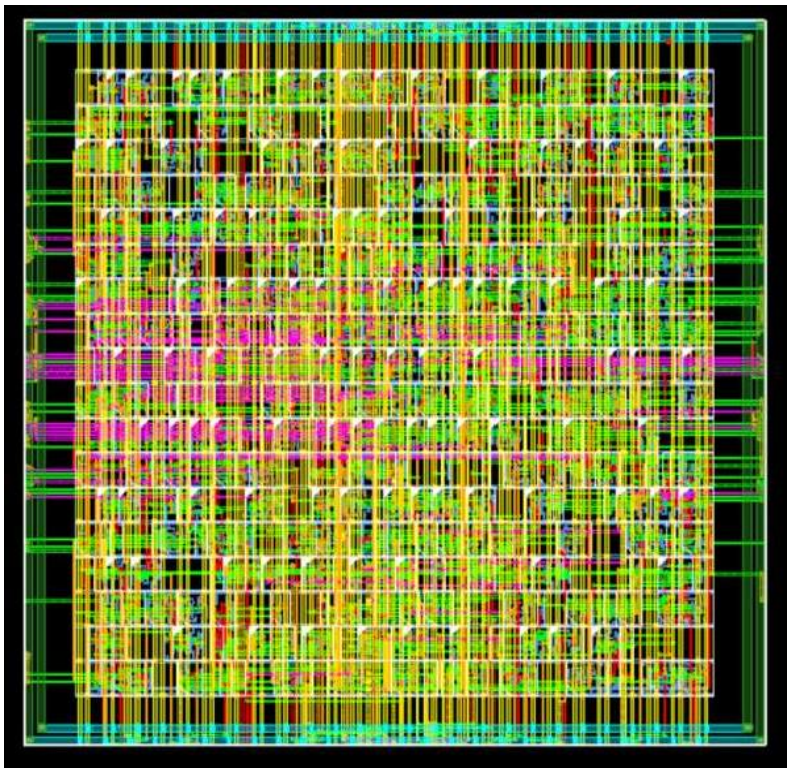

Figure 5. 3 simulation results in model Sim

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