

Design And Analysis Of 64-Bit Adders In Cadence Using Different Logic Families

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Abstract -In this project, we focus on the design and analysis of 64-Bit Adders using different logic families: CMOS, Pseudo-NMOS, and Transmission Gate. Full-Adder circuits are digital logic circuits capable of adding two input bits and a carry-in bit and generating a sum and carry-out bit as outputs. They are an essential building block for larger Adders and are widely used in digital circuits. To design the Adder circuits, we use the design tools provided by Cadence. We implement the Full-Adder circuits using the appropriate MOSFETs for each logic family and cascade several Full-Adders together to form the larger 64-Bit Adder. Once we design the adder circuits, we use simulation tools to verify their functionality and compare their power and performance characteristics. We measure the power consumption of the adder circuits under different operating conditions and analyze the speed of the adder circuits to determine which logic family offers the best trade-off regarding power efficiency and performance. Based on the results obtained from different logic families, we can identify the logic family that provides the best combination of speed and power consumption.

Key Words: Full Adder, Ripple Carry Adder, CMOS, Pseudo-NMOS, Transmission Gate, Power Analysis

1. INTRODUCTION

We are seeing rapid growth in the field of integrated circuit (IC) technology. All ICs must be designed in an optimized manner to meet all requirements of speed, space-saving, and low power consumption. One of the circuits that most ICs occupy is the ALU, which is a combination of arithmetic and logic units. The two most important arithmetic units are adders and multipliers.

Adders are the heart of arithmetic circuits, and many complex arithmetic circuits are based on addition. Due to the widespread use of this operation in arithmetic functions, adders in mobile applications are of interest. Several variations of different logic styles have been proposed in recent years to implement 1-Bit adder cells. These summing cells are typically intended to reduce power consumption and increase speed. These studies also explore different approaches to implementing adders using CMOS technology.

In mobile applications, designers must work within very tight leakage performance specifications to meet battery life and package cost goals for their products. A designer's concern about the level of leakage current has nothing to do with ensuring correct circuit operation but with minimising power consumption.

In this project, all the designs are based on the structure of the Ripple Carry Adder. Since it is a 64-Bit Full-Adder, we cascaded 1-Bit, 4-Bit, 8-Bit, 16-Bit, and 32-Bit together to form a 64-Bit using Ripple carry Adder for each logic family. These Full-Adders of all logic families and their respective symbols are designed in GPDK090 and analyzed using the Cadence Virtuoso platform.

1.1 Full Adder

A Full-Adder is a digital circuit. A 1-Bit Full-Adder adds three 1-Bit inputs named X, Y, and Cin. X and Y are the operands, and Cin has some carryover from the previous less critical stage. A Full-Adder is typically one component of a cascaded adder that adds binary numbers of 4, 8, 16, 32, etc. bits. This circuit produces a 2-Bit output Carry (Cout) and Sum (S).

Equations: These equations are obtained from the truth table of 1-Bit Full-Adder using K-maps for S and Cout. Fig - 1 shows the circuit diagram designed from these equations:

$$\text{Sum}(S) = (X \text{ XOR } Y) \text{ XOR } \text{Cin}$$

$$\text{Carry}(\text{Cout}) = X \cdot Y + Y \cdot \text{Cin} + X \cdot \text{Cin}$$

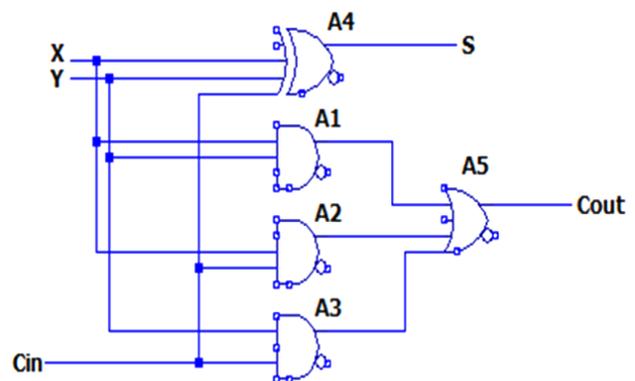


Fig -1: Circuit Diagram of Full-Adder

1.2 Logic Families

A logic family of monolithic digital integrated circuits is a group of electronic logic gates built using several designs, often compatible with logic levels and performance characteristics.

A logic family can also be a set of techniques to implement logic in VLSI integrated circuits, such as a central processing unit, memory, or other complex functions. Some of these logic families use static techniques to reduce design complexity. Other logic families of this type, such as domino logic, use clocked dynamic methods to minimise size, power consumption, and latency.

The logic families used in this project are:

1. Pseudo-NMOS
2. Complementary Metal Oxide Semiconductor (CMOS)
3. Transmission Gate

1) Pseudo-NMOS: This streamlined structure replaces the pull-up circuit with a single pull-up PMOS whose gate is permanently grounded. Pseudo-NMOS works similarly to NMOS logic. When an NMOS transistor receives a significant voltage, it is called a closed circuit. In contrast, when an NMOS transistor gets a voltage of about 0 volts, the source-to-drain connection breaks, called an open circuit.

2) Complementary Metal Oxide Semiconductor (CMOS): CMOS combines NMOS and PMOS. Hence required number of transistors for designing a circuit is $2n$. The Complementary Metal Oxide Semiconductor (CMOS) logic family is a digital logic circuit widely used in modern electronic devices. PMOS transistors are designed to have low resistance between source and drain contacts when the low gate voltage is applied and high resistance when a high gate voltage is applied; It's the opposite. The CMOS circuit is built with an additional configuration, which features low power consumption, strong anti-interference ability, and high-speed operation.

3) Transmission Gate: The Transmission Gate has NMOS and PMOS parallel to each other. The work is based on NMOS and PMOS. As the input is high, NMOS gets ON, and when intake is low, PMOS gets on. As a result, the signal will pass through the circuit and be obtained at the output.

1.2 Power Analysis

Power analysis is a crucial step in VLSI (Very Large Scale Integration) circuit design used in modern electronic devices such as smartphones, computers, and

microcontrollers. Power analysis involves measuring and analysing the power consumption as it affects circuit performance, as high power consumption can slow things down.

Types Of Power Analysis:

Total-Power: It is the sum of the power consumed by all of its components, known as Total-Power. It is measured in watts (W).

Average Power: It is the ratio of total power consumed over a given period to the duration of that period. Its units are watts (W).

Power Delay Product (PDP): Product of current consumption and delay. It can reflect both dynamic power consumption and propagation delay of the system. It is typically measured in joules (J).

Peak-Power: The highest power value is observed at a given time and is measured in Watts (W) or MilliWatts (mw).

2. IMPLEMENTATIONS

2.1 CMOS 1-Bit Schematic

The schematic shown in Fig -2 is designed using Full-Adder equations with CMOS logic, and a CMOS 1-Bit circuit is created as a symbol named CMOS_1BIT. Fig -3 shows the symbol of 1-Bit CMOS.

- In Fig -2, a, b, and c are inputs and carry, sum are outputs.
- In Fig -3, V-pulse is connected to the inputs a,b, and cin individually and given voltage1 as 0v and voltage2 as 1.8v.
- V-pulse for a, b and cin is provided with periods 20us, 40us, and 80us with pulse width 10us, 20us, and 40us, respectively.
- Vdd is connected to the ground.
- Using 'DC Transient Analysis', we have simulated the circuit.

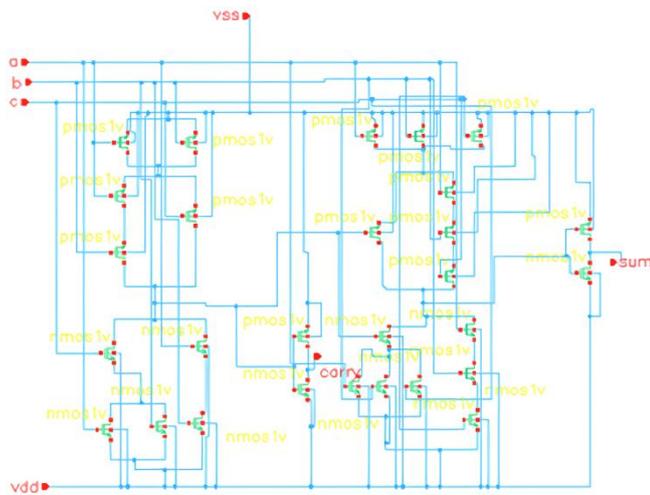


Fig -2: CMOS 1-Bit Schematic

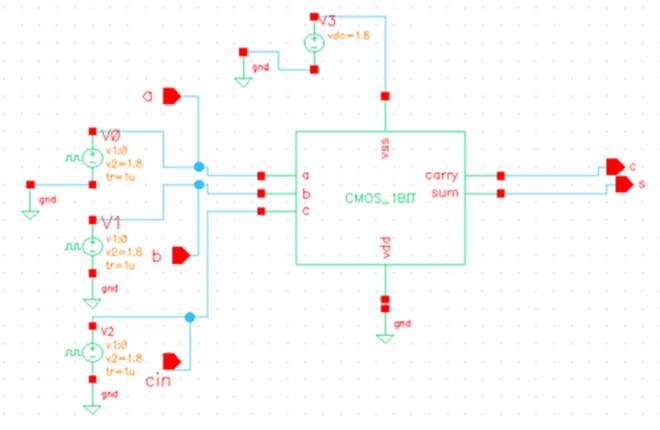


Fig -3: CMOS 1-Bit Symbol

The graph in Fig -4 shows the transient analysis of CMOS 1-bit with a stop time of 100us.

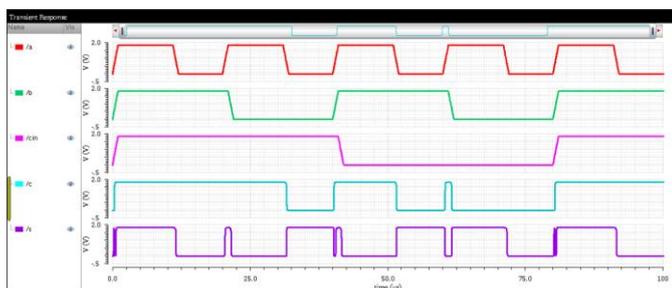


Fig -4: CMOS 1-Bit Graph

To design a CMOS 4-bit adder, four CMOS 1-bit adders are cascaded. Then, two CMOS 4-bit adders are cascaded to design a CMOS 8-bit adder. It is shown in Fig -5.

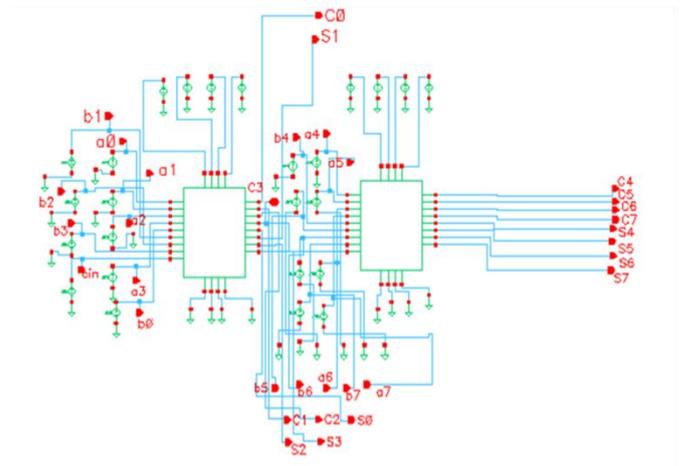


Fig -5: CMOS 8-Bit

Similarly, two CMOS 8-bit adders are cascaded to design a CMOS 16-bit adder then two CMOS 16-bit adders are cascaded to design a CMOS 32-bit adder. It is shown in Fig-6.

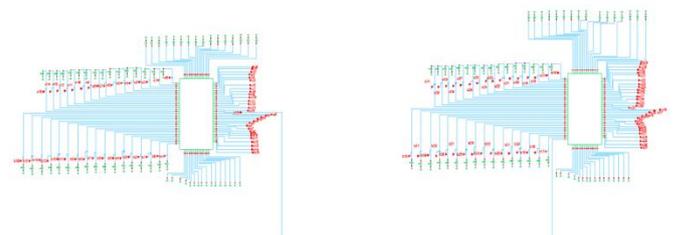


Fig -6: CMOS 32-Bit

Similarly, two CMOS 32-bit adders are cascaded to design a CMOS 64-bit adder. It is shown in Fig -7.

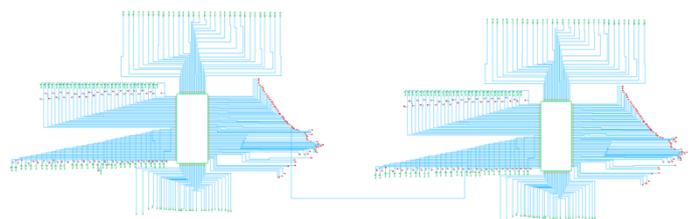


Fig -7: CMOS 64-Bit

2.2 Pseudo-NMOS 1-Bit Schematic

The schematic shown in Fig -8 is designed using Full-Adder equations with Pseudo-NMOS Logic, and Pseudo-NMOS 1-bit Circuit is created as a symbol named Pseudo-NMOS_1BIT. Fig -9 shows the symbol of 1-bit Pseudo-NMOS.

- In Fig -8, a, b, and c are inputs and carry, sum are outputs.

- In Fig -9, V-pulse is connected to the inputs a, b, and cin individually and given voltage1 as 0v and voltage2 as 1.8v
- V-pulse for a, b and cin is provided with period 20us, 40us, 80us with pulse width 10us, 20us, 40us respectively.
- Vdd is connected to the ground.
- Using 'DC Transient Analysis', we have simulated the circuit.

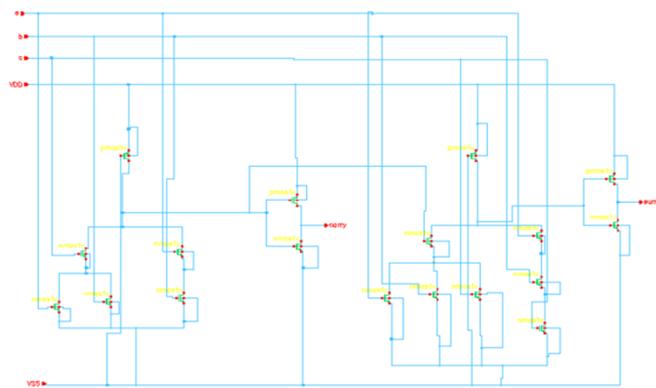


Fig -8: Pseudo-NMOS 1-Bit Schematic

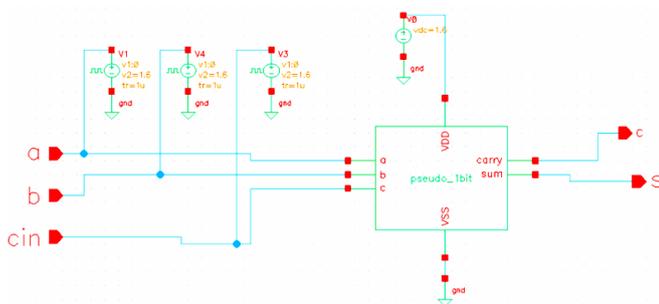


Fig -9: Pseudo-NMOS 1-Bit Symbol

The graph in Fig -10 shows the transient analysis of Pseudo-NMOS 1-Bit with a stop time of 100us.

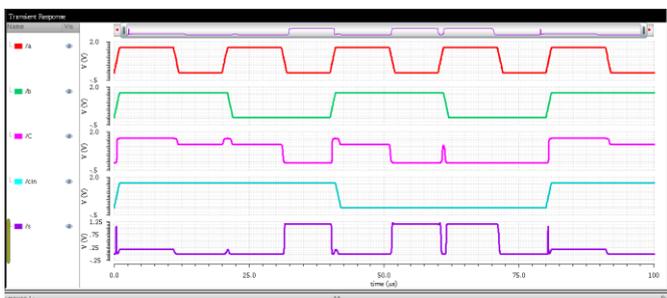


Fig -10: Pseudo-NMOS 1-Bit Graph

Similar to the CMOS designing process, we have designed a 64-Bit Pseudo-NMOS. It is shown in Fig -11.

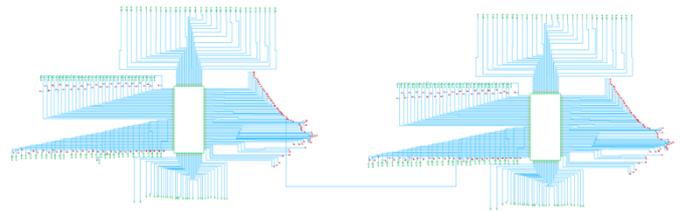


Fig -11: Pseudo-NMOS 64-Bit

2.3 Transmission Gate 1-Bit Schematic

The Schematic shown in Fig -12 is designed using Full-Adder equations with Transmission Gate Logic, and Transmission Gate 1-Bit Circuit is created as a symbol named Transmission Gate 1-BIT. Fig -13 shows the symbol of the 1-Bit Transmission Gate.

- In Fig -12, A, B, and C are inputs and carry, sum are outputs.
- In Fig -13, V-pulse is connected to the inputs a,b, and cin individually and given voltage1 as 0v and voltage2 as 1.8v
- V-pulse for a, b and cin is provided with period 20us, 40us, 80us with pulse width 10us, 20us, 40us respectively.
- Vdd is connected to the ground.
- Using 'DC Transient Analysis', we simulated the circuit.

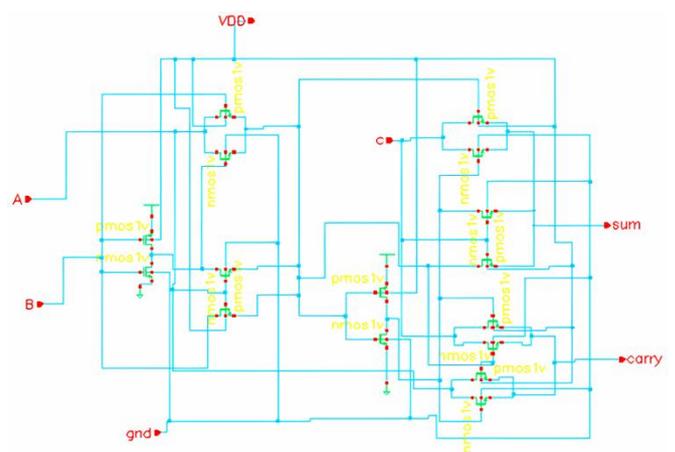


Fig -12: Transmission Gate 1-Bit Schematic

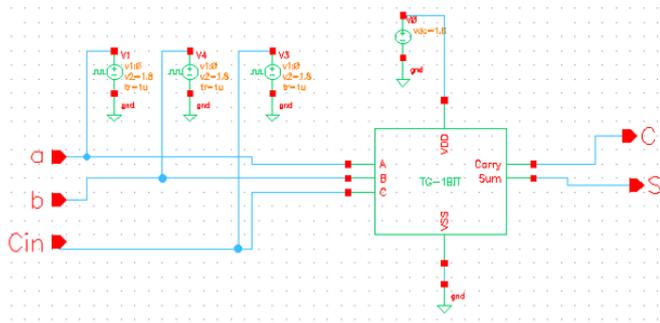


Fig -13: Transmission Gate 1-Bit Symbol



Fig -16: Peak-Power value and Total-Power value of CMOS 64-Bit graph

The graph in Fig -14 shows the transient analysis of Transmission Gate 1-Bit with a stop time of 100us

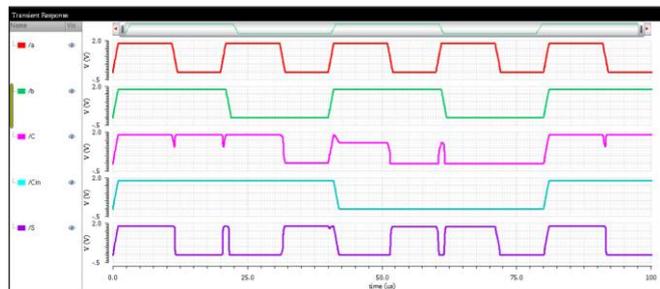


Fig -14: Transmission Gate 1-Bit Graph

Similar to the CMOS and Pseudo-NMOS designing process, we have designed a 64-Bit Transmission Gate. It is shown in Fig -15.

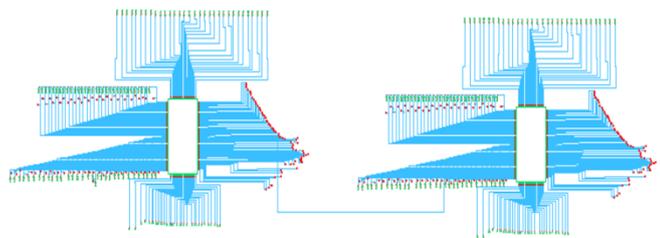


Fig -15: Transmission Gate 64-Bit

3. POWER ANALYSIS OF LOGIC FAMILIES

3.1 Power Analysis Of CMOS 64-Bit

From the graphs in Fig -16, we can observe the Total-Power and Peak-Power values

- The Peak-Power value is: 23.28mw
- The Total-Power value is: 23.77mw

3.2 Power Analysis of Pseudo-NMOS 64-Bit

From the graphs in Fig -17, we can observe the Total-Power and Peak-Power values

- The Peak-Power value: 23.49mw
- The Total-Power value: 23.77mw

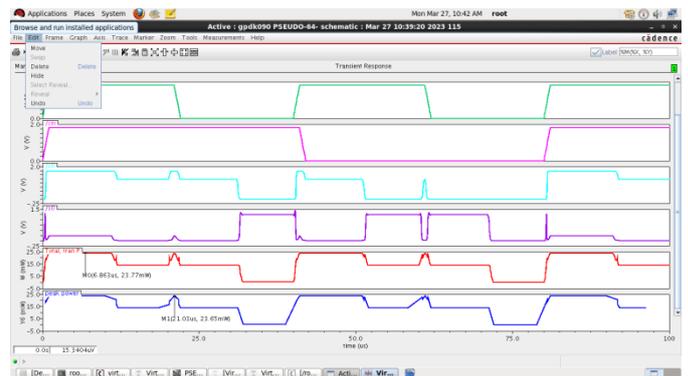


Fig -17: Peak-Power value and Total-Power value Pseudo-NMOS 64-Bit graph

3.3 Power Analysis of Transmission Gate 64-Bit

From the graphs in Fig -18, we can observe the Total-Power and Peak-Power values.

- The Peak-Power value: 4.17mw
- The Total-Power value: 46.34mw

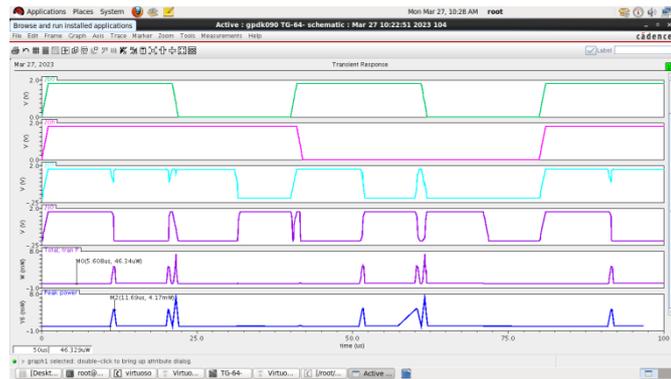


Fig -18: Peak-Power value and Total-Power value of Transmission Gate 64-Bit graph

3.2 Observations

Table -1: Power Analysis Table

Logic Family	CMOS	Transmission Gate	Pseudo-NMOS
No. of Transistor (64-Bit)	1792	1024	1152
Average Power (W)	14.94E-3	219.0E-6	14.94E-3
Total-Power (W)	23.77mW	46.34uW	23.77mW
Peak-Power (W)	23.28mW	4.17mW	23.49mW
Delay (s)	107.608n	275.903p	107.608n
Power Delay Product (PDP) (J)	1.607E-09	6.0422E-14	1.607E-09

Based on our design, the Table -1 shows that the CMOS logic family has the highest transistor count among the three options, while the Transmission Gate logic family has the lowest. However, the Transmission Gate logic family exhibits the highest peak power consumption, while the Pseudo-NMOS and CMOS families have identical power consumption characteristics. In terms of delay, all three logic families have the same value of 107.608 ns. The power-delay product (PDP) is the lowest for the Transmission Gate logic family, indicating better efficiency in terms of power consumption and performance.

However, it may vary to different applications. We can choose the desired logic family based on cost, power, and performance.

4. CONCLUSIONS

Firstly, Transmission Gate Full-Adder circuits use fewer transistors than CMOS and pseudo-NMOS Full-Adder circuits. Secondly, Transmission Gate Full-Adder circuits also have lower delays than other logic families. Thirdly, Transmission Gate Full-Adders exhibit better power delay product results than CMOS and Pseudo-NMOS Full-Adder circuits; however, the choice of the logic family to be used ultimately depends on the application's specific requirements, such as cost, power and performance. Hence, from our designs, these conclusions highlight the advantages of using Transmission Gate Full-Adder circuits in specific applications where power consumption and delay are critical factors.

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