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Design and Performance Analysis of CMOS Voltage Controlled Oscillator (VCO) in Static CMOS 45 nm Technology

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Abstract:

This paper presents a relative study among different topologies of Ring Oscillator based Voltage Controlled Oscillator (VCO) on the basis of different parameters like centre frequency, tuning range, frequency stability, power dissipation and linearity etc. All the design has been done in 45 nm Static CMOS technology and are subsequently compared on various parameters. An inherent idea of the given performance parameters has been realized by the comparative study. The comparative data shows that VCO with both NMOS & PMOS control devices along with complementary V_{ctr} has the best trade-off between power dissipation and tuning range. In this study the topology of VCO with complementary control voltages exhibits tuning range of 0-20 GHz and power dissipation less than 1.5mW thus eliciting Ring oscillator based VCO is best in terms of power consumption. Simulations are carried out using the LTSpice simulator in a 45 nm standard* process.

Keywords: Voltage Controlled Oscillator (VCO), Static CMOS, Tuning range, Power consumption.

1 Introduction

In today's IC industry a good understanding of semiconductor process and devices is essential, as process to device to circuit domains are tightly coupled, for quality of analog / digital designs. In digital designs MOS transistors are considered as simple switches but in analog designs detailed understanding of the device is required because of its multiple roles as amplifying device, capacitor, switch etc. and this implication of the second order effects on the performance of circuit. Further, with the advent of device scaling into nano-meter regime, implications of non-ideal effects become significant and the circuit designer has to decide on the selection of second order effects to be considered for design. At nanoscale integration, the CMOS technology has become a technology of choice for analog circuit design in a mixed signal environment.

Since all the basic devices in an IC respond to continuous time stimulus, analog design forms the foundation for all IC designs. Modern IC technology presents many design challenges. There is significant variability in the manufacturing process for advanced technology nodes. The actual operation of the large number of devices on advanced ICs also causes variability. This variability manifests as changes in the device threshold voltage, supply voltage, operating temperature, which in turn translate into performance variability. Densely packed devices result in parasitic capacitances leading to undesirable signal interference and distortion.

In the domain of VLSI design the selection of a linear and wide range voltage-controlled oscillator for various RF, Biomedical, Clock recovery circuits and other applications is always a challenging work for Electronics Engineers. An oscillator is an electrical autonomous system which generates a periodic oscillating frequency signal depending on its input voltage. VCO is the main component in many RF circuits and is the heart of Phase Lock Loop system, Clock recovery circuit and Frequency Integrated circuits, so it is very vital to select the suitable VCO design. Frequency, amplitude and noise level should be controlled for many of the applications.

Oscillators can be divided into two categories; Firstly, the LC oscillator which is composed of the active devices, coupled with LC resonant circuit. Secondly, the loop ring oscillator which is composed of delayed cascade units with positive feedback. The important requirements of VCO are High gain, wide tuning range, low power consumption and high signal to noise ratio.

The design of a Voltage Controlled Oscillator involves many trade-offs between area, speed, power, and application domains. These problems and a comparative study of different ring oscillator designs is midst interest in this paper. The performance of different circuits has been comparatively analysed through simulation results in 45nm CMOS Technology using LTSpice

2 Simulation Methodology

2.1 Ring Oscillator Design:

The design of the ring oscillator can be done using three inverters. The three-stage ring oscillator with 3 inverter stages connected in series to form a positive feedback system to provide sufficient gain to support sustained oscillations. The frequency of oscillations is given in Eq. (1.1).

$$f = 1/2n\tau \quad \text{..... (1.1)}$$

where τ = time delay for single inverter,

n = number of inverters in the oscillator.

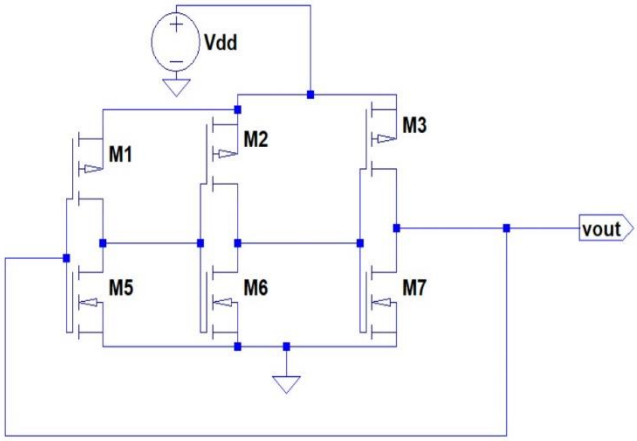


Fig 2.1: Schematic Circuit Diagram of 3 Stage Ring Oscillator.

According to Barkhausen criteria, the necessary but not sufficient condition for positive feedback circuit to oscillate is:

1. The magnitude of loop gain, $|H(j\omega_0)| \geq 1$

2. The phase shift around the loop, $\angle H(j\omega_0) = 2n\pi$

where $\omega 0$ is the frequency at which the circuit may oscillate in rad/s.

Table 2.1 Mentions the effects of device sizing on performance metrics of 3-stage ring oscillator.

W_N (μm)	W_P (μm)	Frequency (GHz)	Settling time (μs)	Output Swing (mV)	Average Power (mW)
1	2	37.487	217.54	943.4 – 84.34	0.973
5	10	34.968	240.84	958.35 – 61.42	4.825
10	20	30.566	207.15	930.16 – 70.57	9.824
25	50	16.865	148.25	927.32 – 127.8	23.54

2.2 VCO with NMOS control Devices

In the VCO topology with NMOS control devices, shown in Fig., an NMOS control device (M7, M8, and M9) are stacked below the NMOS (M4, M5, M6) of basic inverter stage of the RO and the input control voltage is applied to these control devices. The NMOS control devices transition between cutoff, saturation and triode region as DC control voltage is linearly varied from 0 V to V_{DD}

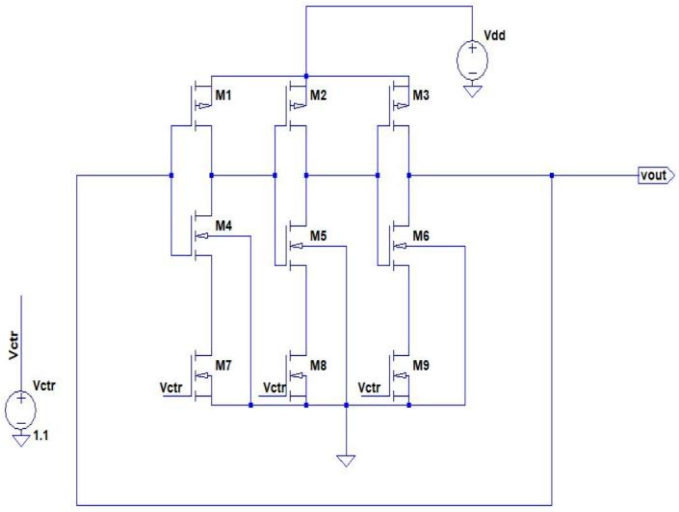


Fig 2.2: Three-stage VCO with NMOS control devices.

1. For $V_{ctr} < V_{Tn}$, control devices are biased in the cut off region. Thus, there is no drain current and hence no oscillations.

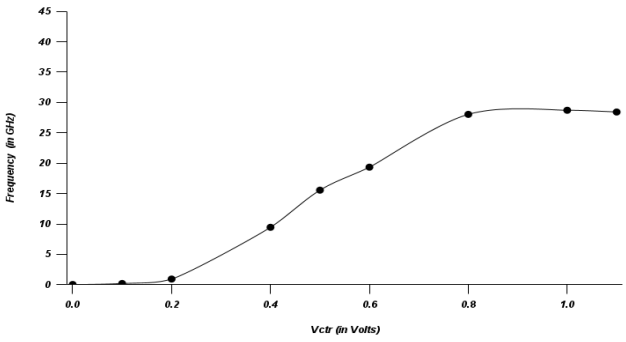
2. For $V_{ctr} > V_{Tn}$, M7, M8 and M9 turn on in the saturation region. Drain current in saturation region for NMOS devices has a square- law dependence on V_{ctr}, as given in Eq. (2.1).

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{ctr} - V_{Tn})^2 \quad \text{..... (2.1)}$$

3. As V_{ctr} is increased further, i.e., as $V_{ctr} - V_{Tn} > V_{DS}$ of control devices, NMOS control devices enter the triode region. Here, the drain current is a linear function of V_{ctr} and is given by Eq. (2.2).

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(2(V_{ctr} - V_{Tn})V_{DS} - {V_{DS}}^2) \text{..... (2.2)}$$

(V_{Tn} = 0.466 V)



Graph 2.2: Transfer characteristics of the NMOS controlled VCO circuit

The VCO exhibits a dead zone, with no oscillations, up to $V_{ctr} < V_{Tn}$ as M7, M8, and M9 are biased in cutoff. As V_{ctr} increases beyond V_{Tn}, the frequency increases with a

steep slope due to the square-law dependence of current on V_{ctr}

Table 2.2 Mentions the effects of device sizing on performance metrics of VCO with NMOS control devices (at $V_{ctr} = 0.2V$).

W_N (μm)	W_P (μm)	Frequency (GHz)	Settling time (ms)	Output Swing (V)	Average Power (μW)
1	2	1.1145	1.149	1.049 – 0.697	13.453
5	10	1.0985	1.118	1.078 – 0.696	57.812
10	20	1.1222	1.038	1.08 – 0.663	112.79
25	50	0.8683	0.746	1.088 – 0.652	268.51

2.3 VCO with PMOS control devices

In this topology, PMOS control devices (M1, M2, M3) are stacked above the PMOS devices (M4, M5, M6) of the basic inverter stage RO. The input control voltage is used as gate control for PMOS control devices. The devices switch from cutoff to saturation and eventually to triode region as control input is decreased from V_{DD} to 0 V.

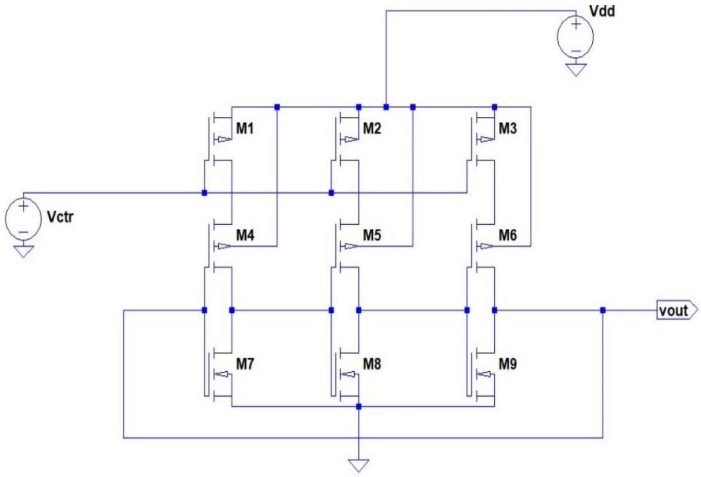


Fig 2.3: Three-stage VCO with PMOS control devices.

the operation of the control devices in different operating regions are mentioned below:

1. For $0 < V_{ctr} < V_{DD} - V_{SD} - |V_{Tp}|$, the PMOS control devices are in the triode region. Here the drain current is a linear function of V_{ctr}.

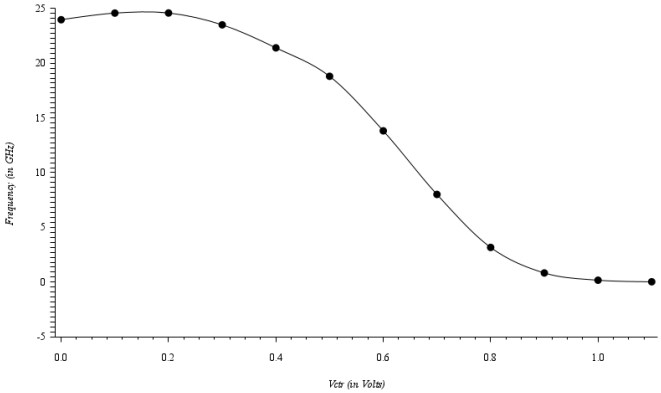
$$I_{Dp} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(2(V_{DD} - V_{ctr} - |V_{Tp}|) \quad \ldots\ldots\ldots\ldots (2.3)$$

($V_{Tp} = 0.4118\,V$)

2. For $V_{DD} - V_{SD} - |V_{Tp}| < V_{ctr} < V_{DD} - |V_{Tp}|$, M1, M2 and M3 are biased in the saturation region. Drain current in saturation region for PMOS devices has a square-law dependence on V_{ctr}.

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{ctr} - |V_{Tp}|)^2 \quad \ldots\ldots\ldots\ldots (2.4)$$

3. The control devices enter cut off region for $V_{ctr} > V_{DD} - |V_{Tp}|$. Thus, the drain current is zero and hence no oscillations are expected.



Graph 2.3: Transfer characteristics of the PMOS controlled VCO circuit.

Similar to the previous circuit, the characteristics have a low slope when the device is in the triode region and a greater slope when in the saturation region. The VCO exhibits a dead zone for $V_{ctr} > V_{DD} - |V_{Tp}|$. Thus, there is significant nonlinearity throughout the tuning range. The circuit has to be sized carefully to avoid asymmetry in rise and fall times.

Table 2.3 Mentions the effects of device sizing on performance metrics of VCO with PMOS control devices (at $V_{ctr} = 0.6V$).

W_N (μm)	W_P (μm)	Frequency (GHz)	Settling time (μs)	Output Swing (mV)	Average Power (mW)
1	2	13.25	105.1	602.1 – 98.4	0.267
5	10	13.21	103.5	662.9 – 36.6	1.266
10	20	13.13	96.8	657.5 – 30.3	2.54
25	50	9.87	59.3	748.9 – 23.5	6.45

2.4 VCO with both NMOS and PMOS control devices using same V_{ctr}

In this circuit, both NMOS (M10, M11, M12) and PMOS (M1, M7, M3) control devices are stacked in series with each ring oscillator stage as shown in the circuit diagram. All NMOS / PMOS control devices are given the same control voltage.

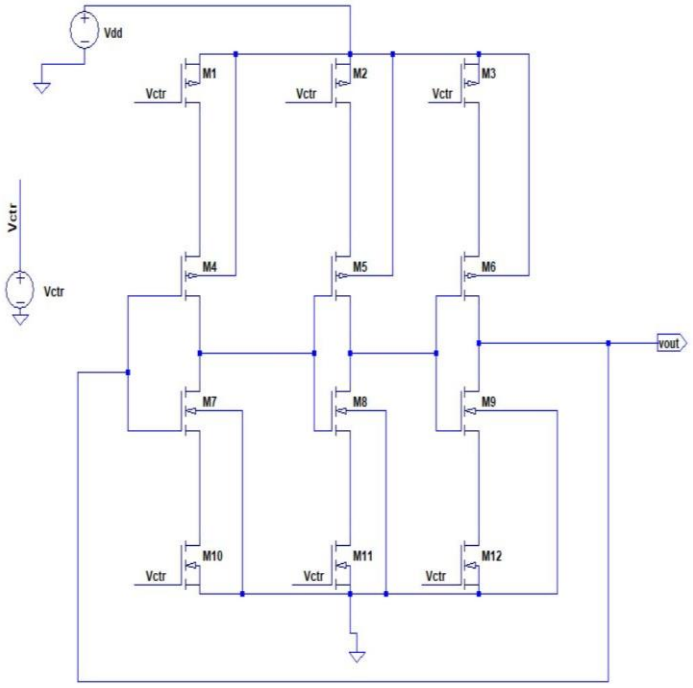


Fig 2.4: VCO with same control voltage to both PMOS and NMOS devices.

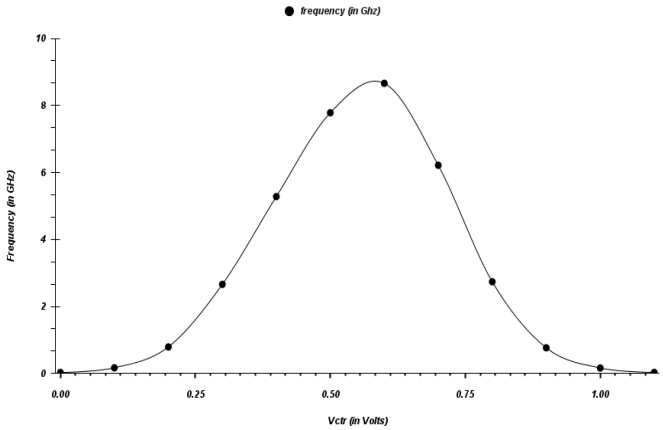
1. For 0 < V_{ctr} < V_{Tn} the NMOS devices turned off whereas the PMOS control devices are in linear region. Hence there is no drain current through the devices and no oscillations are obtained.

2. For V_{Tn} <V_{ctr} <V_{DD} -V_{SDp} - |V_{Tp}|, NMOS devices turn on in saturation while PMOS devices remain in triode region. The drain current start increasing with V_{ctr}.

3. For V_{DD} -V_{SDp} - |V_{Tp}|<V_{ctr}< V_{DSn} + V_{Tn}, both devices are in saturation region. The drain currents are highest in this region.

4. For V_{DSn} + V_{Tn} < V_{ctr} < V_{DD} - |V_{Tp}|, PMOS devices remain in the saturation region while NMOS devices enter the triode region. The drain current begins to decrease with increasing V_{ctr}.

5. For V_{DD} - |V_{Tp}| <V_{ctr}<V_{DD} the PMOS control devices are turned off whereas the NMOS devices are in the linear region. Hence there is no drain current through the devices and no oscillations are exhibited.



Graph 2.4: The variation of frequency as a function of control voltage. It is a bell-shaped characteristic.

Table 2.4 Mentions the effects of device sizing on performance metrics of VCO with NMOS & PMOS control devices (at V_{ctr} =0.6V).

W_N (μm)	W_P (μm)	Frequency (GHz)	Settling time (μs)	Output Swing (V)	Average Power (mW)
1	2	10.35	56.81	775.1 – 98.15	0.217
5	10	9.96	45.37	805.65 – 40.98	1.079
10	20	8.62	47.18	835.46 – 33.01	2.263
25	50	7.28	39.95	867.77 – 31.47	5.562

2.5 VCO with both NMOS & PMOS control devices & complimentary V_{ctr}

The drawbacks of the previous circuits can be overcome by simply using two complimentary control voltages instead of one. The control inputs are such that while NMOS control devices (M10, M11, M12) are applied by V_{ctr2}, PMOS control devices (M1, M2, M3) are given a gate voltage complementary to that given to NMOS (V_{ctr1}= V_{DD} - V_{ctr2}).

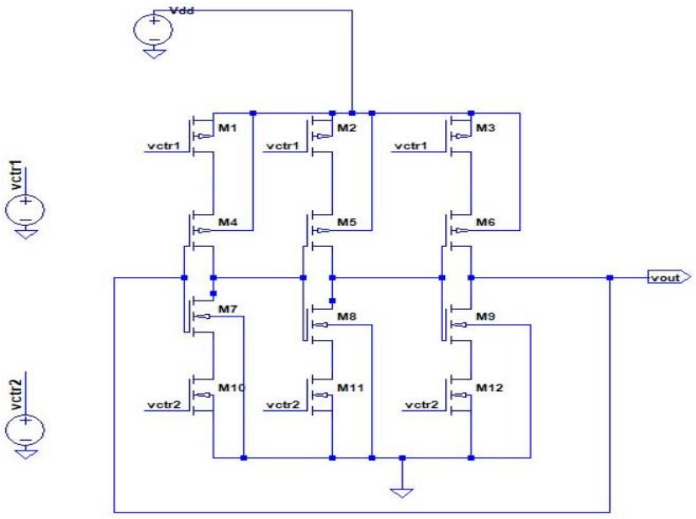
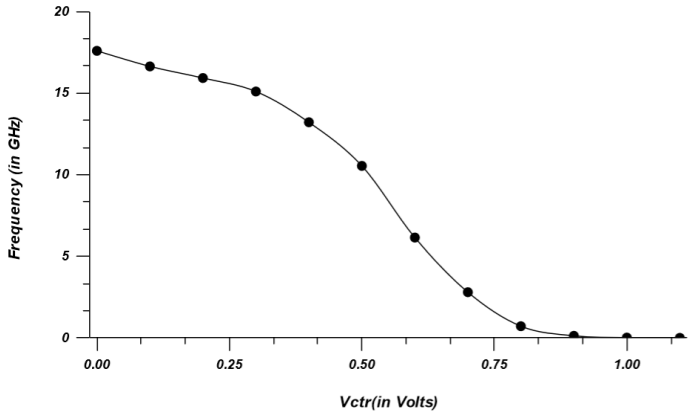


Fig 2.5: VCO with Complementary control Voltage to both PMOS and NMOS devices

1. PMOS control devices are cut off for V_{ctr2} < | V_{Tp}|. Hence oscillations will not occur.

2. When V_{ctr2} increases further, for V_{ctr2} > | V_{Tp}|, both NMOS and PMOS control devices turn on in the saturation region.

3. The devices eventually enter triode region when V_{ctr2} > V_{DS} + V_{Tn}.



Graph 2.5: Variation of Frequency with voltage for complementary control Voltage given to both PMOS & NMOS.

The circuit can oscillate at a frequency much higher than that using a single control voltage. It is a monotonically increasing curve with a wider tuning range. The input voltage range allowable for this circuit can be twice as much as that for the previous circuit.

Table 2.5 Mentions the effects of device sizing on performance metrics of VCO with complementary V_{ctr} in NMOS & PMOS control devices (At V_{ctr1} = 0.2V & V_{ctr2} = 0.9V).

W_N (μm)	W_P (μm)	Frequency (GHz)	Settling time (μs)	Output Swing (mV)	Average Power (mW)
1	2	15.89	103.27	980.75 – 66.53	0.431
5	10	15.86	85.37	978.51 – 43.57	2.168
10	20	15.34	74.75	976.29 – 37.68	4.341
25	50	9.612	55.51	987.42 – 34.79	9.838

Results and Discussions

An Overview of circuits

The frequency of oscillations increases for decreasing device widths. This is because the effect of decreasing load capacitance is more dominant compared to that of decreasing drain currents. From Table 2.1, it can also be observed that, with decreasing device sizes, dynamic power dissipation of the circuit decreases because of the smaller currents through the circuit domination over increasing frequency. Thus, this is the rare case in CMOS design where speed does not trade with power equations given below show the dependence of speed and power dissipation on load capacitances.

VCO with NMOS control devices.

This topology has a high center frequency of 13.88 GHz and a tuning range of 0 – 30 GHz. It can be further optimized to obtain higher center frequencies and tuning ranges. The tuning characteristic is non-linear due to the switching of the control device between operating regions. The dynamic power dissipated in the circuit at the center frequency (f_c) is 3.938 mW. Note that the dynamic power dissipation is less than 12.25 mW for all frequencies in the characteristics given in Table 2.2

VCO with PMOS control devices.

When PMOS control devices are used, a tuning range of 0 – 25GHz with a center frequency of 12.517 GHz is obtained. The reduction in f_c and tuning range is because PMOS devices are inherently weaker than NMOS devices due to smaller hole mobility. The center frequency and tuning range can be further optimized by sizing the device's non-linearity. The dynamic power dissipated in the circuit at f_c is 1.29 mW. The dynamic power dissipation is less than 9.56 mW for all frequencies in the characteristics given in Table 2.3.

$$I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{ctr} - |V_{Tp}|)^2$$

VCO with both NMOS and PMOS control devices using same V_{ctr}.

When both NMOS and PMOS control devices are used and the same control voltage is applied to the gate of all control devices, the tuning range of 0 – 10 GHz with a centre frequency at 5.02 GHz is achieved. The circuit shows bell-shaped characteristics with two dead zones, thus restricting the allowable control voltage range to less than $V_{DD}/2$. Non-linearity in the characteristics can be reduced by ensuring that NMOS/PMOS control devices are in the saturation region for the entire range of the control voltage applied. The dynamic power dissipation is less than 6.76 mW owing to the lower frequencies at which the circuit operates.

VCO with both NMOS & PMOS control devices with complementary V_{ctr}.

Applying complementary voltages to NMOS and PMOS control devices resulted in a tuning range of 0 – 18 GHz with a centre frequency of 9.51 GHz. The tuning range can be further widened by sizing the devices appropriately. Again, the characteristics are non-linear owing to the switching of devices between operating regions. At f_c, the dynamic power dissipation is 1.556 mW, while it is less than 10 mW for all frequencies.

Table 3 Comparative study of performance metrics of VCO with multiple control schemes.

	f_c (GHz)	Tuning range (GHz)	Power Dissipation (mW)
NMOS only	13.88	0 – 30	12.55
PMOS only	12.52	0 – 25	9.56
NMOS/ PMOS with same V_{ctr}	5.02	0 – 10	6.76
NMOS/ PMOS with complementary V_{ctr}	9.51	0 – 18	1.55

Conclusion

In this work, a 3-stage CMOS voltage-controlled oscillator has been designed and implemented in 45 nm technology. Two designs have been proposed for the same topology design optimized for tuning range and design optimized for center frequency.

The performance analysis of the VCO characterized by its center frequency, tuning range, frequency stability, power dissipation and linearity has been carried out.

In CMOS analog design, selection of the CMOS process, selection of circuit topology and sizing of the devices provide decent design choices to optimize the performance and to meet the user specifications. In the chosen technology, the complimentary V_{ctr} in both NMOS PMOS circuits it is found that while sizing the devices there is a trade-off between power dissipation and center frequency. Similarly, there are trade-offs between frequency stability, linearity and tuning range. In this topology, variation with frequency stability is found to be good.

References

1. Behzad Razavi, “Design of analog CMOS integrated circuits”, Tata McGraw-Hill Publishing, Revised Edition, 2016.

2. G. Jovanovic, Stojcev, Stamenkovic, "A CMOS Voltage Controlled Ring Oscillator with Improved Frequency Stability", Scientific Publications of the State University of Novi Pazar, Vol. 2, I (2010).

3. Vandana Sikarwar, Neha Yadav, Shyam Akashe, “Design and analysis of CMOS ring oscillator using 45 nm technology”, 3rd IEEE International Advanced Computing Conference (IACC),2013, pp. 3-5.

4. Rupesh Kumar Patlani, Rekha Yadav,” Design of low power ring VCO and LC – VCO using 45 nm technology”, International Journal of Innovative Science, Engineering and Technology (IJISET), 2014, pp 1-2.

5. B.S. Patro, J.K. Panigrahi, Sushanta K. Mandal,” A 6–17 GHz linear wide tuning range and low power ring oscillator in 45nm CMOS process for electronic warfare”, International Conference on Communication, Information & Computing Technology (ICCICT), 2012, pp. 5-7.

6. Sajotra Deepak, Dhariwal Sandeep, Mishra Ravi Shankar” Comparative Analysis of Voltage Controlled Oscillator using CMOS”, Indian Journal of Science and Technology, Vol 9(14), pp. 5-8.

7. Jan M. Rabaey, A. Chandrakasan and B. Nikolic, *“Digital Integrated Circuits: A Design Perspective”*, Pearson Education, 2003.

8. H. A. Mahmoud and M. A. Bayoumi, “A 10-Transistor Low-Power High-Speed Full Adder Cell”, in *Proceedings of IEEE International Symposium on Circuits and Systems*, pp. 43-46, 1999.