Advanced DC-DC Converter with Triple Outputs for Spacecraft Power Distribution

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Abstract - *An electrical load is energized by a power source designed to precisely convert input current into the specific voltage, current, and frequency required for device functionality. Optimized transformer design is employed to minimize leakage inductance in the core winding, focusing on reducing energy loss, enhancing efficiency, and decreasing overall size and weight. Switched-mode power supplies (SMPS) are superior to linear supplies in achieving these objectives, with forward topology being particularly suited for low to medium-power applications due to its simplicity, cost-effectiveness, and ease of adding multiple outputs. However, forward topology presents challenges such as suboptimal cross-regulation and high voltage stress on the MOSFET switch, which are mitigated through the use of snubber circuits and coupled inductors. This project endeavors to design a triple-output forward converter with integrated protection circuits to enhance reliability. Utilizing the UC2825 PWM IC for primary side voltage mode control, the converter operates at a 500 KHz switching frequency. The final design, incorporating coupled inductors for improved regulation, achieves the targeted 82% efficiency.*

Keywords*: *Transformer Design, MOSFET Selection, External Synchronous Circuit, Coupled Inductors Topology, UC2825 PWM IC, UC2901 Isolated Feedback IC & Efficiency

1. INTRODUCTION

Switched-Mode Power Supplies (SMPS) offer advantages like higher efficiency, better voltage regulation, compact size, and multiple isolated outputs, making them a preferred replacement for linear power supplies. SMPS regulates power delivery through the on-off switching of semiconductor transistors. For low-output power applications (a few watts to under 100 watts) with isolated inputs and outputs, forward converter topology is simpler and cost-effective, despite being less efficient than other SMPS circuits. Forward converters use output inductance and freewheeling diodes, and Pulse Width Modulation (PWM) control is employed to maintain regulated output voltage by varying the MOSFET's duty cycle. In this project, the UC2825 PWM IC is used for voltage mode control, providing simple forward control, improved cross regulation, and a good noise margin. However, for better load and cross regulation in multi-output converters, coupled inductors are used. This triple-output forward converter is being designed for space applications, where reduced size, weight, and high reliability are critical. The design achieves the targeted efficiency of 82% as per the specifications.

1.1 Specification of the converter

Table 1 shows the specifications of the Converter.

Table.1: Converter Specifications

Parameter	Specifications
Input Voltage Range	60V - 100V DC
Nominal Input Voltage	70V DC
Topology	Forward DC-DC Isolated Converter
Switching Frequency	500 KHz
Output Voltage & Current	5V / 4A +15V / 0.667A -15V / 0.667A
Efficiency	78-82%
Line Regulation	1%
Load Regulation	2%
Duty Cycle	20-80%
Output Power	40 W
Output Voltage Ripple	<2%
Operating Temperature Range	–55°C to 125°C

1.2 Block Diagram

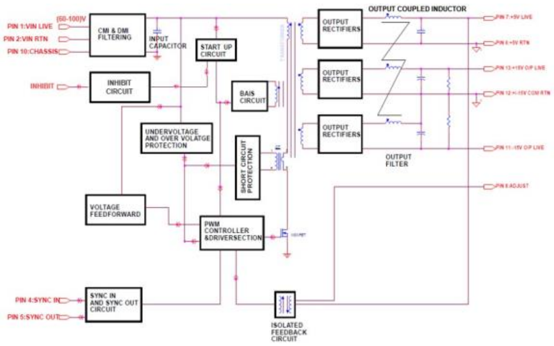

Fig-1: Block diagram of Proposed Converter

The schematic representation of the triple output forward converter is depicted in Figure 1. The system comprises an input section, a control section, a protection section, and an output stage. In addition to the bias voltage circuit derived from the auxiliary winding of a transformer, the input section also incorporates electromagnetic interference (EMI) filters, a start-up circuit, and several other components. An integrated circuit (IC) for PWM control, a MOSFET switch, and input from the bias winding constitute the control section. Output short circuit safety, input under-voltage protection, and output overvoltage protection.

All voltage protection measures are encompassed within the protection section. To provide isolation among the three outputs, each output is assigned a distinct ground potential. An electromagnetic interference (EMI) filter intercepts the input voltage and eliminates noise in both the differential and common modes. The initial power supply for the UC2825 PWM IC is derived from the start-up circuit. Once the converter is completely operational, the bias voltage, which exceeds the start-up voltage, will replace the start-up circuit. Here, a current sense resistor quantifies the primary side current provided to the UC2825 integrated circuit (IC) and compares it to the feedback error signal from the bias voltage feedback. This comparison generates pulse width modulation (PWM) signals that control the main MOSFET switch. By adjusting the gain and cutoff frequencies of the PWM integrated circuit, the switching frequency of the converter is subsequently adjusted to 500kHz. To provide the required RAW voltages, the secondary side outputs undergo correction and filtering by their respective Schottky diodes and output capacitors. The RAW voltages are transmitted to the corresponding linked inductors to generate the precisely controlled outputs of 5V/4A, +15V/0.667A, and -15V/0.667A in the output stage. In the event of any failures or abnormal situations in the protection circuits, the shutdown pin of the PWM IC is latched to inactivate the converter. Furthermore, the converter will not function unless the input undergoes reprocessing.

2. CONVERTER DESIGN

Transformer Design

An appropriate core will be selected which must have an area product greater than the calculated Ap. Area product (Ap) is given as the product of the core cross selection (Ac) and the window area (Aw). These data are available in the ferrite magnetic core design catalog. The area product method is used to calculate the size of a power transformer.

The selected core is YP-41605-TC, Material: P, Ur: 2500 with AL: 1375mH / 1000T.

$$Ap = Ac * Aw \quad (1)$$

$$Ap = \frac{\sqrt{Dmax} \times Pout \times (1 + \frac{1}{Eff})}{Kw \times J \times 10^{-6} \times Bm \times Fsw} \quad (2)$$

Where, Window factor, Kw = 0.4, Current density, J = 4Amp/$mm2$, Flux density, Bm = 0.1Tesla, Pout = 41.21W

Turns Ratio,

$$N_p = \frac{\left(V_{in_{min}} * D_{max}\right)}{B_m * A_c * 10^{-6} * F_{sw}} \quad (3)$$

$$T_{ratio} = \frac{N_s}{N_p} = \frac{V_{out} + (V_D * D_{max})}{D_{max} * V_{in_{min}}} \quad (4)$$

Selection of MOSFET switch

The choice of MOSFET is contingent upon several factors, including the Drain-Source voltage (VDS), Drain current (Id), Drain-Source ON resistance (Rds_on), Gate charge (Qg), and Output Capacitance (Coss). The selection and dimensions of a MOSFET are determined by the losses that occur within it.

$$V_{peak_{MOSFET}} = V_{in_{max}} * \left(1 + \frac{N_p}{N_{mag}}\right) \quad (7)$$

SELECTED IPP60R125CP / BUY65CS08J, 650V , 25A, 125mOhm, PG-TO220.

Output Filter

The secondary output voltage of Transformers is rectified and filtered in order to achieve the desired output parameters. The proposed converter utilizes an LC filter, and it is crucial to select the optimal values for this filter. This ensures that the converters have minimal noise, are compact, and cost-effective, which are the primary requirements for Space applications.

$$L = \frac{V_{out_s} * (1 - D_{min_s}) * T_s}{2 * \Delta I_L} \qquad (8)$$

$$C = \frac{(1 - D_{min_s}) * I_{out_s}}{8 * L * F_{sw}^2 * V_{D_{Delta}}} \qquad (9)$$

Secondary Diode Selection

The selection of the output diode is contingent upon the magnitude of the secondary current and voltage. The essential requirement for these diodes is that they must operate at high frequencies. During the transition from the ON state to the OFF state, the reverse recovery time of a standard signal or p-n diode typically ranges in the order of hundreds of nanoseconds.

However, for fast recovery diodes, this period is less than 100 nanoseconds. On the other hand, Schottky diodes have an extremely low reverse recovery time, almost nil. Schottky diodes are very appropriate due to their minimal forward voltage drop (VFD), high current capacity (IF), and low reverse recovery time (Trr)

Selected diode1 is 35CGQ100, 100V, 16A, 16CYQ100C (Industrial), and **a** SC105H100SCDV

Selected diode2 is 400V, 4A, 1N6627

Selected diode3 is 16CYQ150 (Industrial), 150V, 16A, SC125H150ACDV

3. SIMULATION RESULTS

A feedback path is provided to the system to improve its transient and steady-state response. A voltage controller with type 2 Compensation Technique is employed as feedback. Simulation is essential for any system's initial design. Simulation can be used to predict system behavior and performance. The output-regulated closed loop system is designed in LTspice software as shown in Fig2

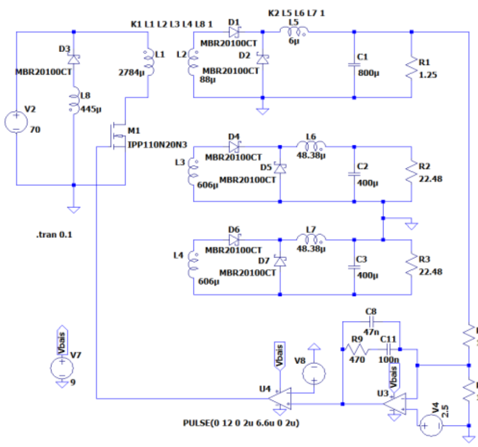

Fig-2: Circuit of Closed Loop Triple Output Forward Converter

Simulation waveform is shown in Fig -3, which includes the first Output voltage of 5V

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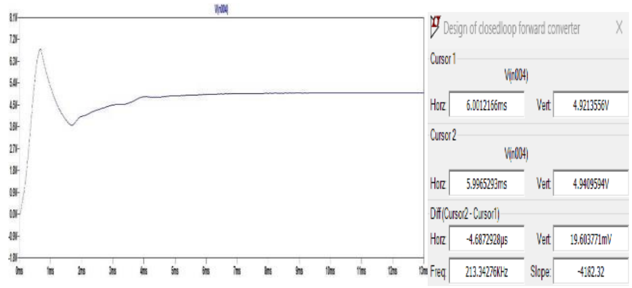


Fig-3: First Output Voltage

The simulation waveform is shown in Fig - 4, which includes the second Output voltage of +15V.

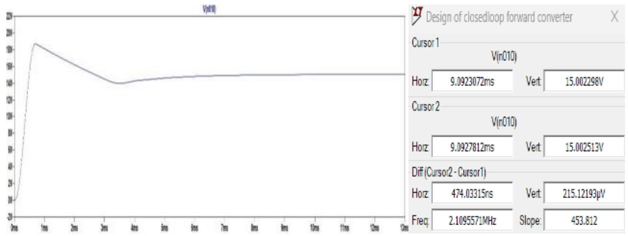


Fig-4: Second Output Voltage

The simulation waveform is shown in Fig - 5, which includes the third Output voltage of -15V.

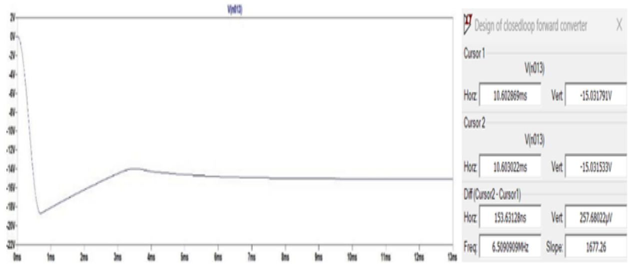


Fig-5: Third Output Voltage

4. HARDWARE EXPERIMENTAL RESULTS

The experimental setup for the triple-output forward converter is depicted in Fig- 6. Components of the experimental setup include a digital storage oscilloscope (DSO), converter, electronic load, pulse generator, multimeter, and input power supply. Regulation of the input voltage is possible within 60 to 100 volts at the minimum, nominal, and maximum load levels. The table above displays the statistical measures of efficiency, line regulation, load regulation, cross-regulation, and ripple voltages. Tabular format displays the test results obtained under full load.

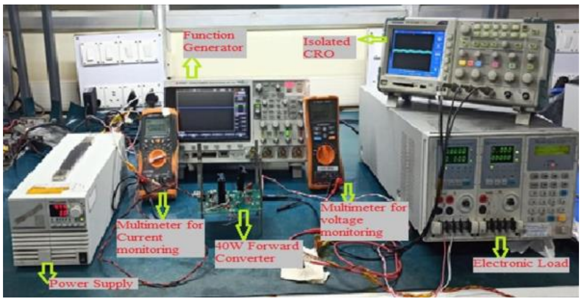


Fig-6: Hardware Setup for a Triple Output 40W Converter

As shown in Table 2 below, the output voltage is determined at varying input voltages and load conditions. At the minimum and the maximum values, input current, input power, and output power, efficiency are observed to be 82%.

Table -2: Output voltages at full load from 60V - 100V input voltages & efficiency

Vin (V)	5V O/P	+15V O/P	-15V O/P	Efficiency (%)
	Vout1	Vout2	Vout3	
60	4.927	14.930	15.050	82.7
70	4.927	14.936	15.050	81.0
100	4.947	14.900	15.040	82.8

The ripple voltage in Table-3 is under 50mV as mentioned in the specification

Table -3: Output ripple voltages at 100% load from 60V - 100V input voltages & efficiency

Vin (V)	Output Ripple Voltage (mV)		
	Spec: Nom: 20mV Max: 50mV		
	5V O/P	+15V O/P	-15V O/P
	Vout1	Vout2	Vout3
60	16	18	28
70	30.4	22	22
100	16	24	22

Line Regulation in Table 4 is less than 1% as mentioned in the specification

Table -4: Line Regulation at full load

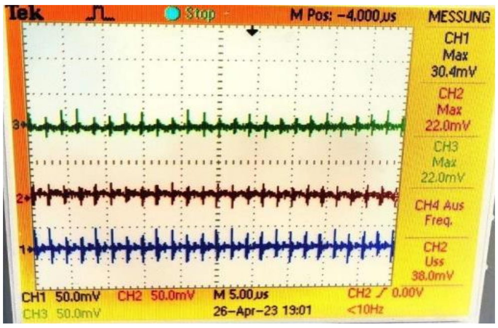
Vin (V)	Load Cond	Line Regulation (%)		
		5V O/P	+15V O/P	-15V O/P
		Vout1	Vout2	Vout3
60	10%	0.00	0.6265	0.6266
	100%	0.0072	0.033	0.006
100	10%	0.00	0.54	0.56
	100%	0.023	0.039	0.039

Load Regulation in Table 5 is less than 2% as mentioned in the specification

Table -5: Output ripple voltages at 100% load from 60V - 100V input voltages & efficiency

Vin (V)	Load Regulation (%)		
	5V O/P	+15V O/P	-15V O/P
	Vout1	Vout2	Vout3
60	0.18	2.01	1.99
70	0.189	2.00	1.98
100	0.213	1.54	1.59

The 40W DC-DC triple output forward converter has ripples that all are within specification like 30.4mV, 22mV, and 22mV at maximum load and nominal voltage is shown in Fig.-7.



Fiig-7: Input Voltage**:** 70V, CH1: 5V/4A, CH2: +15V/0.667A, CH3: -15V/0.667A

As shown in Fig.5, the MOSFET gate voltage output waveform of the 40W DC-DC triple output forward converter has a gate voltage of 10.2V, which is within the specified range.

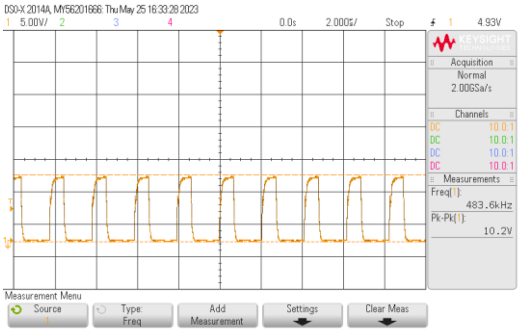


Fig-8: Input Voltage: 70V, Nom. Gate Voltage: 10.2V

The 40W DC-DC triple output forward converter's MOSFET drain voltage output waveform is illustrated in Fig.6 with a full load and the nominal voltage, and it is within specifications with a 129V drain voltage.

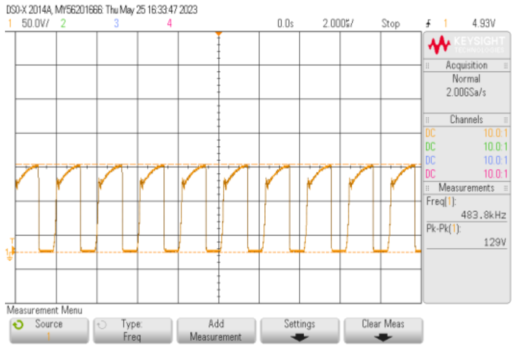


Fig-9: Input Voltage: 70V, Nom. Drain Voltage: 129V

3. CONCLUSIONS

This study presents the implementation of a triple output isolated forward converter using the voltage mode control approach and linked inductor as post regulators. Optimally built post regulators effectively control output voltages to fall well within the intended range. Based on the experimentally verified experimental findings obtained at full load 100% with different input voltages, it is evident that the output ripple, MOSFET stress, Diode stress, Line regulation, and Load regulation all meet the specified requirements. The implementation of a snubber circuit enhances the overall efficiency of the converter by 4-5%. A potential area for further study is enhancing the digitally controlled MOSFET feedforward.

This analysis is specific to space applications. The hardware verification of the design follow-up has been conducted for all three outputs. The simulation and hardware experimental findings, as well as the waveforms, are presented.

REFERENCES

[1] S.Zaharieva, I.Stoev, A.Borodzheva, S.Stoyanov,"Study of Switching Forward Single Ended DC-DC Converter in the Course Power Supplies", 2020 43rd International Convention on Information, Communication and Electronic Technology (MIPRD).M. Young, The Technical Writer's Handbook. Mill Valley, CA: University Science, 1989.

[2] Soumya K, Arpitha Raju B, Bhanuprakash CV, B.K.Singh, "Single Output 40W DC-DC Forward Converter for Space Application", 05 May 2022 International Research Journal of Engineering and Technology (IRJET).K. Elissa, "Title of paper if known," unpublished.

[3] Nagesh L, Bhanuprakash CV, B.K.Singh, Vinod Chippalakatti, "Design and implementation of Triple Output Forward DC-DCConverter with Coupled Inductor as Post-Regulator for Space Application," 2020 International Conference on Smart Technologies in Computing, Electrical and Electronics (ICSTCEE).

[4] Aravind Bhat, K.Uma Rao, Praveen PK, Bhoopendra Kumar Singh, Vinod Chippalkatti,"Multiple Output Forward DC-DC Converter with Regenerative Snubber for Space Application," 2016 Biennial International Conference on Power and Energy Systems Towards Sustainable Energy (PESTSE).

[5] Suresh Kumar Tummala, Lenine Duraiswamy,"Switched Mode Power Supply:A High Efficient Low Noise Forward ConverterDesign Topology," 2022 IEEE 2nd International Conference on Sustainable Energy and Future Electric Transportation.

[6] Congwen Xu, Qishuang Ma, Ping Xu and Nan Wang,"Closed-Loop Gate Drive for Single-Ended Forward Converter to ReduceConducted EMI," 26 June 2020 Published in IEEE Access.

[7]].G.R.P.Lakshmi,"A Dual-Transformer Active-Clamp Forward Converter using a Single Switch," 2017 International Conference on Computation of Power, Energy, Information and Communication (ICCPEIC).