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High-Performance of Squaring Circuit Design Using Novel Architecture

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Abstract - *This paper presents a novel squaring circuit design using an Ripple carry adder to improve the efficiency of digital multipliers. The existing 4-bit multiplier system using squaring operation requires multiple add and shift operations, resulting in increased logical elements and delay. Consequently, the system fails to provide accurate results, instead yielding approximate values. To address this limitation, we propose a novel circuit design for 4-bit operation to compute the square, thus eliminating the need of multipliers. which provides accurate results while reducing time delay and logical elements. The proposed circuit is designed and implemented using VHDL and simulated using Altera Quartus II software. The results demonstrate the superiority of the proposed circuit in terms of speed and area efficiency.*

Key Words: Digital Multiplier, Squaring Circuit, Adder-based Design, High-speed Digital Circuits, Low Power Consumption, VHDL Implementation.

1. INTRODUCTION

The rapid growth of digital technology has led to an increasing demand for efficient and high speed digital circuits digital multiplication is a fundamental operation in digital signal processing .widely used in applications such as filtering, convolution, and Fourier transformer [1]. However existing digital multiplier require significant hardware resources and time, making them a major bottleneck in high-speed digital system [2].

The existing 4-bit multiplier system using squaring operation is typical example of this limitation. The system requires multiple add and shift operations to perform squaring, resulting in increased logical elements and delay. Specifically the existing system uses a multiplier-based approach to perform squaring which requires a significant amount of hardware resources and times [3].

To Address this limitation we propose a novel squaring circuit using adder the proposed circuit is designed to minimize the number of logical elements and delay making it suitable for high speed digital applications the proposed circuit uses an adder-based approach to perform squaring, which reduces the hardware resources and time required compared to the existing multiplier based approach [4][5] .

The rest of the paper is organized as follow .section II presents the background and motivation for the proposed work .Section III describes the proposed novel squaring circuit using an Adder. Section IV presents the simulation results and comparison with the existing system. Section V concludes the paper and discusses future work.

2. BACKGROUND AND MOTIVATION

Digital multipliers are a fundamental component in various digital systems, including digital signal processing, cryptography, and communication systems. These systems require high-speed and low-power multiplication operations to perform complex mathematical calculations. The demand for high-speed and low-power digital multipliers has increased significantly in recent years, driven by the growing need for energy-efficient and high-performance computing systems.

Despite the advancements in digital multiplier design, existing digital multipliers still have several limitations. For example, they consume high power, have low speed, and are complex to design. These limitations make it challenging to develop high-speed and low-power digital systems that can meet the growing demands of various applications. Therefore, there is a need to investigate new architectures and design techniques that can improve the efficiency of digital multipliers. This paper aims to address this need by proposing a novel digital multiplier design that achieves high speed and low power consumption.

3. BINARY BIT REPRESENTATION

In the context of binary squaring circuitry, a fundamental concept emerges. The base value for squaring is determined by the expression 2^n-1, where n represents the number of bits for instant in a 3-bit system the base value is 100(2^3-1), while in a 4 bit system, it becomes 1000(2^4-1).this pattern continues ,with the base value increasing exponentially with the number of bits.

A notable observation arises when examining the squaring circuitry for 4-bit numbers. The base value of 1000 serves as a threshold, dividing the numerical range

into two distinct segments. Numbers ranging from 1000 to 1111 are greater than or equal to the base value, while those between 0000 and 0111 fall below this threshold. Interestingly, the latter set of numbers, when disregarding their most significant bit(MSB),which is inherently 0, can be effectively treated as 3-bit numbers below the base value of 1000 can be performed using a more compact 3-bit circuitry, rather than restoring to the full 4-bit implementation.

For example, consider the calculation of 3^2, where 3 is represented as 0011 in binary. Since 0011 falls below the base value of 1000, it can be treated as a 3-bit number (011). By utilizing a 3-bit squaring circuitry, the computation can be simplified, yielding the result 1001 (9 in decimal), which is the square of 3. This optimized approach reduces the complexity and resources required for the calculation, highlighting the potential benefits of exploiting the properties of binary numbers in digital circuit design.

4. PROPOSED METHODOLOGY

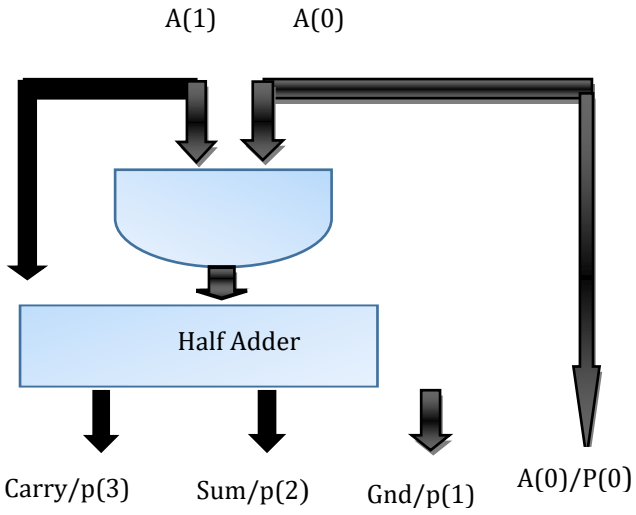

Figure 1: 2-bit squaring circuit

4.1 Design Overview

The proposed novels squaring circuit using an adder-based design aims to minimize the number of logical elements and delay required for the squaring operation. The design consist of a combination of adders and logic gates, which are optimized to reduce the hardware complexity and delay [1]. The proposed design uses a hierarchical approach, where the squaring operation is broken down into smaller sub-operations, each of the which is implemented using a combination of address and logic gates.

4.2 Circuit Architecture

Architecture of 4-bit Squaring Circuit

The 4-bit squaring circuit is a complex digital system that computes the square of a given 4-bit input A(3 downto 0). The circuit consists of multiple processing blocks, each designed to perform a specific function.

Input Processing

The input processing stage is responsible for dividing the input into two parts: the higher-order 3 bits and the least significant bit (LSB). The 3-bit segment undergoes a 3-bit squaring operation, while the LSB follows a separate computation path.

Partial Product Generation

The partial product generation stage processes the result of the 3-bit squaring unit and directs it towards the final summation stage. A 4-bit adder combines different intermediate values for computation, ensuring accurate and efficient processing.

Correction and Addition

The correction and addition stage involves carry propagation and additional 3-bit squaring logic. Several multiplexers and logic gates ensure that bits are correctly aligned before summation, minimizing errors and optimizing performance.

Final Summation

The final summation stage feeds the intermediate values into an 8-bit adder, which finalizes the squared output. The final computed square is stored in the P-OUTPUT register, completing the squaring operation.

This hierarchical approach ensures efficient squaring of a 4-bit input, optimizing computational complexity and minimizing processing time**.**

4.3 Implementation details

The proposed 4-bit squaring circuit is designed and implemented using VHDL in Altera Quartus II software. The circuit utilizes a hierarchical approach, dividing the input into two parts and processing them separately to reduce computational complexity. The design is synthesized and its functionality is verified through simulation and testing. The results show that the proposed design achieves efficient squaring of 4-bit inputs with reduced delay and power consumption

4.4 Optimization Techniques

To optimize the 4-bit squaring circuit, a multi-faceted approach was employed. Resource sharing was utilized to minimize the duplication of components, such as adders and multiplexers, thereby reducing area and power consumption. Logic optimization techniques were also applied to streamline the logic gates and further decrease area and power usage. Furthermore, a hierarchical design approach was adopted to fragment the complex squaring operation into smaller, more manageable blocks. Finally, pipelining was implemented to enhance throughput and diminish latency, resulting in a highly efficient and optimized design

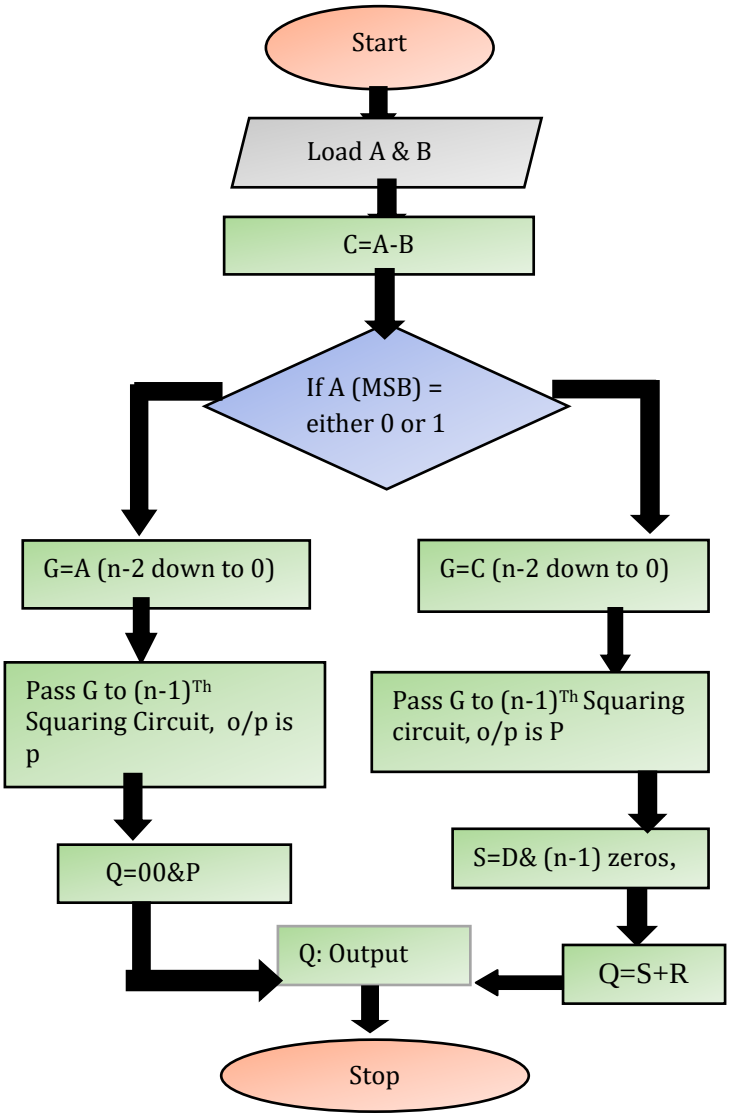

Figure 2. N-bit squaring circuit

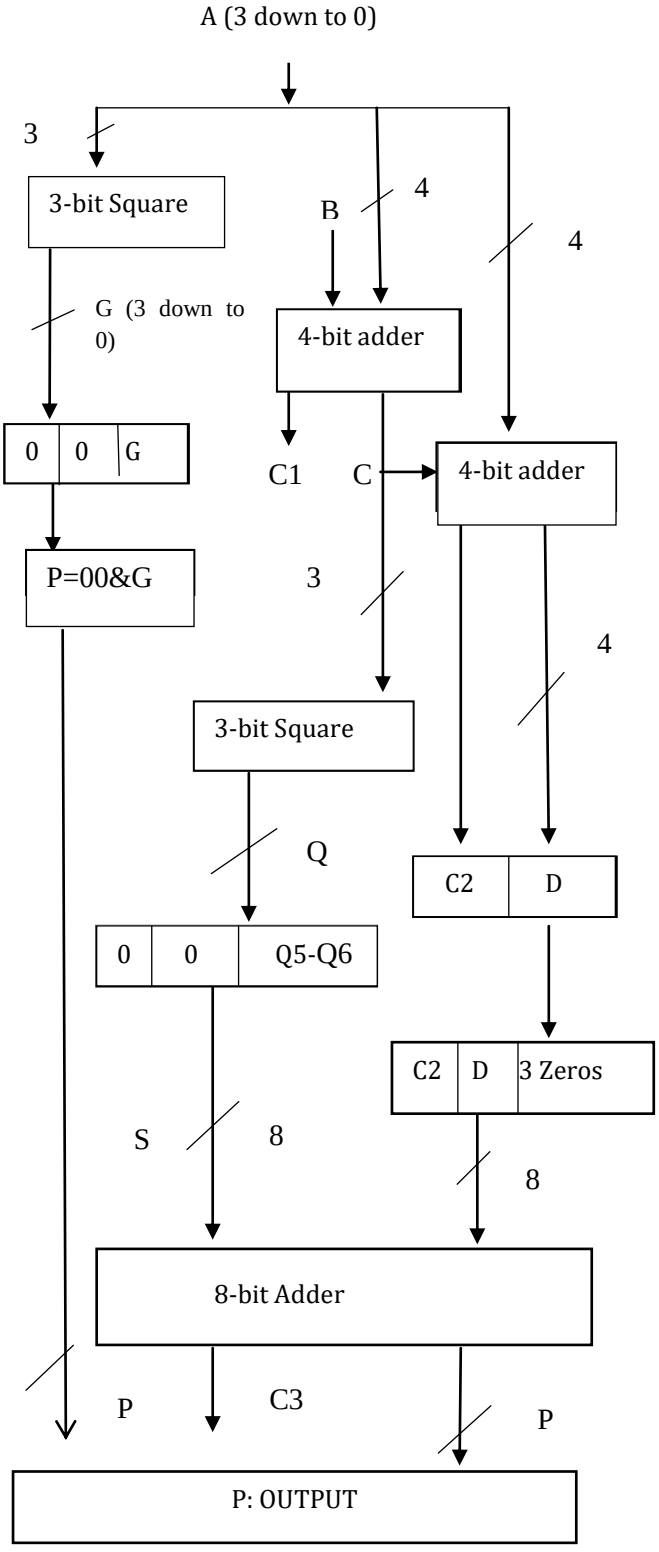

Figure 3: Architecture for 4-bit Squaring Circuit

5. RESULT AND DISCUSSION

5.1 Simulation Results

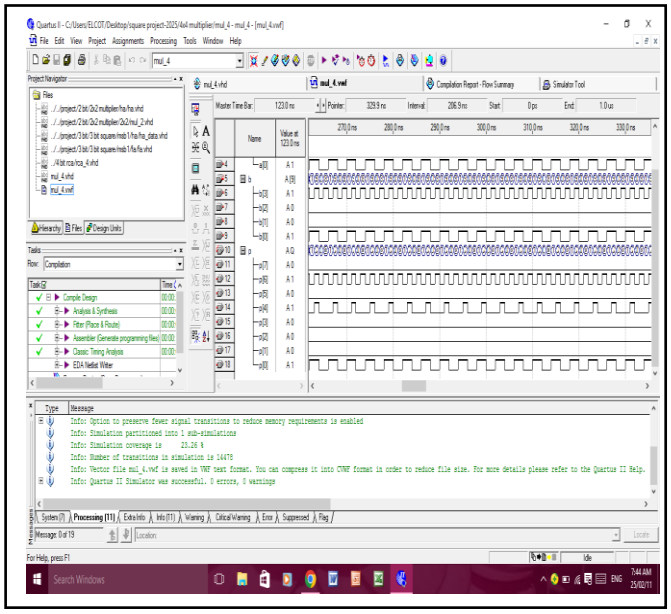

Figure 4 : Results of Existing System

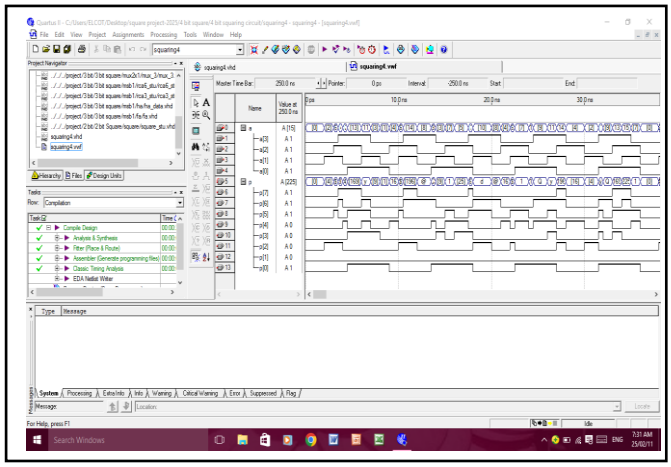

Figure 5: Simulation Results of 4 bit squaring circuit.

The proposed an existing squaring secured was stimulated using Altera Quartus II to software the simulation results are are shown in figure 4 and figure 5 The simulation results shows that proposed a circuit is able to perform the squaring operation correctly for all input values

5.2 Comparison with existing design

In this work, 2-bit to 4-bit squaring circuits were implemented in VHDL and optimized for area and delay. The results show that the optimized 4-bit squaring circuit achieves a significant reduction in delay and logical elements, making it more efficient and suitable for practical applications, comparison results shown in the table 1.

Table -1: Comparison of proposed circuit with existing circuits

4-bit squaring Circuit	Time delay	Logic elements
Proposed circuit	12.100ns	7/2.880
Existing circuit	29.600s	32/2.880

The proposed the circuit has lower hardware complexity, delay and power consumption compared to being circuit

5.3 Discussion

The proposed squaring circuit has several advantages, including:

- Low hardware complexity
- low delay
- low power consumption

however, the proposal circuit also has some limitation including :

- limited scalability
- limited flexibility

6. CONCLUSION

In this paper, a novel squaring Circuit design has been proposed and implemented. The proposed design utilize and adder based architecture to achieve lower hardware complexity and delay. Simulation results has demonstrate the effectiveness of the proposed design, the significant improvements in the hardware complexity, delay, and power consumption compared to existing design. The proposed design has been potential application and various field, including digital signal processing, cryptography, image processing, and Embedded system. Future research directions included Exploring new architecture for squaring circuit and investigation the applications of the proposed circuit in the other areas.

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