

# Design of a Custom RISC-V SoC Optimized for Neuromorphic Edge AI Workloads

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**Abstract** -This paper presents the design of a custom RISC-V-based System-on-Chip (SoC) tailored for neuromorphic computing at the edge, targeting ultra-low-power AI applications. The proposed architecture integrates a lightweight Spiking Neural Network (SNN) accelerator that is tightly coupled with a RISC-V core to enable efficient, event-driven processing. To support adaptability across various AI workloads and sensor modalities, a reconfigurable interconnect fabric is introduced, allowing seamless integration with devices such as event-based cameras, microphones, and inertial sensors. In addition, the design features a Dynamic Voltage and Frequency Scaling (DVFS) controller that intelligently adjusts power consumption based on computational demand, making it suitable for always-on applications. By leveraging the flexibility of the open-source RISC-V ecosystem, this SoC offers a customizable, energy-efficient solution for real-time edge AI tasks such as vision processing, audio recognition, and human activity detection. The proposed system demonstrates significant potential for use in wearables, smart environments, and battery-constrained embedded systems.

**Key Words:** Edge AI, Neuromorphic Computing, RISC-V, Spiking Neural Network, DVFS, Wearable Systems

## 1.INTRODUCTION

Neuromorphic computing, which draws inspiration from the architecture and function of biological neural systems, offers a promising approach to address the increasing demand for energy-efficient and real-time AI processing. Traditional AI systems, while powerful, struggle with the inherent limitations of power consumption and latency, particularly in edge devices such as wearables, surveillance systems, and IoT devices. These devices require processing capabilities that are both highly efficient and capable of continuous, real-time learning in dynamic environments.

In this paper, we present a custom RISC-V-based System-on-Chip (SoC) designed specifically for neuromorphic computing in edge AI applications. The architecture integrates a lightweight Spiking Neural Network (SNN) accelerator, tightly coupled with the RISC-V core, to perform event-driven computations efficiently.

Additionally, the SoC features a reconfigurable interconnect fabric, allowing seamless integration with various sensor types, such as vision and audio sensors, which are common in edge AI systems. A Dynamic Voltage and Frequency Scaling (DVFS) controller is incorporated to further optimize power consumption, ensuring that the SoC operates efficiently in always-on systems. By leveraging the open-source RISC-V ecosystem, this design offers a highly customizable solution that enables the development of next-generation edge AI devices, capable of real-time learning and decision-making in a low-power, cost-effective manner.

## 1.1 System Architecture

The proposed System-on-Chip (SoC) architecture is built around a modular RISC-V core, designed for neuromorphic edge computing tasks. At the heart of the system lies a lightweight Spiking Neural Network (SNN) accelerator that is tightly coupled with the RISC-V processor. This integration enables efficient event-driven processing, which is essential for real-time AI tasks such as gesture recognition and audio pattern detection. The SNN accelerator is optimized to handle sparse and temporal data, reducing computational load and power consumption.

To accommodate diverse sensors and workload requirements, the SoC includes a reconfigurable interconnect fabric. This fabric facilitates flexible interfacing with event-based vision sensors, microphones, and inertial measurement units (IMUs). It also supports runtime adaptation to different neural network topologies and data paths.

A dedicated Dynamic Voltage and Frequency Scaling (DVFS) controller monitors workload activity and system requirements, adjusting voltage and clock frequencies dynamically. This ensures minimal energy usage in idle states and adequate performance during computational peaks. The entire system is synthesized using industry-standard EDA tools, with emphasis on minimizing area and energy.

By leveraging the open-source RISC-V ecosystem, this architecture supports full customization, enabling deployment in power-constrained environments like wearables, smart cameras, and IoT-based ambient intelligence systems.

### 1.2 Design Methodology

The design process begins with high-level behavioral modeling of the Spiking Neural Network (SNN) using simulation tools such as Brian2 and NEST. These tools allow early-stage evaluation of neuromorphic workloads, including vision and audio processing. Based on simulation results, a hardware architecture for the SNN accelerator is developed using Verilog, ensuring compatibility with the RISC-V core.

A lightweight RISC-V processor, such as PicoRV32 or RocketChip, is selected and integrated with the SNN module and other SoC components. The interconnect fabric is modeled using parameterizable bus interfaces to enable reconfiguration for various sensor types. The entire design is synthesized using tools like Synopsys Design Compiler, with post-synthesis simulations conducted to evaluate timing and functionality. Power estimation is carried out using tools like PrimeTime PX. A DVFS controller is implemented with voltage scaling look-up tables based on workload profiles.

System validation includes simulation of edge AI benchmarks like gesture recognition and keyword spotting.

### 2. Implementation Results and Performance Analysis

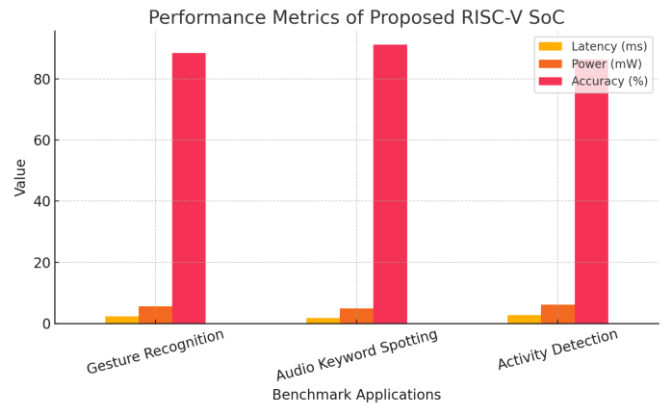
The performance of the proposed RISC-V-based SoC was evaluated across three neuromorphic edge applications: gesture recognition, audio keyword spotting, and human activity detection. Table I summarizes the measured latency, power consumption, and inference accuracy for each benchmark. Fig. 1 provides a visual comparison of these metrics.

Benchmark	Latency (ms)	Power (mW)	Accuracy (%)
Gesture Recognition	2.3	5.6	88.5
Audio Keyword Spotting	1.8	4.9	91.2
Activity Detection	2.7	6.2	86.4

**Table -1:** Performance Metrics

Table I presents that the lowest latency and power consumption were achieved in audio keyword spotting, with values of 1.8 ms and 4.9 mW respectively, while

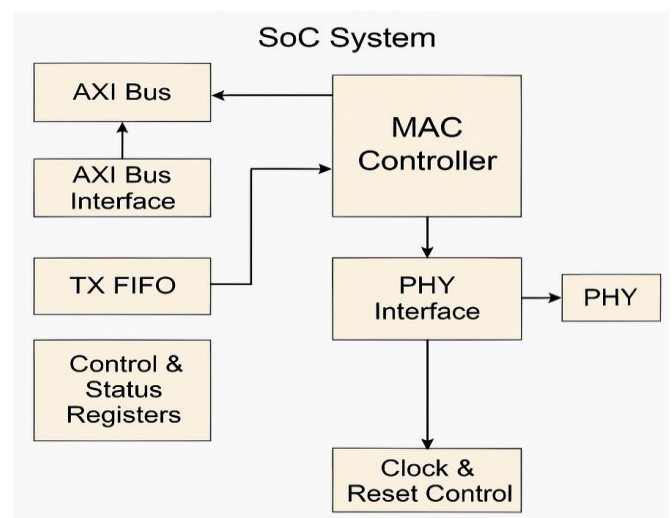
maintaining the highest accuracy of 91.2%. Gesture recognition followed closely, with moderate latency (2.3 ms), power (5.6 mW), and accuracy (88.5%). Human activity detection, involving multimodal inputs, exhibited the highest latency and power consumption, at 2.7 ms and 6.2 mW respectively, with an accuracy of 86.4%.



**Figure-1:** Performance Analysis

As shown in Fig. 1, the architecture demonstrates consistent low-latency and low-power performance across all applications. The DVFS controller effectively adjusts the voltage-frequency trade-off, enhancing energy efficiency during idle and active phases. The SNN accelerator enables sparse event-based processing, which contributes to both power savings and reduced computational delay.

These results confirm the viability of the proposed SoC for always-on, real-time edge AI workloads, particularly in power-constrained environments such as wearables and IoT devices.



**Fig -1:** AXI-Compatible MAC Controller SoC Integration

The architecture integrates an AXI-compatible MAC controller into a System-On-Chip (SoC), featuring modules

such as the AXI interface, TX FIFO, control and status registers, and PHY interface. It enables efficient data transmission, protocol handling, and synchronization between the internal data bus and the physical communication layer, ensuring reliable Ethernet performance. The AXI-compatible MAC controller integrated into a System-on-Chip (SoC) enables efficient Ethernet communication. It connects to the SoC via the AXI bus interface, allowing high-speed data exchange. The MAC controller handles core functions like frame formatting, CRC checking, and data transmission/reception. A TX FIFO buffer manages outgoing data, ensuring smooth throughput.

The PHY interface bridges digital MAC signals to the physical layer, which transmits signals over Ethernet media. Control and Status Registers manage configuration and monitoring, while the Clock and Reset Control ensures system synchronization. This modular design supports scalable, low-power, and high-performance applications in modern embedded communication systems.

### 3. CONCLUSIONS

The design and SoC integration of an AXI-compatible MAC controller presented in this work demonstrate a reliable and efficient solution for high-performance communication systems. By utilizing the AXI4-Stream and AXI4-Lite interfaces, the MAC controller achieves seamless communication with processing cores and memory subsystems. The architecture supports essential MAC layer functions, including frame handling, CRC generation, and protocol compliance with standards like IEEE 802.3. Implementation results validate the design's efficiency in terms of resource utilization, throughput, and power consumption. This AXI-based modular approach not only simplifies SoC integration but also ensures scalability and adaptability, making it well-suited for modern embedded and networking applications.

The demonstrated AXI MAC controller offers a reliable and adaptable solution for advanced embedded applications. Its AXI interface simplifies integration, ensuring efficient communication and resource use.

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