

Design and Synthesis of Majority Logic Gate Based MAC Units with FPGA and ASIC Evaluation

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Abstract - In this project, 4×4 and 8×8 Multiply-Accumulate (MAC) units based on Majority Logic Gates (MLGs) are designed and evaluated. While partial products are produced using traditional logic, MLG is utilized in the arithmetic phase of the suggested design, namely in the full adders and multiplier reduction path. In order to confirm functionality and examine resource usage, timing, and power, the MAC units were initially simulated and synthesized on FPGA using Xilinx Vivado. The same MAC designs were functionally validated and synthesized using Ubuntu, Yosys, OpenLane, and OpenROAD, and their area, latency, and power were measured in order to better assess the design in an ASIC context. After the initial development and analysis of the 4×4 MLG MAC, the same design concept was expanded to an 8×8 MLG MAC. Functional verification verified that both setups' multiply-and-accumulate operations were accurate. The project highlights the trade-offs between MAC size, area, delay, and power and shows that MLG-based arithmetic can be implemented and studied on both FPGA and ASIC platforms.

Key Words: Multiply-Accumulate (MAC) units¹, Majority Logic Gates (MLGs)², FPGA³, ASIC⁴, MLG-based arithmetic⁵ etc.

1. INTRODUCTION

Multiply-Accumulate (MAC) units are essential parts of contemporary digital systems and are widely employed in machine learning, image processing, and digital signal processing. The MAC unit's efficiency in terms of space, latency, and power consumption has a significant impact on these systems' performance. Boolean logic-based arithmetic units, which rely on numerous logic gates like AND, OR, and XOR, are commonly used to create conventional MAC architectures. Particularly as the design grows, this results in higher switching activity, more sophisticated circuitry, and ultimately higher power consumption.

In this work, Majority Logic Gate (MLG)-based design is integrated into the arithmetic section of the MAC unit, specifically in the design of full adders and in the multiplier reduction path, while partial product generation is retained using conventional logic for reliability. MLG-based

design offers a promising solution to these limitations. Majority logic enables compact realization of arithmetic functions by reducing the number of logic levels and simplifying carry propagation in adders.

In order to investigate scalability and performance trade-offs, the suggested MAC designs are constructed in both 4×4 and 8×8 configurations. In order to assess the designs' performance on various platforms, they are functionally validated and synthesized utilizing FPGA and ASIC design procedures. While Yosys with Sky130 standard cell libraries is used for ASIC synthesis and OpenROAD is used for area, delay, and power analysis, Xilinx Vivado is used for FPGA implementation to study resource consumption, timing, and power. The outcomes show that MLG-based MAC design is feasible and shed light on the trade-offs between power consumption, performance, and design size.

2. PROPOSED ARCHITECTURE

The design of Majority Logic Gate (MLG)-based Multiply-Accumulate (MAC) units in 4×4 and 8×8 configurations is shown in the proposed work. By adding majority logic to crucial arithmetic components, the architecture is designed to increase computing efficiency while preserving reliability through traditional partial product generation.

2.1 Overall MAC Structure

The three primary phases of the overall architecture are accumulation, reduction and addition, and partial product creation. An array-based structure is used to perform the multiplication operation, and a register-based accumulator is used to aggregate the result over a series of clock cycles.

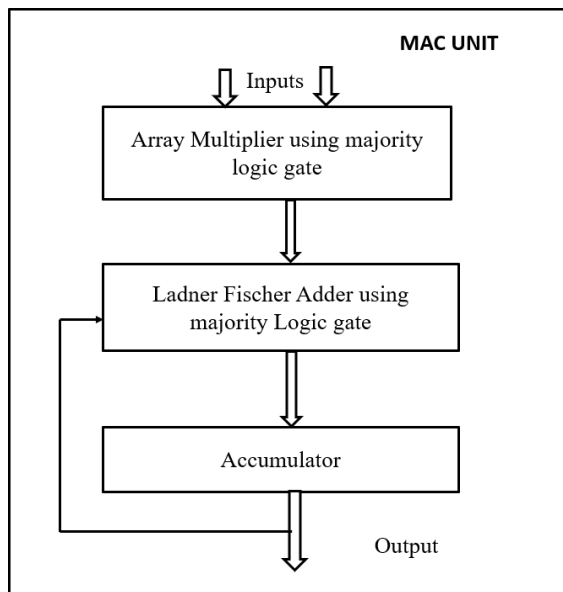


Fig -1: Overall MAC Structure

Table -1: Truth table of Majority Logic Gate

| Input | | | Output |
|-------|---|-----------------|--------|
| A | B | C _{in} | Y |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

2.2 Majority Logic Gate Fundamentals

The Majority Logic Gate (MLG) is a fundamental building block used in the proposed design. A 3-input MLG produces an output based on the majority of its inputs and is defined as:

$$F = AB + BC + CA$$

The symbol and truth table of the MLG are shown in Fig. 2 and Table 1, respectively.

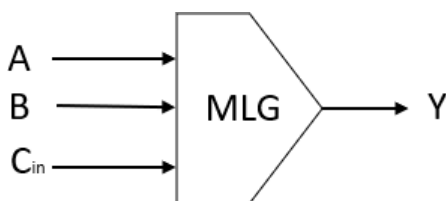


Fig -2: Majority Logic Gate Symbol

2.3 Partial Product Generation

The suggested architecture uses traditional AND-based logic to build partial products. A matrix of partial products is created for a $N \times N$ MAC by ANDing each bit of the multiplicand with each bit of the multiplier. By avoiding approximation in the most crucial part of the computation, this method guarantees accuracy and simplicity in the first multiplication stage.

2.4 MLG-Based Reduction and Addition

The usage of Majority Logic Gates in the arithmetic portion, specifically in Full Adder Design and Multiplier Reduction Path, is the main contribution of the suggested architecture. The employment of Majority Logic Gates in the arithmetic area, specifically in:

$$C_{out} = \text{Majority}(A, B, C_{in})$$

and majority logic and inversion are combined to determine the sum. Compared to traditional XOR-based full adders, this lowers the number of logic levels and streamlines carry propagation.

A network of MLG-based full adders is used in the multiplier reduction path to aggregate several partial products. By effectively compressing the partial product matrix, this reduction stage reduces switching activity and logic depth. The concept reduces hardware complexity and improves power efficiency by substituting MLG-based implementations for traditional adder architectures.

2.5 Accumulation Unit

A register that holds the MAC operation's intermediate result is used to implement the accumulation stage. The multiplier's output is added to the previously accumulated value at each clock cycle. A synchronous register-based structure is used to do this, allowing multiplication results to be accumulated sequentially.

2.6 4 × 4 MAC Architecture

The base design is a 4×4 MAC unit. It includes:

- 4-bit inputs B [3:0] and A [3:0]
- Using AND logic to generate a partial product
- Reduction with complete adders based on MLG
- An output of an 8-bit product
- An accumulator based on registers

This setup is used to examine the MLG-based approach's performance in terms of area, delay, and power as well as to verify that it is correct.

2.7 8 × 8 MAC Architecture

By expanding the same design ideas, the suggested architecture is expanded to an 8×8 MAC unit. The 8×8 MAC consists of:

- A [7:0] and B [7:0] are 8-bit inputs.
- A bigger matrix of partial products
- A larger reduction network based on MLG
- The outcome of a 16-bit multiplication
- For sequential addition, a broader accumulator

By methodically increasing the number of partial products and matching reduction stages while preserving the MLG-based adder structure, the architecture is made scalable. This makes it possible to examine how the design responds to larger operand sizes, especially with regard to trade-offs between area, latency, and power.

2.8 Design Significance

For arithmetic operations, the suggested MLG-based MAC architecture provides a scalable and effective solution. The design achieves regulated power behavior and decreased logic complexity by incorporating majority logic into crucial computing stages, making it appropriate for contemporary VLSI applications.

3. Design Methodology

Both FPGA and ASIC design flows were used in the design, verification, and evaluation of the suggested Majority Logic Gate (MLG)-based MAC designs in order to assess their performance on various platforms. RTL design, functional verification, synthesis, and performance analysis are all part of the technique.

3.1 RTL Design and Functional Verification

Verilog HDL was used to describe the MAC units in both 4×4 and 8×8 designs. The design consists of modules for accumulation, multiplier reduction, MLG-based full adders, and partial product creation. By applying several input combinations and tracking the cumulative output over clock cycles, a testbench was created to confirm the MAC unit's operation.

The accuracy of the multiply-accumulate process was confirmed through functional verification utilizing simulation tools. To guarantee correct synchronization between input operands, multiplication outcomes, and accumulation behavior, the simulation results were examined using waveform viewers.

3.2 FPGA Synthesis and Analysis

The suggested MAC architectures were created using Xilinx Vivado in order to assess the idea in an FPGA environment. Key performance metrics, including the following, were obtained by synthesizing and implementing the RTL design:

- Logic Utilization (LUTs)
- Register Utilization
- Timing performance
- Consumption of power

An initial evaluation of the design's resource usage and operational effectiveness is given by the FPGA synthesis results. Additionally, this stage verifies that the design is both synthesizable for hardware realization and functionally valid.

3.3 ASIC Synthesis and Using Yosys

Yosys is an open-source synthesis program that was used to create the same RTL design for ASIC evaluation. RTL-to-gate-level synthesis was used to process the Verilog design, and the Sky130 standard cell library was used to carry out technology mapping. The synthesis flow consists of:

- Reading Verilog RTL files
- Performing logic synthesis

- Mapping to Sky130 standard cells
- Generating a gate-level netlist

In this stage, a technology-specific netlist appropriate for ASIC analysis is created from the high-level RTL design.

3.4 Timing, Area, and Power Analysis Using OpenROAD

To estimate important performance metrics, OpenROAD was used for additional analysis of the generated gate-level netlist. A specified clock period was used to apply timing constraints, and the design was connected to the matching standard cell libraries. The metrics listed below were obtained:

- Area: Estimated based on the total standard cell utilization
- Delay: Evaluated using static timing analysis (STA)
- Power: Estimated using switching activity and cell-level power models

Without complete physical implementation, this step offers a rough assessment of the design in an ASIC context.

3.5 Methodology Significance

The suggested methodology allows for a thorough assessment of the MLG-based MAC architecture by integrating FPGA and ASIC processes. While the ASIC synthesis and analysis offer a greater understanding of area, latency, and power characteristics, the FPGA synthesis sheds light on resource utilization and functional behavior. This dual-flow technique guarantees that the design is both practically feasible for hardware realization and functionally correct.

4. Results

Both FPGA and ASIC design flows were used to assess the performance of the suggested Majority Logic Gate (MLG)-based MAC architectures. The analysis focuses on area, latency, and power for ASIC synthesis and resource utilization, timing, and power for FPGA implementation.

4.1 FPGA Results

Table -2: FPGA Performance Comparison of MLG-Based MAC Units

| Ref. No. | Unit Type | LUT | Delay (ns) | Power (W) |
|-----------|-----------|-----|------------|-----------|
| [2] | 4x4 | 33 | 14.838 | NG |
| [13] | 8x8 | 92 | 6.712 | 1.261 |
| This work | 4x4 | 26 | 2.431 | 0.114 |
| This work | 8x8 | 93 | 2.566 | 0.111 |

Table 2 displays the FPGA performance of the suggested MLG-based MAC devices. The 4x4 MAC uses 26 LUTs, but the 8x8 MAC needs 93 LUTs, demonstrating the anticipated rise in resource use with scaling.

The suggested design exhibits better timing performance since its delay is much lower than that of the reference designs. Both architectures exhibit efficient power behavior despite increased complexity, with power consumption remaining almost constant at 0.11 W.

Overall, the FPGA results show that the suggested architecture achieves constant power consumption, competitive resource usage, and improved delay performance.

4.2 ASIC Results

Table -3: ASIC Performance Comparison of MLG-Based MAC Units

| Ref. No. | Unit Type | Area (μm^2) | Delay (ns) | Power (μW) |
|-----------|-----------|--------------------------|------------|-------------------------|
| [1] | 8x8 | 3257.52 | 1.56 | 473 |
| This work | 4x4 | 997 | 3.35 | 107 |
| This work | 8x8 | 5762 | 6.5 | 365 |

Table 3 displays the ASIC performance of the suggested MLG-based MAC devices. The expansion of the

multiplier and reduction network causes the area to expand from $997 \mu\text{m}^2$ for the 4×4 MAC to $5762 \mu\text{m}^2$ for the 8×8 MAC.

As the design grows, the latency rises from 3.35 ns to 6.50 ns, representing the longer critical path. Due to increasing hardware complexity and switching activity, power consumption also increases from $107 \mu\text{W}$ to $365 \mu\text{W}$.

The suggested architecture operates in Sky130 (130 nm) technology and shows competitive power performance when compared to the reference design. Variations in technology node and design process have an impact on differences in delay and area.

Overall, the ASIC findings verify that the suggested design maintains a balanced trade-off between area, latency, and power while scaling predictably.

5. CONCLUSIONS





This effort involved the design, synthesis, and evaluation of 4×4 and 8×8 Majority Logic Gate (MLG)-based Multiply-Accumulate (MAC) units. While maintaining traditional logic for partial product creation to guarantee accuracy, the suggested architecture incorporates MLG in the arithmetic phase, specifically in full adders and the multiplier reduction path. Both FPGA and ASIC flows were used to validate the designs. While ASIC synthesis using Yosys with Sky130 libraries and analysis with OpenROAD permitted examination of area, delay, and power characteristics, FPGA synthesis using Xilinx Vivado verified correct functionality and offered insights into resource consumption, delay, and power. The results demonstrate that the proposed architecture scales effectively from 4×4 to 8×8 , with predictable increases in area, delay, and power. The use of MLG-based arithmetic contributes to efficient design with controlled power behavior.



Future work may focus on extending the design to higher bit-width MAC units, optimizing the architecture for advanced technology nodes, and exploring the use of MLG in approximate or low-power computing applications.

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