

HARMONIC MITIGATION-ORIENTED DESIGN OF A MODIFIED CASCADED MULTILEVEL INVERTER FOR MEDIUM-POWER INDUSTRIAL DRIVE SYSTEMS

Shruti Sagar Shukla¹, Dr. Imran Khan²

¹Master of Technology, Electrical Engineering (Power System), Azad Institute of Engineering and Technology, Lucknow, India

²Professor, Department Electrical Engineering (Power System), Azad Institute of Engineering and Technology, Lucknow, India

Abstract - The increasing adoption of power electronic converters in medium-power industrial drive systems has intensified concerns regarding power quality, particularly harmonic distortion. Conventional two-level inverters and standard cascaded multilevel inverters (CMLIs) often exhibit significant Total Harmonic Distortion (THD), increased switching losses, and higher system complexity due to the requirement of multiple switches and isolated DC sources. This paper presents a harmonic mitigation-oriented design of a modified cascaded multilevel inverter aimed at improving power quality while reducing hardware complexity. The proposed topology minimizes the number of switches and DC sources without compromising output voltage quality. A hybrid modulation strategy, combining Sinusoidal Pulse Width Modulation (SPWM) with optimized switching angle techniques, is implemented to achieve effective harmonic suppression. The system is modeled and analyzed using MATLAB/Simulink under typical industrial conditions (415 V, 50 Hz, 25 kW induction motor load). Performance evaluation is conducted using Fast Fourier Transform (FFT)-based harmonic analysis. Simulation results demonstrate that the proposed inverter achieves voltage THD in the range of 4–5%, complying with IEEE harmonic standards, while improving efficiency to approximately 91–95%. Additionally, switching losses are reduced by 15–25%, and torque ripple in the motor load is significantly minimized. The proposed design offers an optimal trade-off between harmonic performance, efficiency, and system complexity, making it suitable for practical industrial applications.

Key Words: Multilevel inverter; Cascaded H-bridge; Harmonic mitigation; Total Harmonic Distortion (THD); Industrial drive systems; Hybrid PWM; MATLAB/Simulink; Power quality

1. INTRODUCTION

The rapid evolution of industrial automation and electrification has significantly increased the reliance on power electronic converters for efficient energy conversion and motor control. In medium-power industrial drive systems, maintaining high power quality is essential to ensure reliable operation, minimize losses, and extend equipment lifespan. However, the integration of non-linear loads and switching devices introduces harmonic distortion, which degrades system performance and leads to issues

such as overheating, torque ripple, and reduced efficiency. Consequently, harmonic mitigation has become a critical research area in modern power electronics, particularly for industrial applications where continuous and stable operation is required.

1.1 Background

1.1.1 Growth of Industrial Automation and Power Quality Requirements

The increasing adoption of automation technologies in industries such as manufacturing, oil and gas, and process control has led to a substantial rise in the use of variable speed drives and power electronic converters. These systems demand high-quality electrical power with minimal distortion to ensure efficient and stable operation. Poor power quality, especially due to harmonics, can adversely affect sensitive equipment and reduce overall system efficiency. International standards such as IEEE 519 emphasize strict limits on harmonic distortion, highlighting the importance of advanced converter designs for industrial applications (Bollen, 2000).

1.1.2 Limitations of Conventional Two-Level Inverters

Conventional two-level inverters have been widely used due to their simple structure and ease of control. However, they generate output voltages with only two levels, resulting in square or quasi-square waveforms that contain significant harmonic components. This leads to high Total Harmonic Distortion (THD), increased electromagnetic interference (EMI), and higher switching losses. These drawbacks negatively impact motor performance by causing torque pulsations, increased heating, and reduced efficiency, making two-level inverters unsuitable for high-performance industrial applications (Rashid, 2014).

1.1.3 Emergence of Multilevel Inverter Technology

To overcome the limitations of conventional inverters, multilevel inverter (MLI) technology has emerged as an effective solution for improving power quality. MLIs generate output voltages with multiple discrete levels, producing waveforms that closely approximate a sinusoidal shape. This significantly reduces harmonic distortion and switching losses while improving efficiency and reliability.

Among various MLI topologies, cascaded H-bridge (CHB) inverters are particularly attractive due to their modular structure, scalability, and suitability for medium-voltage industrial applications (Rodríguez et al., 2002).

1.2 Problem Statement

Despite the advantages of multilevel inverter technology, achieving an optimal balance between harmonic reduction and system complexity remains a significant challenge in practical applications. While increasing the number of voltage levels can effectively reduce harmonic distortion, it also leads to increased hardware requirements and control complexity. This trade-off limits the widespread adoption of advanced inverter topologies in industrial environments.

1.2.1 Trade-off Between Harmonic Reduction and System Complexity

Reducing harmonic distortion typically requires increasing the number of switching devices and implementing advanced modulation techniques. However, this increases circuit complexity, cost, and computational burden. Industrial systems require solutions that not only achieve low THD but also remain cost-effective and easy to implement. Therefore, designing an inverter that balances performance with simplicity is a key challenge in power electronics research (Kouro et al., 2010).

1.2.2 Limitations of Conventional Cascaded Multilevel Inverter (CMLI)

Although the Cascaded Multilevel Inverter offers improved harmonic performance compared to traditional inverters, it has several practical limitations. One major issue is the high switch count, which increases system cost, switching losses, and hardware complexity. Additionally, conventional CMLIs require multiple isolated DC sources for each H-bridge cell, which is often impractical in industrial settings. Furthermore, the control strategies required to manage switching operations and maintain voltage balance are complex and computationally intensive, making real-time implementation challenging (Malinowski et al., 2010).

1.3 Research Gap

Despite extensive research in multilevel inverter technologies, several important gaps remain unaddressed, particularly in the context of medium-power industrial drive systems.

1.3.1 Lack of Simultaneous Achievement of Low THD and Reduced Hardware

Most existing inverter designs focus either on reducing harmonic distortion or minimizing hardware components, but rarely achieve both simultaneously. Advanced techniques such as Selective Harmonic Elimination (SHE) can achieve low THD but require complex computations,

while simpler designs often compromise on harmonic performance. This creates a need for optimized inverter topologies that can deliver low THD without increasing system complexity (Patel and Hoft, 1973).

1.3.2 Limited Practical Industrial-Oriented Designs

Many research studies are primarily simulation-based and do not consider real-world industrial constraints such as cost, reliability, and ease of implementation. As a result, there is a gap between theoretical developments and practical industrial applications. Designing inverter systems that are both high-performing and industrially feasible remains a key challenge.

1.3.3 Lack of Balanced Modulation Techniques

Existing modulation strategies often involve a trade-off between harmonic performance and computational complexity. While advanced methods such as artificial intelligence-based control provide excellent harmonic reduction, they are difficult to implement in real-time systems. Conversely, simpler techniques like SPWM are easy to implement but offer moderate harmonic performance. Therefore, there is a need for balanced modulation techniques that provide effective harmonic mitigation with manageable computational requirements (Holmes and Lipo, 2003).

2. LITERATURE REVIEW

The literature on multilevel inverters (MLIs) highlights significant advancements in power electronic converter design aimed at improving power quality, efficiency, and reliability in industrial applications. Various inverter topologies, modulation strategies, and optimization techniques have been proposed to reduce harmonic distortion and enhance system performance. However, practical challenges such as system complexity and real-time implementation constraints continue to limit their widespread industrial adoption.

2.1 Overview of Multilevel Inverters

Multilevel inverters are widely recognized for their ability to generate high-quality output voltage waveforms with reduced harmonic distortion compared to conventional two-level inverters. By synthesizing output voltages from multiple discrete levels, MLIs produce a staircase waveform that closely approximates a sinusoidal signal, thereby improving power quality and reducing filtering requirements.

2.1.1 NPC, FC, and CHB Topologies

The three classical multilevel inverter topologies are Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB). The NPC inverter uses clamping diodes to divide the DC bus voltage into multiple levels, offering good

efficiency but facing challenges in voltage balancing. The FC inverter employs capacitors to generate voltage levels and provides redundancy, although it requires complex control for capacitor voltage balancing. The CHB inverter consists of series-connected H-bridge cells powered by separate DC sources, making it highly modular and scalable for medium- and high-power applications (Rodríguez et al., 2002).

2.1.2 Comparative Advantages

Each topology offers distinct advantages depending on the application. NPC inverters are suitable for medium-voltage drives due to their relatively simple structure, while FC inverters provide better fault tolerance. However, CHB inverters stand out due to their modularity, scalability, and superior harmonic performance. They also impose lower voltage stress on switching devices, making them particularly attractive for industrial drive systems (Franquelo et al., 2008).

2.2 Cascaded Multilevel Inverter (CMLI)

The Cascaded Multilevel Inverter has gained significant attention due to its flexibility and suitability for industrial applications. It is considered one of the most practical multilevel inverter topologies for medium-power drive systems.

2.2.1 Structure and Working Principle

The CMLI is composed of multiple H-bridge cells connected in series, each supplied by an independent DC source. By controlling the switching states of each H-bridge, the inverter generates multiple voltage levels at the output. The number of levels is determined by the number of cascaded cells, typically expressed as $(2n + 1)$ for n cells per phase. The output voltage is synthesized by summing the individual voltages of each cell, resulting in a stepped waveform that approximates a sinusoidal signal (Malinowski et al., 2010).

2.2.2 Benefits in Industrial Drives

CMLIs offer several advantages in industrial drive applications, including reduced harmonic distortion, improved efficiency, and modular design. The modular structure allows easy expansion and maintenance, while the improved waveform quality leads to smoother motor operation with reduced torque ripple and lower losses. These features make CMLIs highly suitable for medium-voltage industrial drives such as pumps, compressors, and conveyor systems (Wu, 2006).

2.3 Harmonic Distortion in MLIs

Although multilevel inverters significantly reduce harmonic distortion compared to conventional inverters, harmonics remain a critical issue due to switching operations and non-linear load behavior.

2.3.1 Sources and Impact of Harmonics

Harmonics in MLIs primarily arise from high-frequency switching actions and the interaction with non-linear loads such as induction motors and variable frequency drives. These harmonics distort the voltage and current waveforms, leading to increased losses, overheating, electromagnetic interference, and reduced equipment lifespan. In motor-driven systems, harmonics can cause torque pulsations, vibration, and noise, affecting overall system performance (Bollen, 2000).

2.3.2 Reported THD Values in Literature

Various studies have reported Total Harmonic Distortion (THD) values for multilevel inverter systems. Conventional cascaded H-bridge inverters typically exhibit THD levels in the range of 10–12% under simulation conditions, while practical implementations may experience higher values, reaching up to 20–25% due to non-ideal switching and system losses. These findings indicate the need for improved control strategies to achieve acceptable harmonic limits in industrial applications (Kouro et al., 2010).

2.4 Modulation Techniques

Modulation techniques play a crucial role in determining the switching behavior of multilevel inverters and directly influence harmonic performance, efficiency, and system complexity.

2.4.1 Sinusoidal Pulse Width Modulation (SPWM)

SPWM is one of the most commonly used modulation techniques due to its simplicity and ease of implementation. It involves comparing a sinusoidal reference signal with a high-frequency carrier waveform to generate switching pulses. While SPWM improves waveform quality compared to square-wave operation, it typically results in moderate THD levels and is less effective for high-performance applications (Holmes and Lipo, 2003).

2.4.2 Selective Harmonic Elimination (SHE)

Selective Harmonic Elimination is an advanced technique that eliminates specific lower-order harmonics by calculating optimal switching angles. SHE can achieve very low THD values; however, it requires solving complex nonlinear equations, making it computationally intensive and challenging for real-time implementation (Patel and Hoft, 1973).

2.4.3 Space Vector Modulation (SVM)

Space Vector Modulation is a sophisticated technique that represents inverter switching states as vectors in a two-dimensional plane. SVM offers better DC bus utilization and improved harmonic performance compared to SPWM. However, it involves complex mathematical computations,

which increase implementation complexity (Holmes and Lipo, 2003).

3. PROPOSED MODIFIED CMLI TOPOLOGY

This section presents the design and operational framework of the proposed modified Cascaded Multilevel Inverter (CMLI), developed to address the limitations of conventional inverter configurations. The proposed topology focuses on achieving superior harmonic performance while simultaneously reducing hardware complexity and improving efficiency. By integrating structural optimization with an effective control strategy, the design ensures practical applicability in medium-power industrial drive systems.

3.1 Design Objectives

The primary objective of the proposed modified CMLI is to achieve an optimal balance between power quality, efficiency, and system simplicity. In industrial applications, these parameters are critical for ensuring reliable and cost-effective operation.

3.1.1 Reduction of Total Harmonic Distortion (THD < 5%)

A key design goal is to limit the Total Harmonic Distortion (THD) of the output voltage to less than 5%, in compliance with standard power quality requirements. This is achieved by increasing the effective number of voltage levels and implementing optimized switching strategies. Lower THD ensures improved waveform quality, reduced motor losses, and enhanced overall system performance.

3.1.2 Reduction in Switch Count

Another important objective is to minimize the number of switching devices required in the inverter. Conventional CMLIs require a large number of switches as the number of levels increases, which leads to higher cost and complexity. The proposed design aims to reduce the switch count without compromising the number of output voltage levels, thereby simplifying the circuit and reducing switching losses.

3.1.3 Improvement in Efficiency (>90%)

The proposed inverter is designed to achieve an efficiency greater than 90%, which is essential for medium-power industrial applications. Efficiency improvement is primarily achieved by reducing switching losses and optimizing the conduction paths within the inverter. This ensures lower energy loss and improved thermal performance.

3.2 Conventional vs Proposed Topology

The proposed modified CMLI is developed by improving upon the conventional cascaded H-bridge structure,

addressing its key limitations related to hardware complexity and cost.

3.2.1 Structural Comparison

In a conventional CMLI, each H-bridge cell requires four switches and an independent DC source. As the number of levels increases, the number of switches and DC sources increases proportionally, resulting in a bulky and complex system. In contrast, the proposed topology modifies the arrangement of switching devices and voltage sources to achieve the same or higher number of voltage levels with fewer components.

3.2.2 Hardware Reduction Strategy

The hardware reduction strategy involves optimizing the configuration of H-bridge units and utilizing shared or reduced DC sources. By intelligently designing the switching network, the inverter can generate multiple voltage levels using fewer switches and sources. This approach reduces the overall component count by approximately 20–30%, leading to lower cost, simplified design, and improved reliability.

3.3 Circuit Configuration

The circuit configuration of the proposed modified CMLI is designed to maintain modularity while reducing complexity. It retains the fundamental advantages of cascaded structures while introducing improvements in component utilization.

3.3.1 Modified H-Bridge Arrangement

In the proposed design, the traditional H-bridge structure is modified to reduce redundant switching devices. This is achieved by reconfiguring the switching paths and utilizing certain switches more efficiently. The modified arrangement allows multiple voltage levels to be generated with fewer switching components, maintaining the desired output waveform quality.

3.3.2 DC Source Optimization

The proposed topology also reduces the number of required DC sources by employing optimized voltage sharing techniques. Instead of using separate isolated DC sources for each H-bridge cell, the design utilizes fewer sources while still achieving multiple voltage levels. This significantly improves the practicality of the inverter in industrial environments where multiple isolated sources are difficult to implement.

3.4 Operating Principle

The operation of the proposed modified CMLI is based on controlled switching of power electronic devices to synthesize a multilevel output voltage waveform.

3.4.1 Switching States

Each switching device in the inverter operates according to predefined switching states, which determine the output voltage level at any given instant. By carefully selecting the switching combinations, the inverter produces discrete voltage levels that collectively form a staircase waveform. The switching strategy is designed to minimize harmonic distortion and ensure balanced operation across all phases.

3.4.2 Voltage Level Generation

The output voltage is generated by combining the contributions of individual inverter units. Each unit produces a specific voltage level, and the series combination results in a multilevel output waveform. The increased number of levels improves the approximation of a sinusoidal waveform, thereby reducing harmonic distortion and enhancing power quality.

4. MODULATION STRATEGY

Modulation strategy is a decisive factor in multilevel inverter performance because it directly governs switching instants, harmonic spectrum, switching losses, and DC-link utilization. In medium-power industrial drives, the control scheme must deliver low Total Harmonic Distortion (THD) while remaining implementable on real-time controllers. This section outlines the baseline approach, an advanced harmonic-targeting method, and a proposed hybrid strategy that balances performance and computational burden.

4.1 SPWM (Baseline Method)

4.1.1 Working Principle

Sinusoidal Pulse Width Modulation (SPWM) generates gating signals by comparing a sinusoidal reference (fundamental frequency) with one or more high-frequency triangular carrier waves. For multilevel inverters, level-shifted or phase-shifted carrier arrangements are used to produce multiple voltage levels. The intersection points between the reference and carriers determine switching instants, yielding a stepped output that approximates a sinusoid. The method offers straightforward digital implementation, stable operation over a wide modulation index, and predictable switching frequency.

4.1.2 Limitations

Despite its simplicity, SPWM provides only moderate harmonic performance in multilevel configurations, typically leaving residual lower-order harmonics and yielding THD above stringent industrial limits in some cases. It also requires higher switching frequencies to improve waveform quality, which increases switching losses and thermal stress. Furthermore, SPWM does not explicitly eliminate specific harmonics, limiting its effectiveness for compliance with tight standards.

4.2 Selective Harmonic Elimination (SHE)

4.2.1 Harmonic Targeting Approach

Selective Harmonic Elimination (SHE) determines a set of optimal switching angles such that chosen lower-order harmonics (e.g., 5th, 7th) are mathematically canceled while maintaining the desired fundamental component. This is achieved by solving nonlinear transcendental equations derived from Fourier series expansion of the output waveform. When properly configured, SHE can achieve very low THD with excellent control over the harmonic spectrum.

4.2.2 Complexity Issues

The primary drawback of SHE is its computational intensity. The number and nonlinearity of equations increase with the number of voltage levels, leading to multiple valid solutions and sensitivity to modulation index. Real-time implementation is challenging due to the need for iterative solvers or large precomputed lookup tables. Additionally, dynamic operating conditions (load or voltage variations) complicate angle selection, reducing practicality for fast-changing industrial drives.

4.3 Proposed Hybrid Modulation Technique

4.3.1 Combination of SPWM and Optimized Switching

The proposed hybrid strategy integrates SPWM's simplicity with targeted harmonic suppression via optimized switching angles. SPWM provides the base gating pattern and ensures stable operation, while a supervisory optimization layer perturbs selected switching instants (or injects angle corrections) to attenuate dominant harmonics. This retains fixed switching frequency characteristics while improving spectral quality.

5. RESULTS AND DISCUSSION

This section presents a comprehensive evaluation of the proposed modified Cascaded Multilevel Inverter (CMLI) based on simulation results. The performance is analyzed in terms of waveform quality, harmonic distortion, efficiency, switching losses, voltage stress, and load behavior. A comparative study with the conventional CMLI highlights the improvements achieved through the proposed design and hybrid modulation strategy.

5.1 Output Voltage Waveform Analysis

5.1.1 Conventional vs Proposed Waveform

The output voltage waveform is a primary indicator of inverter performance. In the conventional CMLI, the waveform exhibits a staircase profile with relatively fewer voltage levels, resulting in noticeable deviations from an ideal sinusoidal shape. These deviations introduce higher harmonic content and increase distortion in the system.

In contrast, the proposed modified CMLI produces a more refined staircase waveform with increased effective voltage levels. The transitions between voltage steps are smoother, and the waveform closely approximates a sinusoidal signal. This improvement directly contributes to enhanced power quality and reduced harmonic distortion, making the proposed inverter more suitable for industrial applications.

5.2 Harmonic Analysis (FFT Results)

5.2.1 THD Comparison

Harmonic analysis using Fast Fourier Transform (FFT) provides a quantitative assessment of waveform quality. The conventional CMLI exhibits Total Harmonic Distortion (THD) in the range of 8–11%, which exceeds recommended limits for high-performance industrial systems. The presence of dominant lower-order harmonics such as the 5th and 7th significantly affects system efficiency and load performance.

The proposed modified CMLI achieves a substantial reduction in harmonic distortion, with THD values in the range of 4–5%. This improvement is attributed to the increased number of voltage levels and the implementation of the hybrid modulation strategy. The results confirm compliance with standard harmonic limits and demonstrate the effectiveness of the proposed design in mitigating harmonics.

5.3 Modulation Technique Comparison

5.3.1 SPWM vs SHE vs Hybrid

The performance of different modulation techniques is compared to evaluate their effectiveness in harmonic reduction. SPWM, while simple and easy to implement, produces moderate THD levels (typically above 6%), making it less suitable for applications requiring strict power quality standards.

Selective Harmonic Elimination (SHE) offers superior harmonic suppression by eliminating specific lower-order harmonics, achieving THD values close to 3–5%. However, its high computational complexity limits its practical implementation in real-time systems.

The proposed hybrid modulation technique provides an optimal balance between these two methods. It achieves THD levels comparable to SHE (around 4–5%) while maintaining moderate computational complexity similar to SPWM. This makes it a practical and efficient solution for industrial inverter applications.

5.4 Efficiency Analysis

5.4.1 Efficiency Improvement

Efficiency is a critical performance parameter in industrial power systems. The conventional CMLI demonstrates

efficiency in the range of approximately 86–90%, primarily affected by switching losses and harmonic-related losses.

The proposed modified CMLI achieves improved efficiency in the range of 91–95%. This enhancement is mainly due to reduced switching losses, optimized modulation strategy, and lower harmonic distortion. Improved efficiency results in reduced energy consumption, lower thermal stress, and improved overall system performance.

5.5 Switching Loss Analysis

5.5.1 Reduction Due to Fewer Switches

Switching losses are significantly influenced by the number of switching devices and their operating frequency. In the conventional CMLI, a higher number of switches leads to increased switching events and consequently higher losses.

The proposed topology reduces the number of switches by approximately 20–30%, resulting in fewer switching transitions. This reduction directly decreases switching losses by about 15–25%. Lower switching losses improve system efficiency and reduce heat generation, thereby enhancing the reliability and lifespan of the inverter components.

5.6 Voltage Stress Analysis

5.6.1 Improved Device Reliability

Voltage stress across switching devices is an important factor affecting inverter reliability. In conventional inverter designs, higher voltage stress can lead to device degradation and failure over time.

The proposed modified CMLI distributes the total voltage across multiple levels, reducing the stress experienced by individual switches. This balanced voltage distribution improves device reliability and reduces the likelihood of failure. Consequently, the inverter system becomes more robust and suitable for continuous industrial operation.

5.7 Industrial Load Performance

5.7.1 Induction Motor Results

The performance of the inverter is further evaluated using an induction motor load, which represents a typical industrial application. In the case of the conventional CMLI, higher harmonic distortion results in torque ripple, speed fluctuations, and increased losses in the motor.

With the proposed modified CMLI, the improved output waveform significantly enhances motor performance. Torque ripple is reduced by approximately 30–40%, resulting in smoother mechanical operation. Additionally, speed stability is improved due to the reduction in harmonic components in the supply voltage. These improvements lead

to reduced vibration, lower noise levels, and increased efficiency of the motor system.

Overall, the results demonstrate that the proposed inverter not only improves electrical performance but also enhances the operational characteristics of industrial loads, making it a highly effective solution for medium-power drive applications.

6. CONCLUSION

This research presented a harmonic mitigation-oriented design of a modified Cascaded Multilevel Inverter (CMLI) for medium-power industrial drive systems, addressing the critical challenge of achieving low Total Harmonic Distortion (THD) while minimizing system complexity. The proposed topology successfully reduces the number of switches and DC sources through structural optimization, thereby lowering hardware requirements and switching losses. A hybrid modulation strategy, combining Sinusoidal Pulse Width Modulation (SPWM) with optimized switching control, was implemented to enhance harmonic performance without introducing excessive computational burden.

Simulation results obtained using MATLAB/Simulink demonstrate that the proposed inverter achieves a voltage THD in the range of 4–5%, which satisfies standard power quality requirements. This represents a significant improvement over the conventional CMLI, which exhibits THD values of approximately 8–11%. Additionally, the efficiency of the system is improved to 91–95%, attributed to reduced switching and harmonic losses. The reduction in switch count also contributes to a decrease in switching losses by approximately 15–25%, improving thermal performance and system reliability.

Furthermore, the proposed inverter shows improved voltage stress distribution across switching devices, enhancing durability and operational stability. When tested with an induction motor load, the system demonstrates reduced torque ripple and improved speed stability, confirming its suitability for industrial applications. Overall, the research validates that the proposed modified CMLI offers an effective balance between performance, efficiency, and practical implementation.

6.1. Future Scope of Research

Future work can focus on the development of a hardware prototype to experimentally validate the simulation results under real operating conditions. Implementation of the proposed hybrid modulation strategy using real-time controllers such as DSP or FPGA can further establish its practical feasibility. Additionally, advanced control techniques incorporating artificial intelligence or adaptive algorithms may be explored to enhance dynamic performance under varying load conditions. Integration of DC-link voltage balancing mechanisms and investigation

under transient and fault conditions can further improve system reliability and industrial applicability.

REFERENCES

1. Bollen, M.H.J., 2000. *Understanding Power Quality Problems: Voltage Sags and Interruptions*. New York: IEEE Press.
2. Franquelo, L.G., Rodríguez, J., Leon, J.I., Kouro, S., Portillo, R. and Prats, M.A.M., 2008. The age of multilevel converters arrives. *IEEE Industrial Electronics Magazine*, 2(2), pp.28–39.
3. Haykin, S., 2009. *Neural Networks and Learning Machines*. 3rd ed. New Delhi: Pearson Education.
4. Holmes, D.G. and Lipo, T.A., 2003. *Pulse Width Modulation for Power Converters: Principles and Practice*. Hoboken: Wiley-IEEE Press.
5. Holland, J.H., 1992. *Adaptation in Natural and Artificial Systems*. Cambridge: MIT Press.
6. Kennedy, J. and Eberhart, R., 1995. Particle swarm optimization. In: *Proceedings of IEEE International Conference on Neural Networks*. Perth, Australia, pp.1942–1948.
7. Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L.G., Wu, B., Rodríguez, J., Pérez, M.A. and Leon, J.I., 2010. Recent advances and industrial applications of multilevel converters. *IEEE Transactions on Industrial Electronics*, 57(8), pp.2553–2580.
8. Malinowski, M., Gopakumar, K., Rodríguez, J. and Pérez, M.A., 2010. A survey on cascaded multilevel inverters. *IEEE Transactions on Industrial Electronics*, 57(7), pp.2197–2206.
9. Patel, H. and Hoft, R.G., 1973. Generalized techniques of harmonic elimination and voltage control in thyristor inverters. *IEEE Transactions on Industry Applications*, IA-9(3), pp.310–317.
10. Rashid, M.H., 2014. *Power Electronics: Circuits, Devices and Applications*. 4th ed. New Delhi: Pearson Education.
11. Rodríguez, J., Lai, J.S. and Peng, F.Z., 2002. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Transactions on Industrial Electronics*, 49(4), pp.724–738.
12. Wu, B., 2006. *High-Power Converters and AC Drives*. Hoboken: Wiley-IEEE Press.
13. Tennyson, D.I., Jibia, A.U., Shanono, I.H. and Kadandani, N.B., 2025. Harmonic mitigation for symmetrical cascaded H-bridge inverter using sparrow search

- algorithm. *Journal of Electrical Systems and Information Technology*.
14. Bile, B.M., 2025. A new multilevel inverter topology for harmonic elimination using pulse width and height modulation. *Results in Engineering*.
 15. Taha, T.A., 2025. Recent advancements in multilevel inverter topologies and control techniques. *Symmetry*, 17(7), p.1010.
 16. Bhatt, K. and Chakravorty, S., 2020. Mitigation of harmonics from cascaded H-bridge multilevel inverter using SHE PWM and AI techniques. *Recent Advances in Electrical and Electronic Engineering*, 13(7), pp.952–968.
 17. Chitrakala, G., Stalin, N. and Mohan, V., 2020. Reduced distortion cascaded multilevel inverter using optimization techniques. *Journal of Circuits, Systems and Computers*, 29(2).
 18. Janardhan, K., Mittal, A. and Ojha, A., 2020. Multilevel inverter topology with minimal switch count and THD. *Journal of Circuits, Systems and Computers*, 29(11).
 19. Panda, K.P., Bana, P.R. and Panda, G., 2020. Selective harmonic elimination in reduced switch multilevel inverter. *IEEE Transactions on Industry Applications*, 56(3), pp.2862–2870.
 20. Routray, A., Singh, R.K. and Mahanty, R., 2020. Harmonic reduction using grey wolf optimization in cascaded inverter. *IEEE Transactions on Industry Applications*, 56(2).
 21. Memon, M.A., Mekhilef, S. and Mubin, M., 2018. Hybrid PSO-based harmonic elimination in multilevel inverter. *IET Power Electronics*, 11(10), pp.1673–1680.
 22. Kumar Dash, S., Nayak, B. and Sahu, J.B., 2018. Whale optimization-based harmonic elimination in multilevel inverter. *International Journal of Power Electronics and Drive Systems*, 9(4), pp.1944–1951.
 23. Mahesh, A. and Sandhu, K.S., 2018. Evolutionary algorithm-based optimal switching angles for CHB inverter. *Procedia Computer Science*, 125, pp.412–419.
 24. Mahesh, A. and Sandhu, K.S., 2019. Pigeon-inspired optimization for harmonic reduction in multilevel inverter. *International Journal of Emerging Electric Power Systems*, 20(2).
 25. Krithiga, G. and Mohan, V., 2022. Marine predator algorithm-based harmonic reduction in multilevel inverter. *International Transactions on Electrical Energy Systems*, 2022.
 26. Mousavi, S.Y.M. et al., 2018. Artificial bee colony algorithm for selective harmonic elimination. *International Transactions on Electrical Energy Systems*, 28(4).
 27. Konstantinou, G.S., Ciobotaru, M. and Agelidis, V.G., 2013. Selective harmonic elimination PWM for modular multilevel converters. *IET Power Electronics*, 6(1), pp.96–107.
 28. Pourdadashnia, A., Sadoughi, M., Farhadi-Kangarlu, M. and Tousi, B., 2021. Selective harmonic elimination in cascaded multilevel inverter using PSO. *IEEE/ArXiv preprint*.
 29. Sadoughi, M. et al., 2021. Harmonic reduction in CHB inverter using optimized DC-link control. *IEEE/ArXiv preprint*.
 30. Mathews, M., Ramesh, B. and Sreedhar, T., 2022. Neural network-based THD minimization in multilevel inverter. *IEEE/ArXiv preprint*.
 31. Hashemi-Zadeh, A. et al., 2025. AI-driven optimization of PWM in cascaded converters. *IEEE/ArXiv preprint*.
 32. Pathak, V., 2025. Reduced device count asymmetrical multilevel inverter topology. *Progress In Electromagnetics Research*.
 33. Vanajakshi, N. et al., 2023. Fuzzy logic-based harmonic mitigation in cascaded multilevel inverter. *International Journal of Power Electronics*.
 34. Khamooshi, R. and Moghani, J.S., 2014. Harmonic optimization in cascaded H-bridge inverter using variable DC sources. *IEEE PEDSTC Conference*.
 35. Chatterjee, A. et al., 2017. Genetic algorithm-based harmonic elimination in multilevel inverter. *IEEE Conference on Power Electronics*.
 36. Ganesan, K. et al., 2015. BAT algorithm-based harmonic elimination in cascaded inverter. *Procedia Technology*, 21, pp.651–657.
 37. Debnath, R., 2012. Cuckoo search algorithm for harmonic elimination in multilevel inverter. *Journal of Bioinformatics and Intelligent Control*.