POWER OPTIMIZATION USING BODY BIASING METHOD FOR DUAL VOLTAGE FPGA

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Abstract - *Dual supply voltage is a mature low power technique that has already been widely used in application-specific integrated circuit (ASIC). It has also been introduced into field programmable gate array (FPGA) where non-critical blocks are configured to work at unsettled low voltage level, so as to reduce dynamic power. These supply voltage optimizations decreases the computation time, delay and power.In existing method a model design of Dual Voltage Supply for FPGA blocks to reduce the dynamic power in FPGA's. The particular model is designed to work in Vdd1 and others in Vdd2. The proposed system will be developed by using Dual Mode Logic Switches and Body Biasing method to reduce the power reduction ratio.The design can be simulated using back end low power tools available in Tanner EDA .*

Key Words: Dual voltage, field-programmable gate array (FPGA), path delay distribution (PDD), variable supply voltage.

1. INTRODUCTION

In recent FPGAs, power consumption has become a very important design consideration. Due to the large number of transistors required for field programmability and the low utilization rate of FPGA resources, existing FPGAs consume more power compared to ASICs [1]. As the process technology advances to nanometer technology and low-energy embedded applications are explored for FPGAs, power consumption becomes a crucial design constraint for FPGAs. Several recent papers have studied FPGA power modeling and optimization. [2]– [4] presented power evaluation frameworks for generic parameterized FPGA architectures and showed that both interconnect and leakage power are significant for FPGAs in nanometer technologies.

Dual voltage design is a mature low power technique that has already been wide employed in application-specific integrated circuit (ASIC). It has also been introduced into field-programmable gate array (FPGA) by [1], where noncritical blocks are configured to work at V_L (lower voltage level) so as to reduce dynamic power consumption. Three Vdd states for interconnect switches are known to be high Vdd, low Vdd and power-gating. Previous works show that over half of the total power consumption of FPGA can be reduced due to the dual-V_{DD} technique [1].In dual voltage design, the V_H (higher V_{DD}) is usually selected according to the technology node while the V_L could be adjusted. For ASIC, the V_L can be optimized according to a specific circuit. There are lots of research on the architecture of dual-V_{DD} FPGA and its V_{DD} assignment algorithms, but the methods to find the optimum voltages are much less. However recent gate-level algorithms gave a different conclusion that is value actually fluctuates in a wider range with specific circuits [6]–[8], so applications should be considered for power optimization in the design of a dual voltage FPGA.

This paper presents an circuit level modeling with dual mode logic switches and body biasing method to estimate the optimum ratio of VL/VH quickly. It mainly utilizes the path delay distributions (PDDs) of applications and also the delay function (delay as a function of supply voltage) of circuit technology to calculate the optimum VL/VH. The improved versions count minor factors (including transition density, capacitance, and path overlap) for a more accurate estimation. In the proposed method, the proportion of the gates and wires that work at VL is deduced from the power model, which can be obtained faster, quicker, therefore the computation time is greatly reduced.

2. PROPOSED METHOD OF DUAL VOLTAGE DESIGN

2.1. Basic Model

The basic model is constructed under transition density and path overlap.

1) Transition Density and Capacitance: Transition density is assumed to influences on their optimum V_L/V_H ratio are counted by using a modified PDD as shown in (1), where the transition density and capacitance are introduced because the weight of cell delays . The power optimal V_L/V_H ratio can be

easily found when $p(t)$, S, V_T, and V_H are provided. The $p(t)$ is the key factors its accuracy affects the result. The $p(t)$ was assumed to be linear in [5], then the optimal ratio was believed to fall merely between 0.6 and 0.7. However, practical $p(t)$ is not linear but similar to a Gaussian distribution [10], resulting a wider range.In general, when the mean of a PDD decreases, its optimum V_L/V_H will decrease and its overall power reduction ratio will increase[1].

$$\int_0^a p'(t) \cdot t \cdot dt = \frac{\sum_i C_i \cdot D_i \cdot t_i}{N C_{\mathrm{ave}} D_{\mathrm{ave}}} (t_i \in \mathrm{Path}|_{0 \le t \le a}). \quad (1)$$

All the parameters are explained as follows:
a a value of path delay;
I the cells on the paths whose delay is smaller than a;
C_i capacitance/delay of Cell i;
D_i transition density of Cell i;
C_{ave} average capacitance/delay;
D_{ave} average transition density;
N total number of paths;
$p^0(t)$ the equivalent PDD.

It means that the $p(t)$ should be modified and replaced by a $p^0(t)$, where cells are weighted by their importance to the power consumption.

2) Path Overlap: Path overlap refers to that some cells will be passed by more than one path. As a result, they are counted more than once in the PDD. As shown in Fig. 1, the overlap between long paths and short paths might force some V_L cells of the short paths to work at V_H because they are also restricted by the long paths. So, path overlap could reduce power reduction ratio. This impact is modeled as where the r of *Group A* is multiplied by $O(V_L)$ (<1) and the r of *Group B* is multiplied by $P(V_L)$ (<1). The coefficients are also related to the V_L level.

$$r(V_L, t) = \begin{cases} \frac{1-t}{t \cdot (S-1)} \cdot P(V_L), & t \ge \frac{1}{S} \text{(Group B)} \\ O(V_L), & t < \frac{1}{S} \text{(Group A)} \end{cases} \quad (2)$$

It is difficult to figure out an accurate relationship because it differs from one implementation to another. So, they are taken to be constant (first approximation) in this paper just for rough estimation of the path overlap's impact. So, when the path overlap is counted to improve model accuracy we get (2).

2.2. Improved Models

Body biasing technique works well to reduce channel

sub threshold leakage, but does not do much for gate leakage and actually exacerbates junction leakage. It has little effect on dynamic power.

Dual voltage FPGA was designed with the dual body biasing circuit. The dual mode provides regulated power supply to the design. Analyze the condition of circuit is in active or standby mode, if it is in standby mode biasing totally reduce the leaking current in FPGA. By selecting the proper biasing conditions, those maintained despite variations in ambient temperature, which cause changes in amplification and even distortion occurs in the circuit.
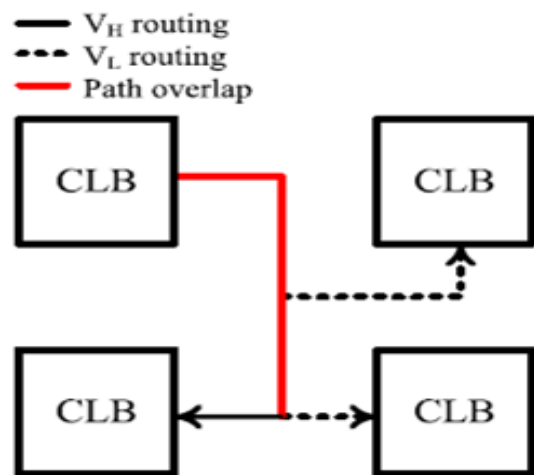

Fig.1.Path overlapping reduces the amount of V_L cells (Section III for the explanation of CLB).

Body biasing provides the optimum power and regulate the function of the circuit. By using the dual voltage body biasing effect there the circuit is maintained in both active and sleeping mode. Fig. 2 shows that flow of body biasing method.

The Optimization Method for Dual Voltage FPGA by using the body bias effects is used to eliminate the leakage power dissipation of the circuit. For the body bias effects connect the parallel PMOS and NMOS in the header and footer of the circuit which make the circuit as low power consumption circuit. When the circuit is operate at that point parallel CMOS circuit allow the power supply to the circuit due to this reason the gate power dissipation such as leakage , short circuit and dynamic power dissipation is reduced.
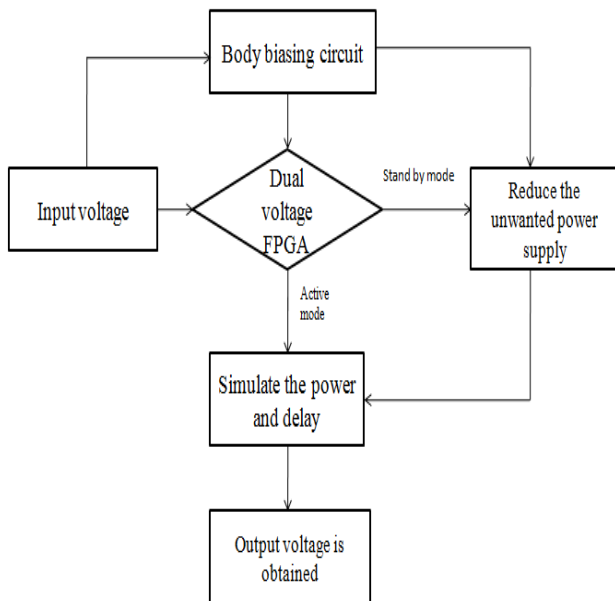
Fig. 2.Flow of Body Biasing Method

Whenever the input is enable the PMOS is enable it allow the flow to the voltage supply to the circuit otherwise it is not allow the supply voltage to the circuit. The parallel of PMOS which is connect with the circuit is used to avoid the negative feedback of the circuit which make the circuit as the high performance circuit. The S is related to the CMOS technology and can be obtained from SPICE simulation. To increase further more accuracy the improved models can obviously help. However, more computation time is also required.
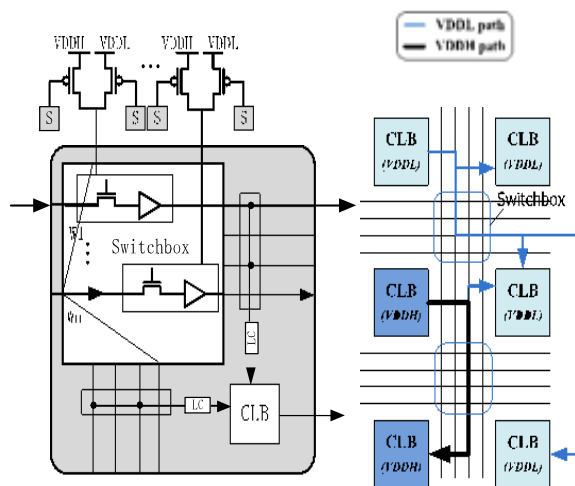

Fig.3. Routing-tree-level programmable granularity: (a) the architecture and (b) a mapping instance.

3. EXPERIMENT SETUP

3.1. Modeling of Dual-V_{DD} FPGA Architecture

Dual-VDD architecture is built on cluster-based island-style FPGA architecture, with the configuration stored in SRAM cells. It facilitates configurable supply voltage for logic blocks and routing multiplexers. A implied academic model of cluster-based island-style FPGA architecture is studied in this paper. Single-driver switchbox is used as [12], where each routing track has only one physical driver with a multiplexer on its input. The basic logic element (BLE) consists of a 4-input LUT and a flip-flop. Eight such BLEs cluster together to form a cluster logic block (CLB). The dual-V_{DD} technique is implemented through design V_{DD}-programmable interconnect and logic block [4].

The V_{DD}-programmable granularity means the minimal unit whose supply voltage must be configured as a whole. Every granularity is power gated by two parallel PMOS transistors that connect to different supply voltages. The transistors are controlled by two-bit SRAM. Level convertors (LCs) are used to avoid leakage power when V_L blocks drive V_H blocks. In this paper, a CLB is the granularity of logic resources as previous papers. Considering the path overlap, a routing-tree-based interconnect granularity [4] is adopted as shown in Fig. 3, where routing path between two CLBs is the minimal assignment unit. Because LCs only exist on the CLB input, the routing tree driven by a V_L CLB has to use V_L. Other routing trees can use either V_L or V_H depending on the assignment algorithm.

3.2. Dual Voltage Assignment on Gate Level

In order to be effective, a dual VDD scheme requires that paths in the circuit vary in their delays. If all paths are of same delay then all circuit elements will require high VDD to maintain the performance of the design. It is evident from the figure that path delays in a circuit vary considerably. Therefore, a dual-VDD scheme can be expected to reduce the power consumption significantly.

The optimal assignment is known to be NP-hard, so greedy and heuristic algorithms are adopted as approximate solutions [2]. The supply voltages of CLBs are selected according to the defined criticality. The method of [7] assigns V_L to the cells that have larger▲power × slack/▲delay. The work in [6] priorly exploits the cells that have minimum impact on the other slacks. In this paper, the criticality is defined as the number of sensitive paths passing through a CLB [4], and the detailed algorithm is as follows.

Assign VL to any or all CLBs with zero criticality and assign VH to the others. Assign VL to the CLB with stripped criticality (>0) and therefore the routing wires driven by it.Check the temporal arrangement constraints, cancel Step a pair of if there's any violation or otherwise update the provision of this CLB.Assign VL to the diffuse wire switches that don't cause any violations.Set the criticality of the present CLB to zero, and jump to Step a pair of if not all CLB criticalities are zero.The algorithm finishes when all CLB criticalities are zero, meaning that the supply voltage of all gates is assigned.

3.3. Power Estimation

Assigned appropriate supply voltages to all logic blocks, then estimate power consumption of the entire FPGA. In the core of the FPGA we concentrate only on the power consumption, and never try to optimize or estimate IO power consumption. Power evaluation framework used in this paper is based on that in [13]. The evaluation flow begins with a BLIF file that describes the design's function. This file is first packed by the T-Vpack. Then, its placement and routing results are generated by the VPR [14]. Afterward, the circuit design is mapped onto a single-V_{DD} FPGA and its timing graph is generated to guide the following V_{DD} assignment in a dual-V_{DD} FPGA. Simultaneously, the transition density of the whole circuit is analyzed by ACE. SPICE simulation is run to get the node capacitance in the FPGA, including the LCs. Finally, with all of the results above, FPGAs power consumption can be estimated. All the tools above are commonly used by FPGA researchers.

4. EXPERIMENTAL RESULT AND DISCUSSION

4.1. Results and Comparisons

Power reduction truly depends on the voltage values of VDDH and V_{DDL} due to the dual-V_{DD} architecture. In order to understand dependence and to come up with a good voltage choice, we varied V_{DDL} and fixed the high-V_{DD}. When V_{DDL} is increased than fixed value, the number of CLBs on low V_{DD} increases, the total power consumption is also increases. This happens because power consumption of the circuit elements is significantly higher than the fixed value. On the other side, when we reduce V_{DDL} to our fixed value the power consumption again increases because the number of CLBs and routing muxes on low V_{DD} becomes very low.

On the basis of the above dual-V_{DD} FPGA model, circuit level dual voltage assignment algorithm and power estimation model, different power reduction ratios under different VL were simulated and the optimal VL was selected as a baseline result. Meanwhile, according to the PDD and delay function obtained

above, the proposed basic model can generate an application dependent V_L. With the circuit parameters from the FPGA model, including transition density and capacitance, proposed model can generate an optimized V_L then existing model.
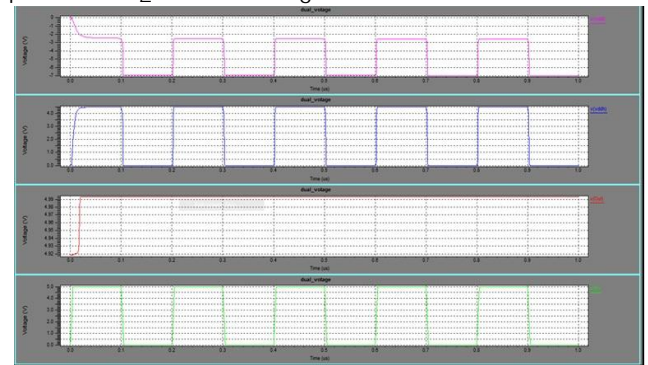

Fig.4.The output waveform for the circuit level model.

With the path overlapping proportions from part of the dual voltage assignment results, the proposed method can generate a further optimized V_L.
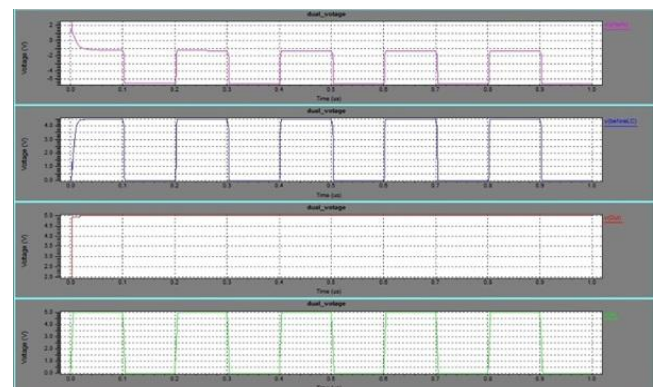

Fig.5.The output waveform for the body biasing model.

TABLE I
Comparing the effectiveness of circuit level and body biasing model for the dual voltage design

Parameter	Circuit Level	Body Biasing
Power(W)	0.654	0.570
Time consumption (Seconds)	4.17	2.24

The output waveform for circuit model and body biasing method is shown in Fig. 4 and Fig. 6. It shows that the proposed method is able to generate a V_L near to the baseline circuit-level method while requires computation time orders less. As shown in Table I, compare the effectiveness of circuit level

and body biasing model for the dual voltage design. It can be obviously concluded that the proposed dual voltage design method provides more power reductions than the fixed dual voltage design methods while consuming much less time than circuit-level methods.

5. CONCLUSION

A fast application-dependent method to estimate the optimum V_L/V_H ratio for a dual voltage FPGA design is presented in this paper. According to different applications, the method can give a V_L/V_H.The system will be developed by using Dual Mode Logic Switches and Body Biasing with voltage FPGA method to reduce the power reduction ratio.It has ability to reduce further more power than the circuit level power modeling while the computation time required is 100–10 000 times shorter. The final power reduction ratio is higher than the circuit level power model for FPGA in previous papers. Furthermore, it is possible to integrate the proposed methods into the synthesis tool of dual voltage FPGA, especially embedded FPGA, to make V_L and power optimized for applications.

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