International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 02 Issue: 05 | Aug-2015 www.irjet.net p-ISSN: 2395-0072

2D Mesh Topology for Routing Algorithms in NoC Based on VBR and CBR

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Abstract - ***NoC has been proposed as a highly structured and scalable solution to address communication problems in SoC. On chip interconnection network provides advantages over dedicated wiring and buses, i.e.low-latency, low-power consumption and scalability. The mesh topology has gained more designers due to its simplicity. However, source routing has one serious drawback of overhead for storing the path information in header of every packet. This disadvantage becomes as the size of the network grows. In this project we proposed a technique, called Junction Based Routing (JBR), to remove this limitation. In the proposed technique, path information for only a few hops is stored in the packet header. In this project, we have design 2D Mesh topology for NoC by using XY, OE and JBR (OE) algorithm on the basis of CBR and VBR. The parameter design parameters viz. latency, total network power and throughput are compared on the basis of CBR and VBR. It is observed that latency and throughput is improved in case of VBR as compared to CBR and Total Network Power is reduced for VBR as compared to CBR.***

Key Words: *NoC, 2D mesh topology, Routing algorithms, Junction based routing, VBR traffic, simulator etc.*

1. INTRODUCTION

NoC has been proposed as a highly structured and scalable solution to address communication problems in SoC. On chip interconnection network provides advantages over dedicated wiring and buses, i.e., high-bandwidth, low-latency, low-power consumption and scalability. NoCs designs many types of topology such as Mesh, Torus, Star, Octagon and SPIN. Design of NoC router architecture depends upon the network topology. The mesh topology is the most common network topologies.The main features of NoC platforms are routing algorithm and topology. The NoC parameters are used to gives better performance of the system as compared to SoC.For evaluating NoC using a simulator, data is transmitted into the network in different ways and performance values are evaluated regarding the traffic.

Number of messages is transported back and forth via the interconnection networks. Thus, the interconnections among multiple cores on a chip have a significant impact on communication and performance of the chip design in terms of end-to-end delay, throughput, and packets loss ratio. Therefore, it is worthwhile studying the different characteristics of different topologies. Source routing has an important disadvantage of overhead for storing the path Information in header of each packet sent. This disadvantage becomes worse as the size of the network grows.The Junction Based Routing (JBR) can be used to remove this disadvantage. The idea of junction based routing is basically derived from the railway networks. Railway networks generally have a few large stations, called junctions which are connected by fast railways. A long distance journeys from a small town to another small town is achieved by first going to the nearest junction close to the source and from there reaching a junction close to the destination.

2. LITERATURE REVIEW

Sumant Katiyal, Jayesh kumar Dalal, Parag Parandkar proposed that Network on chip is a scalable and flexible communication architecture for the design of core based System-on-Chip. Communication performance of a NOC heavily depends on routing algorithm. XY routing algorithm is distributed deterministic routing algorithm. Odd-Even (OE) routing algorithm is distributed adaptive routing algorithm with deadlock-free ability. DyAD combines the advantages of both deterministic and adaptive routing schemes. Key metrics which determines best performance for routing algorithms for Network-on-Chip architectures are Minimum Latency, Minimum Power and Maximum Throughput. We demonstrated the impact of traffic load (bandwidth) variations on average latency and total network power for three routing algorithms XY,

OE and DyAD on a 3x3 2-dimensional mesh topology. The simulation is performed on nirgam NoC simulator version 2.1 for constant bit rate traffic condition. The simulation results reveals the dominance of DyAD over XY and OE algorithms depicting the minimum values of overall average latency per channel (in clock cycles per flit) as 1.58871, overall average latency per channel (in clock cycles per packet) as 9.53226, overall average latency (in clock cycles per flit) as 26.105, and total network power as 0.1771 milliwatts, achieved for DyAD routing algorithm.

Pan Hao, Hong QiI, Du Jiaqin & Pan Pan, purposed that NOC is to solve the choke point in communication and the clock problem from architecture. Each route in NOC includes some routers, and it takes a few clock periods by passing a router. When the network is in congestion, the package transmission will produce much more time delay. So adopting a appropriate routing algorithm to get the balance between the time delay and throughput rate becomes the key problem. In this paper, we have done some research on XY and OE algorithms based on the 4×4 mesh topology by using NIRGAM emulator. The result shows that the ratio of throughput rate and package time delay is 2.5358 in OE routing algorithm, which is larger than 2.1126 in XY routing algorithm, and it proves that the OE routing algorithm is better to Mesh topology than OE routing algorithm.[12]

Saad Mubeen and Shashi Kumar described very important for exploiting enormous computing power available on a multicore chip. Routing algorithms significantly affect the performance of a NoC. Most of the existing NoC architectural proposals advocate distributed routing algorithms for building NoC platforms. Although source routing offers many advantages, but researchers avoided it due to its apparent disadvantage of larger header size requirement that results in lower bandwidth utilization. From this conclusion they proposed a strong case for the use of source routing for NoCs, especially for platforms with small sizes and regular topologies. first selects the most appropriate deadlock free routing algorithm, from a set of routing algorithms, based on the application's traffic patterns. Then the selected (possibly adaptive) routing algorithm is used to compute efficient static paths with the goal of link load balancing. The simulation results that 28% lower latency even at medium load, as compared to distributed routing. Also designed a router to support source routing for mesh topology NoC platforms. A Matlab based tool called MatPC has been developed for this purpose. From this, the use of source routing in mesh topology NoC, because of the small and fixed size of practical NoCs, the overhead of source routing is negligible and it is easily compensated by a large number of its advantages, including lower router cost and higher communication speed of the router. Evaluation results show that source routing gives higher latency and throughput performance as compared to corresponding distributed routing. [4]

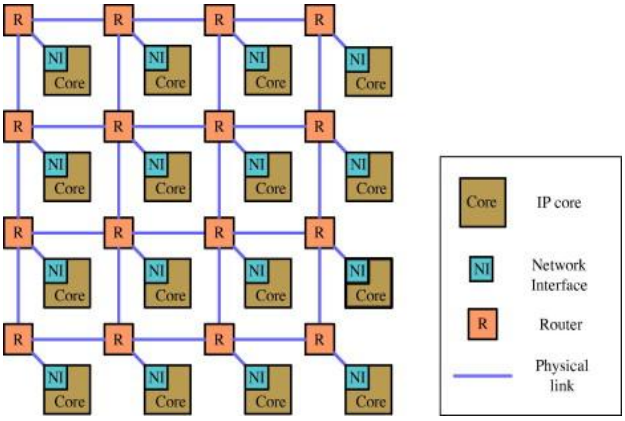
N. Ashok kumar, Nagarajan, S. Ravanaraja proposed that, Network-on-chip is a very active research field with many practical applications in industry. Based on the study, they identified as especially crucial for continued development and success of NoC paradigm as procedures and test cases for benchmarking, traffic characterization and modeling, design automation, latency and power minimization, fault-tolerance, QoS policies, prototyping, and network interface design. They developed efficient communication architectures, in some cases specifically optimized for specific applications. There is a converging trend within the research community towards an agreement that Networks on Chip constitute an enabling solution for this level of integration. Also their proposal has a variable impact in performance while traditional fault-tolerant solution like Hamming Code has a constant impact. Besides their proposal can save among 15% to100% the energy when compared Hamming Code. [5]

Wang zhang, liganghou, leizuo, proposed that Networks-on-chip (NoCs) have emerged as an alternative to ad-hoc wiring or bus-based global interconnection in Systems-on-Chip (SoCs). The architecture of network significantly determines system performance. This paper proposes a network on chip architecture with 2-demention mesh topology, odd-even routing algorithm, wormhole switching technique and only input buffers. The size of packet is 20 bytes and that of flit is 5 bytes. The performance of proposed architecture is evaluated based on metrics of latency and throughput per channel under Constant Bit Rate (CBR) and Bursty traffic. For the proposed architecture, the evaluation results reveal that the average latency of whole network channels is 1.97 cycles under CBR traffic and 1.92 cycles under Bursty traffic. The average throughput of whole network channels is 8.8555 Gbps under CBR traffic and 8.8212 Gbps under Bursty traffic. [15]

3. NETWORK ON CHIP

Network on chip is a communication subsystem on an integrated circuit (commonly call "chip"), typically between IP cores in a system on chip (SoC).The basic properties of the NoC are:

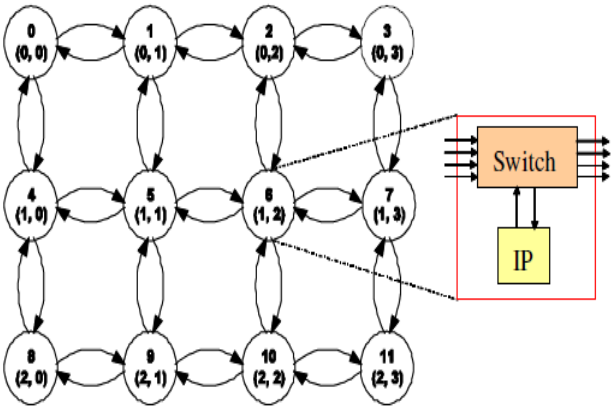
1. Separates communication from computation
2. Avoids global, centralized controller for communication.
3. Allows arbitrary number of terminals.



Network-On-Chip (NoC) consists of IP core, Network interfaces, routers, links. In NoC each core is connected to a switch by a network interface. The function of a network interface that define how data packets are formatted for transmission and routing.Routers direct data over several links (hops).Links connect switches with network interfaces or with other switches. NoC architecture consists of various topology as:
Mesh, Ring, Torus, Star etc.

3.1 Mesh Topology

Network topology provides the interconnection of various elements (links, nodes, etc.) of a network. Design of NoC router architecture depends upon the network topology. The mesh topology is one of the most common network topologies to use.Two-dimensional mesh topology will be used throughout in this. It is oneof the easiest topologies to implement on a silicon die, because of its flat configuration.A mesh-shaped network consists of m columns and n rows. The routers are situated in the intersections of two wires and the computational resources are near routers. Addresses of routers and resources can be easily defined as x-y coordinates in mesh. Mesh topology is easy to implement as all nodes are in equally distance as shown in Figure:



It is one of the easiest topologies to implement on a silicon die, because of its flat configuration. Mesh size given as R x C means the number of node rows is R and the number of node columns is C. Cube and hypercube are also regular topologies similar to mesh.

4. ROUTING ALGORITHMS

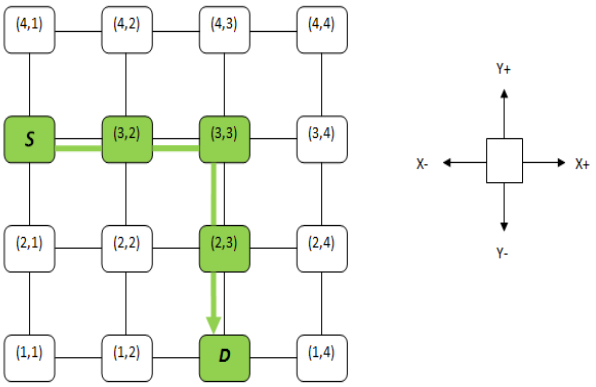
Routing algorithms define the path taken by a packet between source and target switches. They must prevent deadlock, Live lock, and starvation [8][9] situations. Deadlock may be defined as a cyclic dependency among nodes requiring access to a set of resources, so that no forward progress can be made, no matter what sequence of events happens [6]. Live lock refers to packets circulating the network without ever making any progress towards their destination. Starvation happens when a packet in a buffer requests an output channel, being blocked because the output channel is always allocated to another packet. Routing algorithms can be classified according to the three different criteria: (i) where the routing decisions are taken; (ii) how a path is defined, and (iii) the path length. In source routing, the whole path is decided at the source switch, the header of the packet has to carry all the routing information, increasing the packet size [9].

Routing schemes have been classified in several ways in literature. In a scheme called Source routing, the source node selects the entire path before sending the packet. The major drawback of this approach is that each packet must carry this routing information, thus increasing the packet size. In addition, the path cannot be changed after the packet has left the source. A more common solution is the use of distributed routing. Here a router upon receiving a packet decides, based on the destination address, whether it should be delivered to the local resource or forwarded to a neighboring router. In the latter case, a routing algorithm is invoked (or a routing table is accessed) to determine which neighbor the packet should be sent. Source routing was not considered suitable for very large and dynamic networks because of the overhead on packet size. But it is likely to have some advantages for small networks with regular topologies, especially with networks having an upper limit on the number of output ports in the routers. Mesh topology NoC is one such network. This will simplify the design of the router since the routing information is directly available in the packet. The overhead may also be reduced since we do not need to carry destination address.

4.1 X-Y Routing Algorithm

In X-Y routing, if the column of the source and the column of the destination are different, a packet moves along the

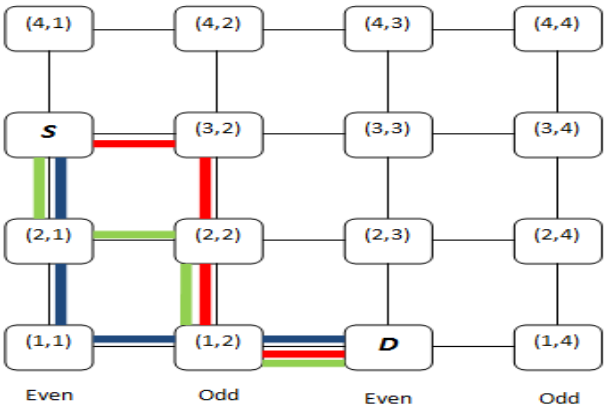
horizontal axis toward the destination. After that it makes progress to the destination vertically. In Figure, source node (3, 1) is communicating with (1, 3). The path which is shown using the vector is allowed for sending data from S to D.



Allows path in XY routing algorithms.

4.2 OE Routing Algorithm

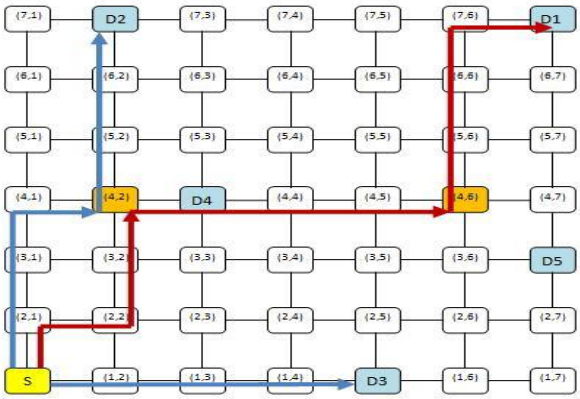
Odd-Even routing algorithm is another partially adaptive routing algorithm and has a higher adaptiveness in compared with the other routing algorithms [3][7]. Packets are not allowed to make an East-North or East-South turn at the nodes that are in an even column of a mesh network. North-West or South-West turn is limited at the nodes that are in an odd column. For instance, source node S is sending data to destination node D. Applying Odd-Even routing algorithm, there are three possible paths for sending data from S to D that are shown in Figure:



There are many other deadlock free routing algorithms for mesh topology NoCs.

4.3 Junction-Based Routing

Source routing has an important disadvantage of overhead for storing the path information in header of each packet sent. This disadvantage becomes worse as the size of the network grows. In this chapter we describe a routing technique, called Junction Based Routing (JBR) to remove this disadvantage. The idea of junction based routing is basically derived from the railway networks. Railway networks generally have a few large stations, called junctions which are connected by fast railways.A long distance journeys from a small town to another small town is achieved by first going to the nearest junction close to the source and from there reaching a junction close to the destination. Consider the following 7x7 mesh topology NoC that has the diameter of 13 hops.



The node that is presented using (x,y) is located at xth row and yth column. Distance between nodes that is located at position (x1, y1) and (x2, y2) is calculated using the formula:
Distance = |y2-y1| + |x2-x1|. The number of routers used from a source node to a destination node is equal to the number of links used plus one. We define hop count as number of routers on the path from a source to the destination.
Hop Count = Distance + 1.

5. VARIABLE BIT RATE TRAFFIC

The VBR service category is used for connections that transport traffic at variable rates traffic that relies on accurate timing between the traffic source and destination. An example of traffic that requires this type of service category are variable rate, compressed video streams. Sources that use VBR connections are expected to transmit at a rate that varies with time (for example, traffic that can be considered bursty). VBR connections can be characterized by a Peak Cell Rate (PCR), Sustained Cell Rate (SCR), and Maximum Burst Size (MBS).

6. CONSTANT BIT RATE TRAFFIC

It is synthetic traffic generator. Configurable parameters for CBR traffic are as follows: Packet size (in bytes) Load percentage (percentage of channel bandwidth to be used). Destination - User can specify a fixed destination or randomly chosen destination. Inter-flit interval (in clock cycles).

Algorithms	XY		JBR(OE)	
Traffics	CBR	VBR	CBR	VBR
OAL/channel (CC/F)	14.6	9.70	10.47	8.83
Total Network Power(watt)	0.22	0.19	0.362	0.224
Throughput (Gbps)	18.5	17.1	18.15	16.45

7. PERFORMANCE PARAMETERS

Some of the most important parameters that are used in evaluating the performance of NoCs are defined in this sub-section briefly.

7.1 Latency

Network latency presents the required time to transfer n bytes of payload from its source to its destination. Latency consists of routing delay, contention delay, channel occupancy and overhead.

7.2 Bandwidth

Communication bandwidth is the amount of data that can be moved using a communication link in a unit time period.

7.3 Throughput

Throughput is the total number of received packets by the destinations per time unit.

7.4 Packet Loss

Packet loss happens when one or more packets do not reach their destination due to the error introduced by the network, the contention for network link or lack of buffer space etc.

8. OBSERVATION

From literature review, we observe that the performance of parameters using comparative study:

TNP= Total Network power (watt), OAL= Overall average Latency (clock cycle/flits).

P= Average Throughput of Network/ Average Latency per packet of Network.

9. CONCLUSION

In this the routing algorithms XY and JBR(OE) for NoC architecture of mesh topology is studied under CBR and VBR. Also, we compare their results using parameters such as latency, max. Throughput and power under CBR and VBR. By using this algorithms, we compare parameters of Total network power, Average latency per channel (in clock cycles per flit), average latency per channel (in clock cycles per packet), average latency (in clock cycles per flit) and Throughput with previous results. Through this we conclude that performance of overall average Latency (CC/F) under VBR for all three algorithms is better than under CBR. Also, we conclude that performance of Total network power(watt) under VBR is better than CBR. Also, We conclude that performance of Max. Throughput under CBR is better than under VBR.

10. FUTURE SCOPE

In future, we can find out the performance of throughput, power, latency by increasing size of networks using JBR(OE) algorithms. Also, we can show the results of parameters with various traffics such as(Hot spot traffic, Random traffic).We can compare performance of these parameters with given traffics(CBR,VBR) and various traffics(Hot spot traffic, Random traffic).

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