Implementation of Split Array Based Charge Scaling DAC

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Abstract— ***This Paper presents the implementation of 6 bit split array based charge scaling DAC, with low power dissipation and less area. Proposed design is implemented in Cadence virtuoso tool using GPDK 180nm CMOS technology, with supply voltage of 1V. Split array based charge scaling DAC is employed in Successive Approximation register ADC or can be used as standalone device in wireless sensor network Transceivers. The output voltage swing provided by the DAC is -0.2mV to 0.93mV in steps of 14.6mV. The design has DNL error less than 0.5 LSB.***

Index Terms- **Two-stage op-amp, DAC, DNL, ICMR, low power, low area**

1.INTRODUCTION

Data converters lie at the heart of modern Digital Signal Processing systems. The real time analog signals are to be converted to digital signals, due to ease of processing. Therefore, data converters are used as interface circuitry between digital and analog domain [1].

As the development of Radio Frequency (RF) communication assisted by progress in VLSI technology has made it practical to build high rate compactly packed digital circuit [2]. Figure (1) shows the application of converters in Wireless Sensor Network (WSN) transceiver system.

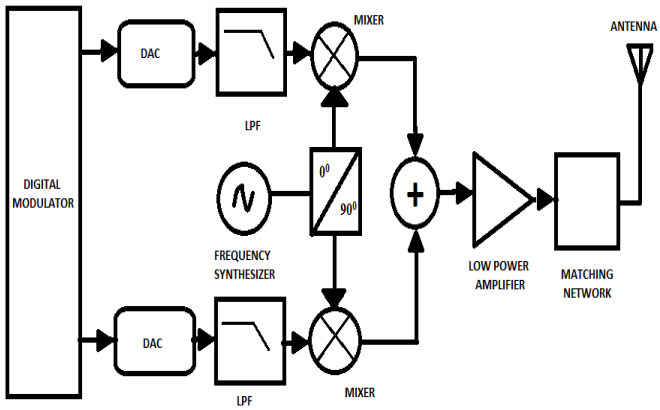

Figure 1: Direct conversion transmitter used in WSN transceiver

In WSN Transceivers, ADC converts the continuous signal to digital signal for processing. Once processing is done, DAC converts the digital signal to analog signal, which is then smoothened by Low Pass Filter and up-converted using mixer for wireless long distance communication.

2. Proposed dac Architecture

Charge scaling DAC with split array is presented in Figure (2) which decreases area and power by splitting the Binary Weighted Capacitor (BWC) array into two sub-arrays [3]. To make the total capacitance of the LSB array equal to the capacitance of the lowest bit in the MSB array, an attenuation capacitor with a fractional value is inserted. The result of the capacitor array is given to the op-amp to get the resultant analog signal.

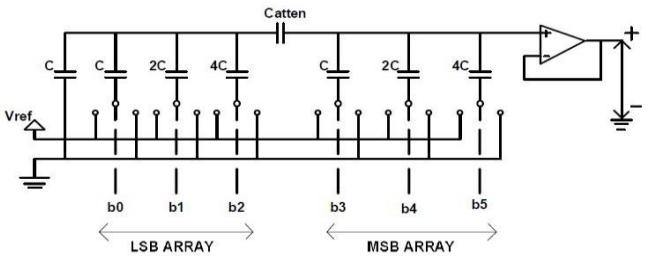

Figure 2: Proposed DAC

2.1 Op-amp

The Op-amp used in the proposed DAC architecture is the two stage op-amp as shown in Figure (3), the

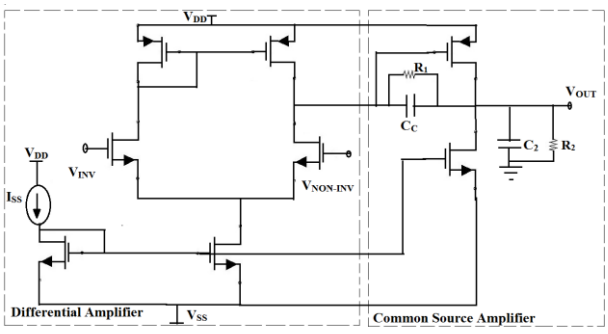

Figure 3: Two Stage Op-amp

initial stage is the differential amplifier (In figure (4)) that yields high gain. Differential signals reject common mode noise, robust to supply noise, simpler biasing and has higher linearity. For extremely low common mode level the transistor M_1 and M_2 will turn off causing a severe clipping at the output.

Therefore the bias current should have least dependence on input common mode level. To solve this problem current source I_{SS} is used for I_{D1}- I_{D2} to be independent of input common mode level [4]. If V_{IN-} is much more negative then M_1 is OFF, M_2 is ON.

$$V_{OUT} = V_{DD} - I_{SS} R_D \quad \text{.....(1)}$$

If V_{IN-} increases M_1 gradually turns ON , drawing a part of I_{SS} from R_{D1} and hence $\mathbf{V_{OUT}=V_{DD} - (I_{SS}/2)\ R_D}$ increases. As V_{IN-} becomes more positive M_1 carries greater current than M_2 and V_{OUT2} increases. For larger V_{IN-} - V_{IN+} , M_1 hogs all of I_{SS} turning M_2 OFF, as a result $\mathbf{V_{OUT} = V_{DD}}$.

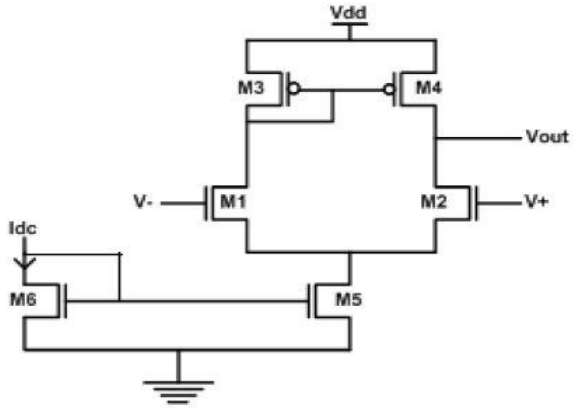

Figure 4: Differential Amplifier

The second stage of Op-amp is the Common source amplifier shown in figure (5). The output swing and gain of differential amplifier is increased by using a common source amplifier. Load impedance of common source stage is increased to increase the gain. However increasing the output impedance limits the output voltage swing. Therefore, load of the common source stage is restored by a current source.

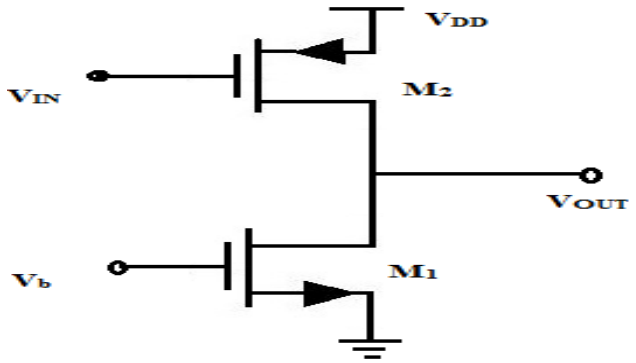

Figure 5: Common Source Amplifier

2:1 MUX SWITCH

2:1 multiplexer is employed as switch in proposed DAC. A multiplexer (MUX) is a switch that directs one of its inputs to the output. The input select signal decides which input to be moved to the output. Multiplexer is unidirectional. Multiplexer is used in application where input must be chosen from multiple data to a single output [5].

A 2:1 multiplexer requires an inverter and two Transmission gate (TG). The input select signal activates one of the TG. If V_{IN} is "logic 1", V_{REF} is passed to the output V_{OUT}. When V_{IN} is "logic 0", output is linked to gnd.

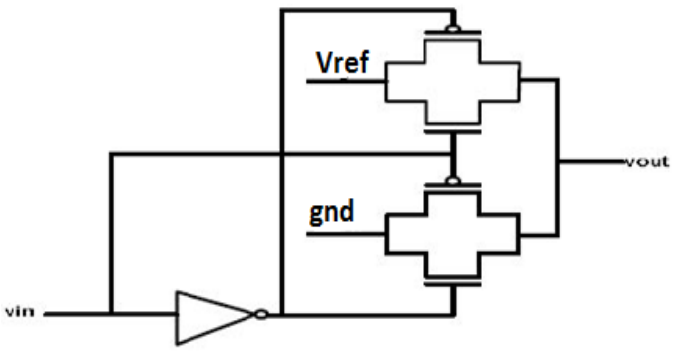

Figure 6: 2:1 MUX as Switch

3.DESIGN OF DIGIAL TO ANALOG CONVERTER ARCHIETECTURE

Design of op-amp begins with the power budget [6]. Two-stage Op-amp is designed by beginning with total power consumption of DAC to be 500µW. So, Op-amp with power consumption in the order of few microwatts is to be designed. Beginning with this given power, and using supply voltage of 1V in 0.18 n-well CMOS technology, value of total current flowing through the op-amp is calculated.

Input transistors are designed so that maximum current flows through them, as the input transistors decide the gain of op-amp. Assuming overdrive voltage to be 0.2V, and using $\mu_n C_{ox}$=300µA/V^2 and $\mu_p C_{ox}$=60µA/V^2, the values of W/L of all transistors are calculated. Since, digital to analog converter is designed for 6-bit resolution; hence, minimum op-amp gain required is given by 2^{N+1} i.e. 42dB and phase margin greater than 60^0 for system to be stable.

3.1 Design of Op-amp

The above requirements are satisfied by using design equations [7] given below:

Current through current mirror is obtained using,

$$Slew\ Rate = \frac{I_5}{C_C} \quad \text{.....(2)}$$

The dimensions of M_1, M_2 is obtained using,

$$G_{BW} = \frac{g_{m1}}{C_c} \quad \text{.....(3)}$$

The dimensions of M_3, M_4 is obtained using,

$$\left(\frac{W}{L}\right)_{3,4} = \frac{I_5}{\mu_p \times C_{OX} \times (V_{DD} - ICMR + + |VT3*(max)| + |VT1(MIN)|)^2} \quad \text{....(4)}$$

The dimensions of M_5, M_8 is obtained using,

$$\left(\frac{W}{L}\right)_{5,8} = \frac{2 * I_5}{\mu_n * C_{OX} * (V_{DSAT5})^2} \quad \text{.....(5)}$$

The dimensions of M_6, M_7 is obtained respectively using,

$$\left(\frac{W}{L}\right)_6 = g_{m6} \left(\frac{W}{L}\right)_4 \quad \text{.....(6)}$$

$$\frac{I_7}{I_5} = \frac{\left(\frac{W}{L}\right)_7}{\left(\frac{W}{L}\right)_5} \quad \text{.....(7)}$$

For system to be stable, phase margin to be greater than 60^0.

Therefore miller capacitance is given by,

$$\_ \quad C_C > 0.22 * C_L \quad \text{.....(8)}$$

3.2 Design of Capacitor array

Unit capacitance [8] is calculated using,

$$\sqrt{\frac{kT}{C_{total}} + \frac{LSB^2}{12}} \leq \frac{LSB}{2} \quad \text{.....(9)}$$

$$C_{total} = \left[2^{\frac{N}{2}} + \left(2^{\frac{N}{2}} - 1\right)\right] C_0 \quad \text{.....(10)}$$

Attenuation capacitance is calculated using,

$$C_{atten} = \frac{Sum\ of\ LSB\ Array\ Capacitors}{Sum\ of\ MSB\ Array\ capacitors} \times C_0 \quad \text{....(11)}$$

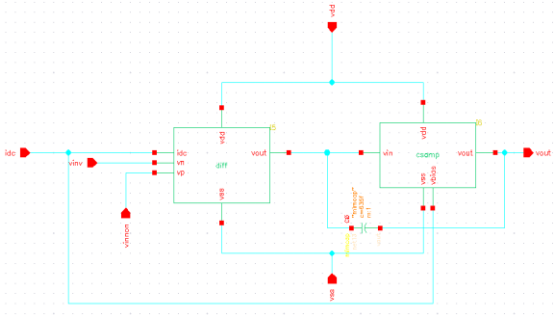

Figure 7: Schematic of Two-Stage Op-amp

Figure (8) shows the schematic of 2:1 MUX as a switch passing V_{REF} or connecting output to GND when input is "LOGIC 1" and "LOGIC 0" respectively.

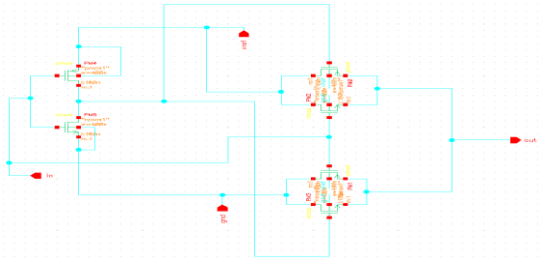

Figure 8: Schematic of 2:1 MUX as a Switch

Figure (10) shows the schematic of the proposed DAC.

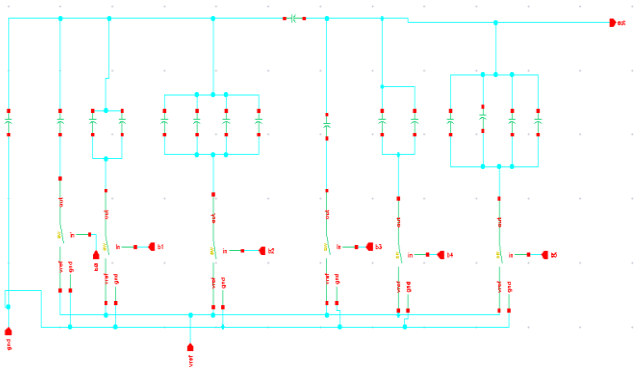

Figure 9: Schematic of capcitor array

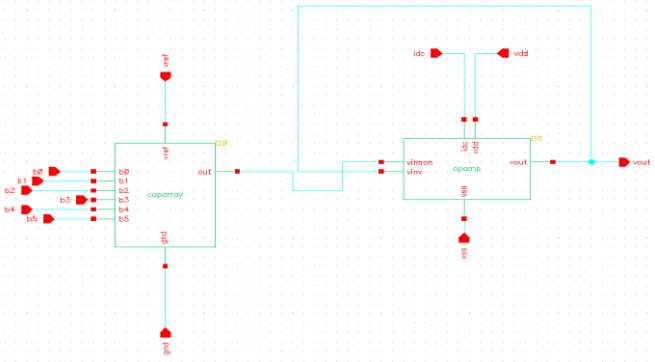

Figure (10): Schematic of Proposed DAC

4.SIMULATION RESULTS

Figure (11) and (12) shows the simulation result of Op-amp with gain of 52 dB and Phase Margin of 86^0.

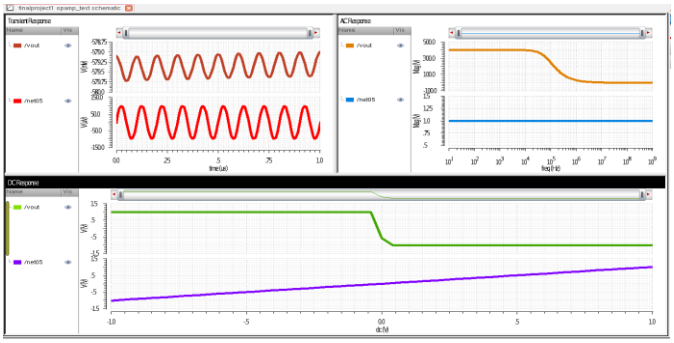

Figure 11: Simulation result of Two-Stage Opamp

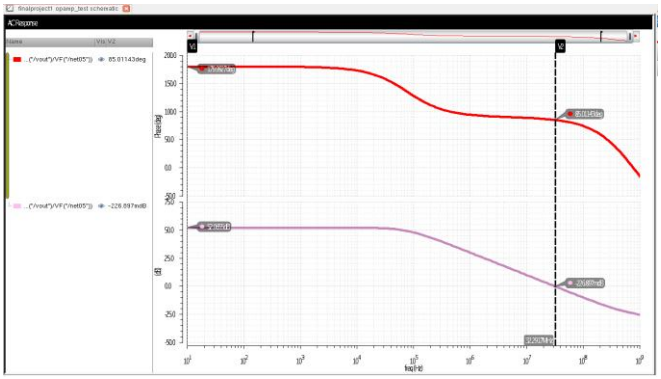

Figure 12: Gain and Phase Plot of Two-Stage Opamp

Figure (13) and (14) shows the simulation result and layout of Proposed DAC.

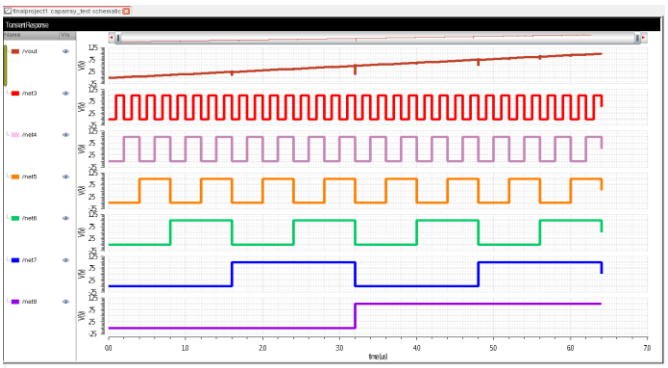

Figure 13: Simulation result of Proposed DAC

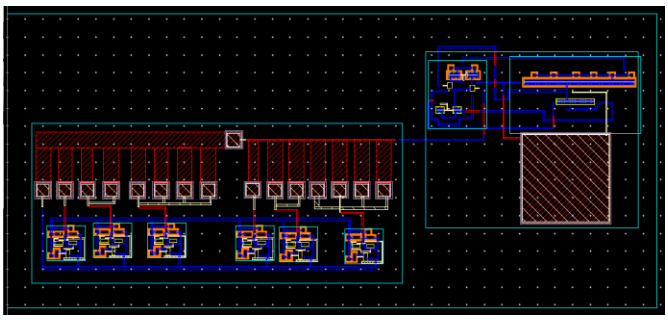

Figure 14: Layout of Proposed DAC

Chart-1 shows the DNL error of proposed DAC.

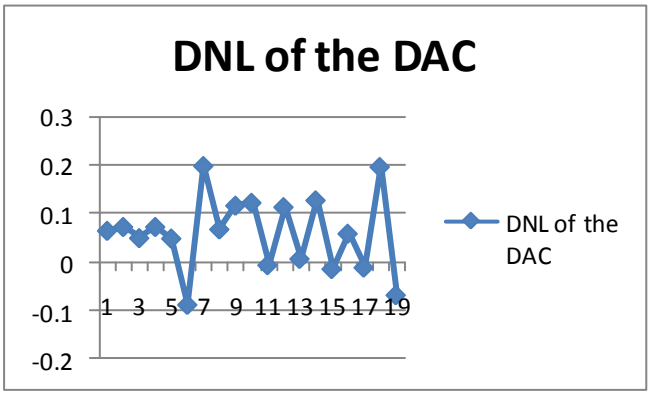

Chart-1: DNL of proposed DAC

5.PERFORMANCE SUMMARY OF PROPOSED DAC

	[2]	Proposed DAC
Technology	180nm	180nm
Supply voltage	1V	1V
Resolution	6 Bit	6 Bit
Power dissipation	1.5mW	0.5mW
UGW	16Mhz	30Mhz

6.CONCLUSION

In this paper, a DAC used in WSN transceivers has been investigated and designed. The design is mainly optimized for the low power, moderate resolution and moderate speed. Two stage op-amp is chosen as a basic component because of its advantages over other amplifiers. Two stage op-amp is simulated GPDK 180nm CMOS technology with gain and phase equal to 52dB and 86^0. Power dissipation of 370µw is achieved. Split array based charge scaling DAC is simulated with GPDK 180nm CMOS technology. The DAC is designed for resolution of 6-bit wit DNL error less than 0.5LSB. Power dissipation achieved is 499µW.

7.FUTURE WORK

The power dissipation can be further reduced by using split array DAC with monotonic switching procedure. By using this method parasitic capacitance is balanced and matching of capacitance is enhanced.

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