

# Evaluation of low power Schmitt Trigger for communication system

Annu Khurana<sup>1</sup>, Anshul Saxena<sup>2</sup>, Neeraj Jain<sup>3</sup>

<sup>1</sup> Research Scholar, ECED, MITRC College, Alwar, India

<sup>2</sup> Assistant Professor, ECED, MITRC College, Alwar, India

<sup>3</sup> Assistant Professor, ECED, MITRC College, Alwar, India

\*\*\*

**Abstract** - The CMOS device is used to achieve better performance in relations of power consumption, speed, magnitude, hysteresis and reliability. Schmitt trigger circuit lessened power dissipation and improving compatibility with low voltage power supplies and analog component the most effective solution is to reduce the power dissipation. This article accessible the presentation to comparison of six transistor (6T) conventional, and four transistor (4T) Schmitt trigger is castoff in such a way that by adjusting its voltage, the output can be ended to increase premature, thereby reducing the output delay with due to less converting time, power consumption is less, circuit is replicated in MATLAB tool in both 180nm and 90nm technology, a simulation result show that 4T Schmitt trigger 12.3% delay reduction and 24% power reduction.

**Key Words:** Schmitt trigger, Threshold voltage, Delay, Power dissipation, Hysteresis.

## 1. INTRODUCTION

Digital circuit does not directly suitable for defining the digital signal, for some reasons it may have slow rise or fall time and may have the small noise sense by proceeding circuitry, so all of these critical conditions required a specified device that will “clean up” or maintain a signal the required device is known as the Schmitt trigger [1], output state depends on input state and changes only as input level crosses a preset threshold level. Schmitt trigger device is mostly used in analog and digital (0 or 1) circuit as wave shaping device to resolve the noise problem [2], This device is widely used to drive the load with fast switching low power loss and low power supply [3]. Schmitt trigger has been used irrelevant to improve on/off (0 or 1) control state [4], and reduce the sensitivity to noise, for example, sensor [3], pulse with modulation circuit [6]. SRAM, Schmitt trigger is the decision making circuit [27]. Schmitt trigger is used to convert a slowly varying analog signal voltage into possible binary states, depending upon the analog voltage is above or below a predefined (preset) threshold voltage. The conventional (6T) Schmitt trigger circuit with different [1 to 0] and [0 to 1] transition threshold voltage (V<sub>H</sub> and V<sub>L</sub>) has better noise sensitive than the inverter [10], when the input signal goes to v<sub>dd</sub> to gnd, threshold voltage of the 6T Schmitt trigger circuit is (V<sub>H</sub>) and when the input signal goes down to gnd from v<sub>dd</sub>, So threshold voltage of the conventional Schmitt trigger is V<sub>L</sub> [15] [16], The main difference between Schmitt trigger and comparators

shows by DC transfer characteristics. Comparator show one switching threshold, besides Schmitt trigger shows difference switching threshold value for positive edge and negative edge input signal, this type of property is called hysteresis [16]. The Schmitt trigger is comparator that has positive feedback [5]. Power supply voltage is lowered; leakage power reduces [25]. The technology can be implemented completely at the circuit level these approaches involve many modifications on the Schmitt trigger structure [26]. Structural and electronic properties of schmitt trigger have been investigated by MATLAB tool [28] and under certain limiting conditions, all the results as derived in this paper get transformed into well known formulas of nanotechnology and the electron statistics [29].

## 2. CIRCUIT DESCRIPTION

### 2.1 Conventional Schmitt Trigger

The conventional 6T Schmitt trigger is the combination of three PMOS transistor and three NMOS transistor, (i.e. upper PMOS and lower NMOS) and considered as low for each other, the lower two NMOS transistor can be considered as series connection. Schmitt trigger can adjust its threshold in such a way that it can operate after its input exceeds the voltage of v<sub>dd</sub>/3 [17], The voltage transfer characteristic exhibits a typical as the show in fig, V<sub>OH</sub> is maximum output voltage, and V<sub>OL</sub> is the minimum output voltage. V<sub>H</sub> is the input voltage at which output switch from V<sub>OH</sub> to V<sub>OL</sub>. V<sub>L</sub> is the input voltage at which output switch from V<sub>OL</sub> to V<sub>OH</sub>; ΔH is called the hysteresis width [16]. The voltage is V<sub>H</sub>, V<sub>L</sub>, and ΔH.

$$V_H = V_{dd} - R \frac{V_{th}}{(R+1)} \quad (1)$$

$$V_L = \frac{R|V_{TP}|}{(R+1)} \quad (2)$$

Where the ratio  $R = \sqrt{\beta_n/\beta_p}$ ; The NMOS and PMOS transconductance parameter are  $\beta_n$  and  $\beta_p$  respectively. When the input is low, only PMOS will be Considered and causes the output to be high (equal to V<sub>dd</sub>), during this condition, P1, P2 and P3 are (because V<sub>GS</sub> < |V<sub>TP</sub>| source voltage and gate voltage is equal). Therefore, the output voltage is pulled to V<sub>dd</sub>. When the input increases to V<sub>dd</sub>, N<sub>1</sub>, N<sub>2</sub> and N<sub>3</sub> are turned ON. Thus, the output voltage pulled down to be ground. The PMOS and NMOS ratio is set according to following equation.

$$\frac{W}{L_{eff}} (PMOS) = \gamma \frac{W}{L_{eff}} (NMOS) \quad (3)$$

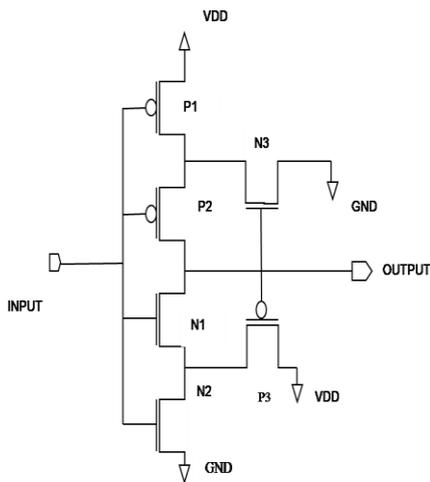


Figure 1. The conventional Schmitt trigger

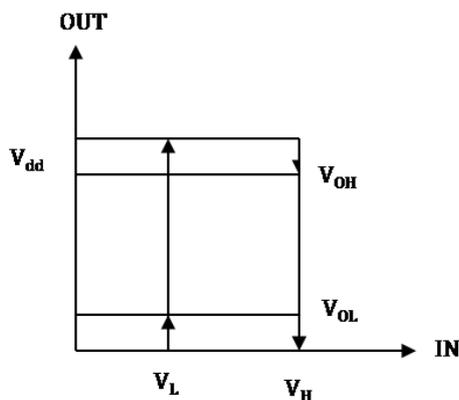


Figure 2. The transfer curve

### 2.2 4T Schmitt Trigger

The proposed circuit is created by a combination of one PMOS (P1) and three NMOS (N1, N2 and N3), there is no direct connection between power supply and ground as PMOS is connected to power supply and circuit output, beside NMOS is connected to output and ground node, there is no static power due to no direct connection between power supply to be ground.

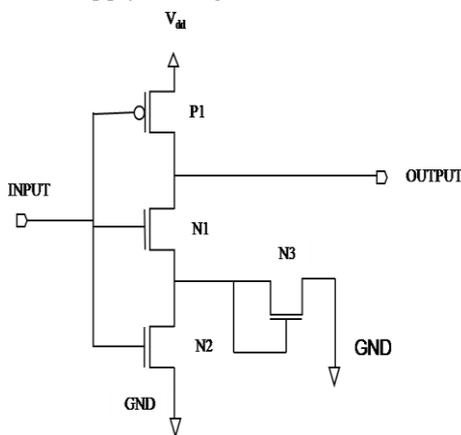


Figure 3. The proposed Schmitt trigger

### 3. SIMULATION RESULT:

The circuit works simulated in cadence for 180nm and 90nm technology, from the result table, we can observe that 90nm technology, and we are getting effective percentage reduction in delay and power as compared to 180nm technology.

#### 3.1 Propagation Delay

The time difference between the input increasing the reference voltage and output changing the logic state is known as the propagation delay, propagation delay time of the Schmitt trigger generally varies as a function with the amplitude of input; a larger input will result in a smaller delay time. The delay time after the circuit is measured as the average of response time of the gate for positive and negative output transition for the sine wave at 1GHz. Delay will reduce when the voltage is increased [13],

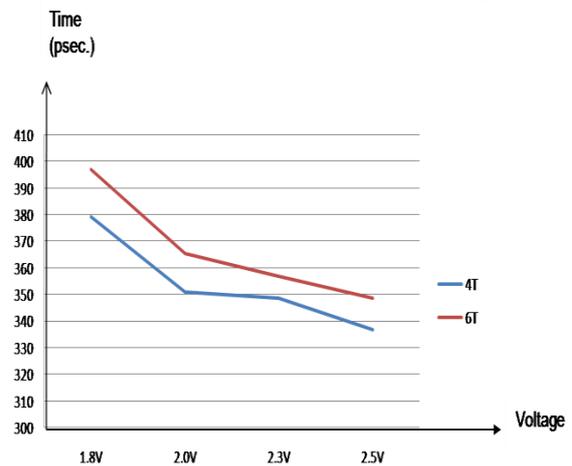


Figure 4 Delay analyses in 180nm technology

The main goal of using the Schmitt trigger in our project, that we can set the threshold limits as per our requirements. Due to observe that 4T Schmitt trigger gives a better performance as compared to 6T conventional Schmitt trigger, due to lower threshold voltage of the Schmitt trigger, we can observe that the signal rise and fall time lower provides a fast signal propagation and less delay in 90nm technology.

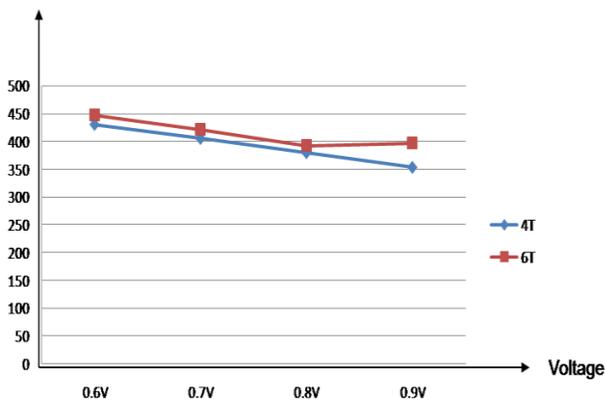


Figure 5 Delay analyses in 90nm technology

### 3.2 Hysteresis

Hysteresis is the property of quality of the Schmitt trigger, in which the input threshold change depending on whether the input is rising or falling, in another way hysteresis is the difference between the input signal level at which a Schmitt trigger is standby mode and active mode(OFF and ON state)[16], The little bit amount of hysteresis can be useful in a Schmitt trigger circuit because it reduces the circuit sensitivity to noise and helps reduces multiple transition of output when changing state.

$$\Delta H = V_H - V_L \quad (4)$$

$$V_H = 1.528V, V_L = 0.651V, \Delta H = 0.877V \quad (5)$$

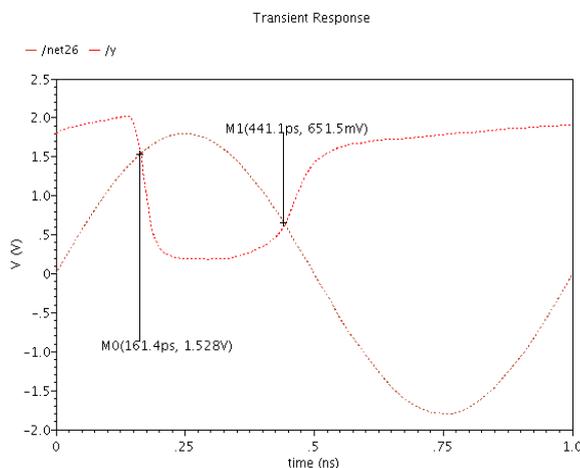


Figure 6 Hysteresis measurement of the Schmitt trigger

### 3.3 Power Analysis

In the Schmitt trigger either the transistors are in off mode or in on mode due to the early switching of opposite level [13], for the 180nm technology, as shown in fig, with 4T Schmitt trigger in consumes a power off 7.38pw and with conventional Schmitt trigger, it consumes 8.88pw power, so, we achieved a power reduction of 16.89% in this case. In 90nm technology, for the same example with 4T Schmitt trigger, it consumes a power of 1.67pw and with 6T, conventional Schmitt trigger; it consumes 2.2pw power, so we achieved a power reduction of 24% using the 4T Schmitt trigger. It can we observe that in 90nm technology, more power reduction in comparison to

180nm technology. And also varied supply voltage and shows the change in power for both 180nm and 90nm technology as shown in figure.

Power in 6T in 90nm technology= 2.2pw, Power in 4T in 90nm technology= 1.67pw, % Reduction in power =  $(2.2 - 1.67) / 2.2pw \times 100 = 24\%$

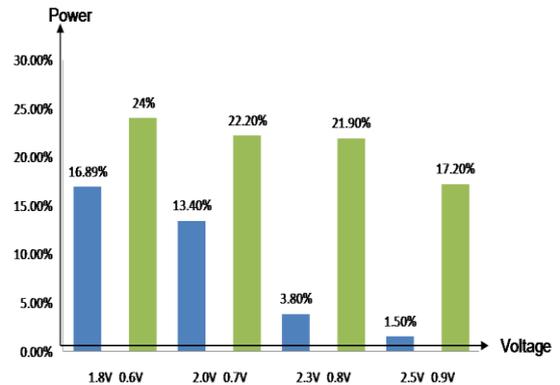


Figure 7 Power reduction graph in 180nm and 90nm technology

Table 1: Show the parameter of 6 transistor on 180nm

Voltage (Vdd)	Delay	Leakage Power	Hysteresis
1.8V	396.9Psec	8.88PW	0.869V
2.0V	365.2Psec	15.33PW	0.836V
2.3V	356.8Psec	132.4PW	0.72V
2.5V	348.5Psec	235.6PW	0.58V

Table 2: Show the parameter of 6 transistor on 90nm

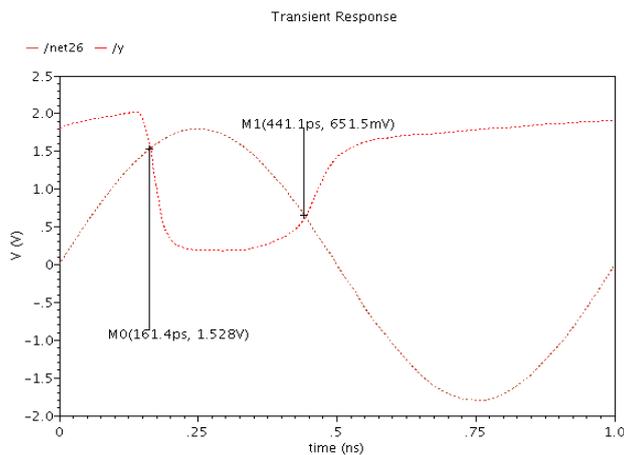
Voltage (Vdd)	Delay	Leakage Power	Hysteresis
0.6V	447.3Psec	2.2PW	649.61mV
0.7V	421.6Psec	9.9PW	592.01mV
0.8V	396.6Psec	18.29PW	511.6mV
0.9V	372.5Psec	19.29PW	444mV

Table 3: Show the parameter of 4 transistors on 180nm

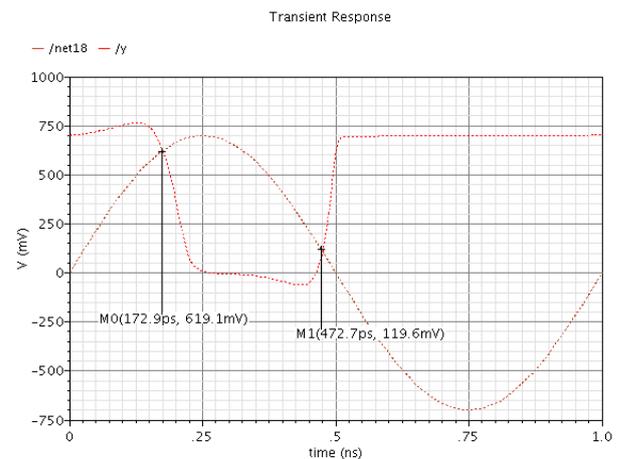
Voltage (Vdd)	Delay	Leakage Power	Hysteresis
1.8V	379.3Psec	7.38PW	0.583V
2.0V	350.9Psec	13.27PW	0.538V
2.3V	348.0Psec	127.28PW	0.488V
2.5V	336.8Psec	232.0PW	0.429V

Table 4: Show the parameter of 4 transistor in 90nm

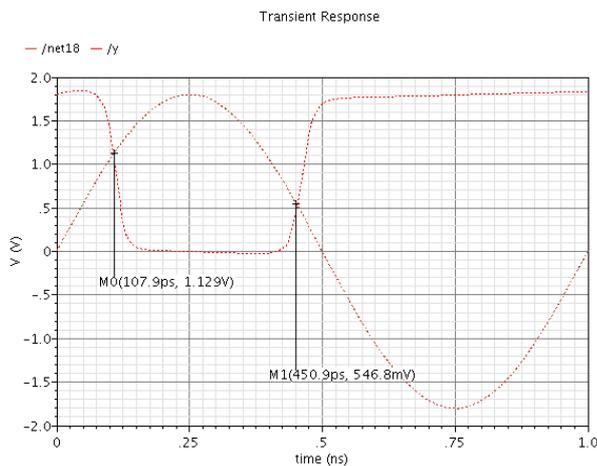
Voltage (Vdd)	Delay	Leakage Power	Hysteresis
0.6V	430.7Psec	1.67PW	572.35mv
0.7V	405.5Psec	7.7PW	499.1mV
0.8V	379.7Psec	17.28PW	441.3mV
0.9V	353.2Psec	15.97PW	349.2mV



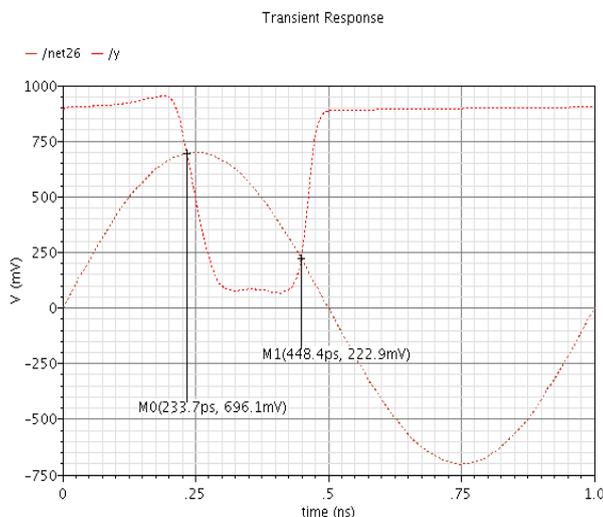
**Figure 8** Transfer characteristic of 6T Schmitt trigger in 180nm



**Figure 11** Transfer characteristic of the 4T Schmitt trigger in 90nm



**Figure 9** Transfer characteristic of the 4T Schmitt trigger in 180nm



**Figure 10** Transfer characteristic of the 6T Schmitt trigger in 90 nm

**4. CONCLUSION:**

I proposed Schmitt trigger is modified by using four transistors having less average power consumption with decreases in area; delay is also decreased by using only one PMOS as because delay is more concentrated to PMOS due to less mobility of holes compared to electrons, proposed Schmitt trigger is created by using 4transistor and have better performance than the conventional Schmitt trigger as there are fewer transistor counts by which area is reduced and delay is also reduced; the average power consumption of the proposed Schmitt trigger is less in comparison to the conventional Schmitt trigger, measured result correctly verified the principle of operation and characteristic of the low-power Schmitt trigger circuit. The circuit has been used for the design of low power.

**ACKNOWLEDGEMENTS:** This work was supported by MITRC, Alwar, with the calibration MATLAB design system Bangalore.

**REFERENCE**

- [1] C. Zhang, A. Srivastava and P. Ajmera, "Low Voltage CMOS Schmitt Trigger Circuit," IEEE Electronics Letters, Vol.39, No.24, pp.1696-1698, nov. 2003.
- [2] C. Wu and C. Chiang, "A low Photo Current CMOS Retinal Focal-Plane Sensor with a Pseudo-BJT Smoothing Networking and an Adaptive Current Schmitt Trigger for Scanner Application" ,IEEE Sensors J. Vol.4, No.4, pp. 510-510, August 2004.
- [3] H.Morimura, T. Shimannura, K. Fujii, S. Shigematsu, Y. Okazaki and M. Katsuyuki, "A zero sink current Schmitt trigger and window flexible counting circuit for fingerprint sensors/identifier" IEEE International Solid State Circuit Conference (ISSCC), Vol.1, pp.122-517, 2004.
- [4] S.L.Chen and K.Ming-Dou, "A new Schmitt trigger circuit in a 0.13μ 1/2.5v CMOS processes to receive 3.

- 3v input signals," IEEE Transaction on Circuits and System 2; Express Briefs, Vol.52, issue 7. pp. 361-365, 2005.
- [5] V. Pedroni, "LOW-Voltage high speed Schmitt trigger and compact window comparator," IEEE Electronics Letter, Vol.41, no.22, 1213-1214, 2005.
- [6] H. Kim, H.J.Kim and W.S.Chung, "Pulse width modulator circuit using CMOS Oats," IEEE Transactions on Circuit and System 1; Regular papers, Vol.54, pp.1869-1878, sept. 2007.
- [7] C. Kho Pham "CMOS Schmitt Trigger Circuit with controllable hysteresis using logical threshold voltage control circuit" IEEE Vol.36, No.1821-1824, 2007.
- [8] Kulkarni, K. Kim, and K. Roy, "A 160mV robust Schmitt trigger based sub-threshold SRAM," IEEE J. Solid State Circuits, Vol.42, NO. 10, pp. 2303-2313, October 2007.
- [9] Jay deep P. Kulkarni, Keejong Kim, and Kaushilc, "A 160mV robust Schmitt trigger based sub-threshold SRAM," IEEE Journal of the solid-state circuit. Vol.42, No. 171-176, Oct 2007.
- [10] V.Katyal, R. L. Geiger and D. J. Chen, "Adjustable Hysteresis CMOS Schmitt Trigger," IEEE ISCAS, pp.1938-1941, 2008.
- [11] Yoichi Sasaki, Kazuteru Nanba and Hideo Ito, "Circuit and latch capable of masking soft error with Schmitt trigger," Journal of Electronic Testing Vol. 24, No. 1-3 2008.
- [12] Sungsik Lee, Ahra Lee, Chang Han Je, Myung Lee, Gunn Hwang and Chang-Auck Choi "1.5v sub mw cmos interfaces circuit for capacitive sensor application in ubiquitous sensor networks" ETRI Journal, viol.30, No.5, oct. 2008.
- [13] S.Saini, S. Veeramachaneni, A. M. Kumar, M.B. Srinivas, M.B., "Schmitt trigger as an alternative to buffer insertion for delay and power reduction in VLSI interconnects," TENCON 2009-2009 IEEE Region 10 conferences, pp. 1-5, 2009.
- [14] F.Yuan, "A high-speed differential CMOS Schmitt trigger with regenerative current feedback and adjustable hysteresis," Analog Integrated Circuit and Signal Processing, Vol.63, No.1, pp.121-127, 2010.
- [15] F. Yuan, "Differential CMOS Schmitt trigger with tunable hysteresis," Analog Integrated Circuit and Signal Processing, Vol.62, No.2, pp.290-248, 2010.
- [16] Avireni Srinivasulu, "A Novel current Conveyon based Schmitt trigger and its application as a relaxation oscillator" Vol.39, No. 678-686. Issue6. 29 ARP 2010.
- [17] Zafer Takhirav, Bobak Nazer, and Ajay Jashi, "Error mitigation in digital logic using a feedback equalization with Schmitt trigger (FEST) circuit" IEEE, Vol.22, No. 321-327, 2011.
- [18] Pratchayaporn Singhanath Varakorn Kasemsuwant and kittipal Chitsakul, "DTMOS Schmitt Trigger with fully adjustable hysteresis" IPCSIT Vol.7 (2011).
- [19] Shrivathsava N.L., Tripathi and Kulkarni, "Novel design of VCO with output peak to peak at control", (IJICA), ISSN; 2231-1890 Vol.1 Issue 2, 2011
- [20] R. Rohith Kumar Reddy, N Ramanjaneyule, "high performance CMOS Schmitt Trigger" Vol.2 Issue, July-August 2012, pp.23, 1-2324.
- [21] Aaron Arthurs, Justin Roorck, and jjadi, "A Comparative study of ultra-low voltage digital circuit design," International Solid State Circuit Conference (ISSCC) 2012.
- [22] Swati Kundra, Priyanka Soni. "Low power Schmitt Trigger" ISSN 2222-1727 Vol.3, No.2, 2012.
- [23] Shikha Singh, V. Sclochana Verma, "Crasstalk noise and delay reduction in VLSI interconnects," ISSN No. 2250-3536.Vol.2 ISSUE 2, March 2012.
- [24] Archana nagda, Rajendra's Prasad, N.K. Vyas, "Leakage power reduction techniques; A new approach," ISSN 2248-9622, Vol.2 Issue 2, mar-apr 2012, pp. 308-312.
- [25] Yogeshwar Singh Randhawa and Sanjay Sharma, "Effect of Multi Threshold Techniques on Compretive Study of 11T and 6T Cell during Leakage Power Robustness", Quantum Matter, ISSN; 2164-7515, Vol. 2, pp. 105-108, Issue 2013.
- [26] Tuzun, Burcu, Erkoc, "Structural and Electronic Properties of Unusual Carbon Nanorods", Quantum Matter, ISSN; 2164-7515, Vol. 1, No 2 pp. 136-148, December 2012.
- [27] Paitya, N. Bhattacharya, S. and Ghatak, "Influence of Quantizing Magnetic Field on the Fowler-Nordheim Field Emission form Non-Parabolic Materials", Quantum Matter, ISSN; 2164-7515, Vol. 1, No 1, pp. 63-85, June 2012.