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Data Analysis: Results and Discussion of Different Flip Flop Configurations

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Abstract - ***The design of an efficient and high performance memory element known as Flip-Flop Extension verification is carried out to ascertain its efficiency and effectiveness over the conventional SR and JK Flip Flops. This is achieved through the analysis of the design data of the Flip Flop Extension in comparison with the existing related conventional Flip Flops frameworks to examine and evaluate the significant advantages of the Flip Flops Extension at 87.5% and or 100% active states utilization against SR at 50% and JK at 75% active states utilizations. From the data analysis carried out, the Flip Flop Extension at 87.5% is found suitable to be used as memory element with speed, size and power consumption performance advantage over the conventional SR and JK Flip Flops; while the Flip Flop 'No Rest state' at 100% active state utilization cannot be used to build Storage devices, but they may still be useful in other digital application areas yet to be examined.***

Key Words: *Conventional Flip Flop, Flip Flop Extension, Memory Element, Active State Utilization, Input Combination, and K-Map.*

1. INTRODUCTION

A model of comparison analysis framework through examination of existing related frameworks is used to examine and evaluate the significant advantages of the Flip Flops Extension at 87.5% and or 100% active states utilization over the existing conventional SR and JK Flip Flops that stand at 50% and 75% active state utilization respectively. In all semiconductor memory devices, especially the ones where Flip Flops are employed, a memory element must be constructed from the intended Flip Flops that will have provisions for READ and WRITE commands, SELECT and DATA terminals amongst other requirements. Therefore, two previously designed memory elements known as Flip Flops Extension having their active states utilization at 87.5% and or 100% will be examined.

2. DATA ANALYSIS CHARACTERISTICS OF THE DIFFERENT FLIP FLOPS

The basic memory cell is a Flip-Flop adequately gated. This is analysed as follows with the following input signal requirements:

SELECT input to select a particular location in memory, designated = S_e
WRITE input command, designated = W
DATA input to be written into, designated = I
READ input command, designated = R_e
DATA output to be read from, designated = O

WRITE Command Consideration:
First, let us consider writing (W) into the memory which requires select (S_e) and data (I) inputs using the conventional SR-FF. These three inputs with the previous output of the SR-Flip Flop will determine the input combinations as presented in the various Flip Flops combination Tables under review in this paper.

We should note that under the READ Command Consideration, the "READ input command, designated (R_e) and DATA input to be read from, designated (O)" are not associated with the WRITE Command Consideration in the input Combination Table. These signals are only relevant in a basic memory cell with separate READ and WRITE command consideration.

2.1 Construction of Input Combination Tables

The Table of combination (0-15) in all Flip Flops presented here is obtained as follows:

- From S/N (0-7), the memory space is not selected since $S_e = 0$. Therefore, the Flip Flop will maintain its previous/present values. That is $Q_n = Q_{n+1}$ throughout these portions of the table combination.
- From S/N (8-15), the memory space is selected but anywhere W = 0, nothing will be written into the memory space, hence the Flip Flop will retains its previous/present states

- From S/N (8-15), the memory space is selected but anywhere W = 1, the memory space will receive the contents of the data to be written in 'I'. That is, the next Flip Flop output, Q_{n+1} = 1 which may be different from its previous/present output, Q_n.

3. DATA PRESENTATION AND THE RESULTING DESIGN OF CONVENTIONAL SR-FF AT 50%

Considering using Set and Reset (SR) Flip Flop as Basic Memory Element, the Data Presentation and the Resulting Design of SR-FF at 50% utilization looks similar to that of JK-FF at 75% utilization except for the invalid or inactive states which could be avoided when using this design. This design was established many years back. Tables 1.1 represent the input combination tables for the conventional SR-FF. The resulting memory element is shown in Figure 1(a) with detailed circuit diagram in Figure 1(b).

Table 1.1: Truth Table of a Memory Element on an SR-FLIP FLOP at (50%)

S/N	S_e	I	W	Q_n	Q_{n+1}	$Q_n \rightarrow Q_{n+1}$	S	R	S	R	Q_n	Q_{n+1}
0	0	0	0	0	0	0→0	0	X	0	0	0	0
1	0	0	0	1	1	1→1	X	0	0	0	1	1
2	0	0	1	0	0	0→0	0	X	0	1	0	0
3	0	0	1	1	1	1→1	X	0	0	1	1	0
4	0	1	0	0	0	0→0	0	X	1	0	0	1
5	0	1	0	1	1	1→1	X	0	1	0	1	1
6	0	1	1	0	0	0→0	0	X	1	1	0	X
7	0	1	1	1	1	1→1	X	0	1	1	1	X
8	1	0	0	0	0	0→0	0	X				
9	1	0	0	1	1	1→1	X	0				
10	1	0	1	0	0	0→0	0	X				
11	1	0	1	1	0	1→0	0	1				
12	1	1	0	0	0	0→0	0	X				
13	1	1	0	1	1	1→1	X	0				
14	1	1	1	0	1	0→1	1	0				
15	1	1	1	1	1	1→1	X	0				

SR-FF; at (50%) Basic Memory Element will be active only when SR = 00, 01 & 10

The values of S & R are plotted into their respective K-Maps as shown in Table 1.2 from where the corresponding logic equations 3.1 and 3.2 are derived.

Table 1.2: K-Maps for S&R terminals of SR- Flip Flop (50%)

K-Map for S

S= $S_e I W$ ..... (3.1)

WQ_n \ S_eI	00	01	11	10
00	0^0	0^4	0^{12}	0^8
01	X^1	X^5	X^{13}	X^9
11	X^3	X^7	X^{15}	0^{11}
10	0^2	0^6	1^{14}	0^{10}

K-Map for R

R= $S_e \bar{I} W$ ..... (3.2)

WQ_n \ S_eI	00	01	11	10
00	X^0	X^4	X^{12}	X^8
01	0^1	d^5	0^{13}	0^9
11	0^3	0^7	0^{15}	1^{11}
10	X^2	X^6	0^{14}	X^{10}

When the values of S&R are plotted into their respective K-Maps as shown in Table 1.2 from where the corresponding logic equations **S = S_e. I. W** and **R = S_e.** $\bar{I}$ **.W** are derived, the logic network of Figure 1(a) is obtained.

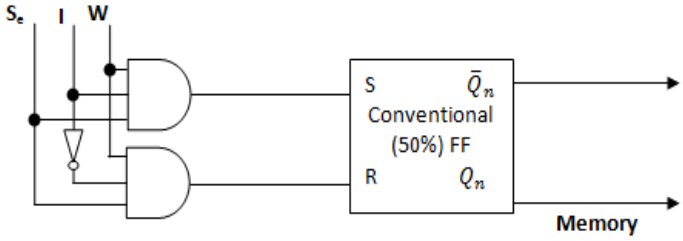

Figure 1a: Basic Memory Element for Conventional 50% SR-FF

The resulting logic circuit diagram of the SR-FF at 50% after adding the design is shown in Figure 1(b) below.

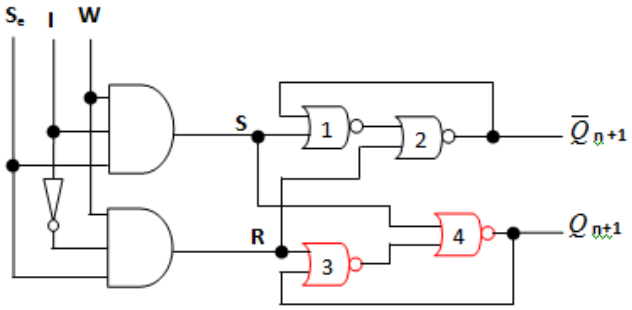

Figure 1(b): Logic Circuit Diagram of Memory Element for JK-FF at 50% utilization

4. DATA PRESENTATION AND THE RESULTING DESIGN OF CONVENTIONAL JK-FF AT 75%

This design was also established many years back and is currently proven as the most widely used memory element for the design of computer storage unit. Table 2.1 represents the input combination table for the conventional JK-FF. The resulting memory element is shown in Figure 2(a) with detailed circuit diagram in Figure 2(b).

Table 2.1: Truth Table of a Memory Element on a JK-Conventional FLIP FLOP (75%)

S/N	S_e	I	W	Q_n	Q_{n+1}	$Q_n \rightarrow Q_{n+1}$	J	K	J	K	Q_n	Q_{n+1}
0	0	0	0	0	0	0→0	0	d	0	0	0	0
1	0	0	0	1	1	1→1	d	0	0	0	1	1
2	0	0	1	0	0	0→0	0	d	0	1	0	0
3	0	0	1	1	1	1→1	d	0	0	1	1	0
4	0	1	0	0	0	0→0	0	d	1	0	0	1
5	0	1	0	1	1	1→1	d	0	1	0	1	1
6	0	1	1	0	0	0→0	0	d	1	1	0	1
7	0	1	1	1	1	1→1	d	0	1	1	1	0
8	1	0	0	0	0	0→0	0	d				
9	1	0	0	1	1	1→1	d	0				
10	1	0	1	0	0	0→0	0	d				
11	1	0	1	1	0	1→0	d	1				
12	1	1	0	0	0	0→0	0	d				
13	1	1	0	1	1	1→1	d	0				
14	1	1	1	0	1	0→1	1	d				
15	1	1	1	1	1	1→1	d	0				

JK-Conventional FLIP FLOP (75%)

The values of J & K are plotted into their respective K-Maps as shown in Table 2.2 from where the corresponding logic equations 4.1 and 4.2 are derived.

Table 2.2: K-Maps for J & K terminals of JK-Conventional Flip Flop (75%)

K-Map for J					K-Map for K				
J= S_eIW ..... (4.1)					K = $S_e\bar{I}W$ ..... (4.2)				
	S_eI					S_eI			
WQ_n	00	01	11	10	WQ_n	00	01	11	10
00	0^0	0^4	0^{12}	0^8	00	d^0	d^4	d^{12}	d^8
01	d^1	d^5	d^{13}	d^9	01	0^1	0^5	0^{13}	0^9
11	d^3	d^7	d^{15}	d^{11}	11	0^3	0^7	0^{15}	1^{11}
10	0^2	0^6	1^{14}	0^{10}	10	d^2	d^6	d^{14}	d^{10}

Using the input-output equations related to JK Flip-Flops from the K-map analysis of Table 2.2, the circuit diagrams of a memory element logic unit can be designed as shown in Figures 2(a) and 2(b).

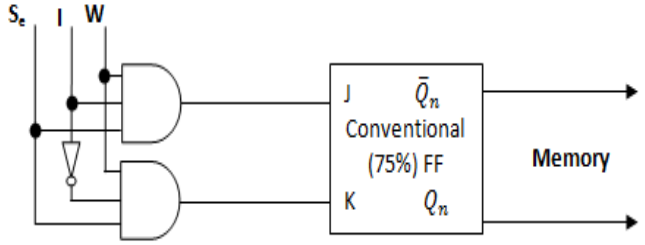

Figure 2(a): Block Diagram of Memory Element for JK-FF at 75% utilization

Figure 2b shows the complete circuit diagram of the memory element of JK-FF at 75% active states that is obtained from the combination of the Flip Flop design with the Read/Write data analysis construction of Tables 2.1.

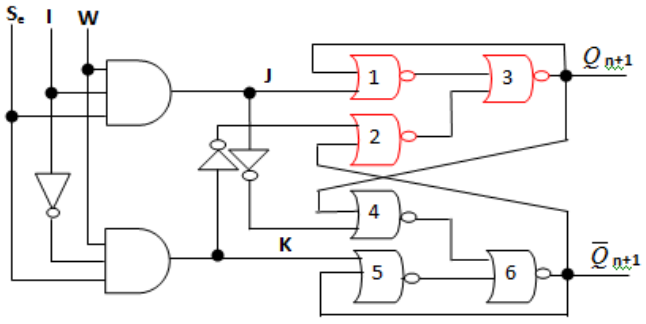

Figure 2(b): Logic Circuit Diagram of Memory Element for JK-FF at 75% utilization

5. DATA PRESENTATION AND THE RESULTING DESIGN OF JK-FF EXTENSION-0 AT 87.5%

Let us now consider the modified (JK-Flip Flops known as Flip Flop Extension – 0) as depicted in Table 3.1 using the same analysis technique adopted for conventional JK-FF at 75% active state utilization.

Table 3.1: Truth Table of a Memory Element on a JK-FF extension -0; One Rest at (87.5%)

S/N	S_e	I	W	Q_n	Q_{n+1}	$Q_n \rightarrow Q_{n+1}$	J	K
0	0	0	0	0	0	0→0 ⟶	0	d
1	0	0	0	1	1	1→1 ⟶	1	0
2	0	0	1	0	0	0→0 ⟶	0	d
3	0	0	1	1	1	1→1 ⟶	1	0
4	0	1	0	0	0	0→0 ⟶	0	d
5	0	1	0	1	1	1→1 ⟶	1	0
6	0	1	1	0	0	0→0 ⟶	0	d
7	0	1	1	1	1	1→1 ⟶	1	0
8	1	0	0	0	0	0→0 ⟶	0	d
9	1	0	0	1	1	1→1 ⟶	1	0
10	1	0	1	0	0	0→0 ⟶	0	d
11	1	0	1	1	0	1→0 ⟶	d	d
12	1	1	0	0	0	0→0 ⟶	0	d
13	1	1	0	1	1	1→1 ⟶	1	0
14	1	1	1	0	1	0→1 ⟶	1	d
15	1	1	1	1	1	1→1 ⟶	1	0

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	**1**
1	1	1	0

JK- FF Extension – 0; One rest at 87.5%

The values of J & K are plotted into their respective K-Maps as shown in Table 4.1 from where the corresponding logic equations 5.1 and 5.2 are derived and the logic circuit diagram of the memory element cell is shown in Figures 3(a) and 3(b).

Table 4.1: K-Maps for J & K terminals of JK-FF Extension – 0; Rest (87.5%)

K-Map for J					K-Map for K				
J= S_eIW + Q_n ..... (5.1)					K = 0 ..... (5.2)				
	S_eI					S_eI			
WQ_n	00	01	11	10	WQ_n	00	01	11	10
00	0^0	0^4	0^{12}	0^8	00	d^0	d^4	d^{12}	d^8
01	1^1	1^5	1^{13}	1^9	01	0^1	0^5	0^{13}	0^9
11	1^3	1^7	1^{15}	d^{11}	11	0^3	0^7	0^{15}	d^{11}
10	0^2	0^6	1^{14}	0^{10}	10	d^2	d^6	d^{14}	d^{10}

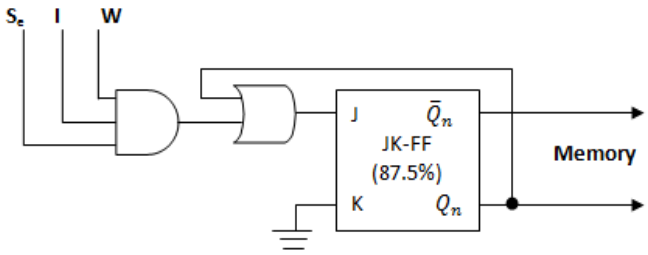

Figure 3(a): Block Diagram of Memory Element for JK-FF Extension – 0 at 87.5% utilization

Shown in Figure 3b is the logic circuit diagram of memory element of JK-FF Extension – 0 at 87.5% active states as obtained from the combination of the design Flip Flop with the Read/Write data analysis construction of Table 3.1.

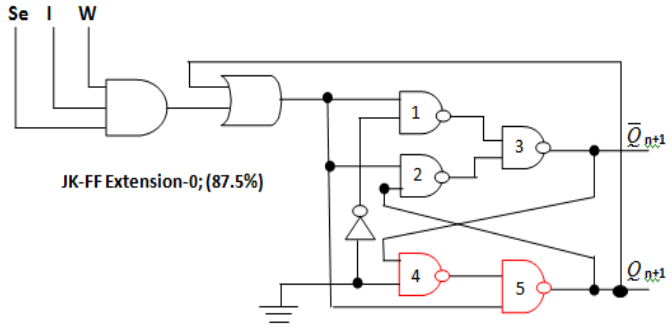

Figure 3(b): Logic Circuit Diagram of Memory Element for JK-FF Extension – 0 at 87.5% utilization

6. DATA PRESENTATION AND THE RESULTING DESIGN OF JK-FF EXTENSION-1 AT 87.5%

Tables 5.1 contains the data employed to design the memory element using (JK-Flip Flops Extension – 1) 'One Rest' Flip Flop at 87.5% active state utilization.

Table 5.1: Truth Table of a Memory Element on a JK-FF extension -1; One Rest at (87.5%)

S/N	S_e	I	W	Q_n	Q_{n+1}	$Q_n \rightarrow Q_{n+1}$	J	K		J	K	Q_n	Q_{n+1}
0	0	0	0	0	0	0→0	0	1		0	0	0	1
1	0	0	0	1	1	1→1	d	0		0	0	1	1
2	0	0	1	0	0	0→0	0	1		0	1	0	0
3	0	0	1	1	1	1→1	d	0		0	1	1	1
4	0	1	0	0	0	0→0	0	1		1	0	0	1
5	0	1	0	1	1	1→1	d	0		1	0	1	1
6	0	1	1	0	0	0→0	0	1		1	1	0	1
7	0	1	1	1	1	1→1	d	0		1	1	1	0
8	1	0	0	0	0	0→0	0	1		JK- FF Extension – 1; One rest at 87.5%			
9	1	0	0	1	1	1→1	d	0					
10	1	0	1	0	0	0→0	0	1					
11	1	0	1	1	0	1→0	d	1					
12	1	1	0	0	0	0→0	0	1					
13	1	1	0	1	1	1→1	d	0					
14	1	1	1	0	1	0→1	d	d					
15	1	1	1	1	1	1→1	d	0					

The values of J & K are plotted into their respective K-Maps as shown in Table 5.2 from where the corresponding logic equations 6.1 and 6.2 are derived.

Table 5.2: K-Maps for J & K terminals of JK-FF Extension – 1; Rest (87.5%)

K-Map for J					K-Map for K				
J= 0.....(6.1)					$K = \bar{Q}_n + S_e\bar{I}W$.....(6.2)				
	S_eI					S_eI			
WQ_n	00	01	11	10	WQ_n	00	01	11	10
00	0^0	0^4	0^{12}	0^8	00	1^0	1^4	1^{12}	1^8
01	d^1	d^5	d^{13}	d^9	01	0^1	0^5	0^{13}	0^9
11	d^3	d^7	d^{15}	d^{11}	11	0^3	0^7	0^{15}	1^{11}
10	0^2	0^6	d^{14}	0^{10}	10	1^2	1^6	d^{14}	1^{10}

Using the input-output equations related to JK Flip-Flops from the K-map analysis of Table 5.1, the circuit diagrams of a memory element logic unit can be designed as shown in Figures 4(a) and 4(b) on JK-FF Extension – 1 at 87.5% 'One Rest' using only NAND gates.

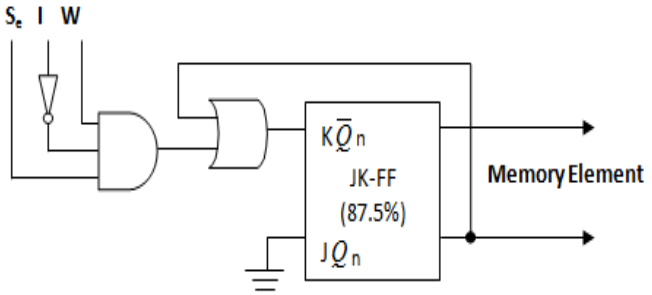

Figure 4(a): Block Diagram of Memory Element for JK-FF Extension – 1 at 87.5% utilization

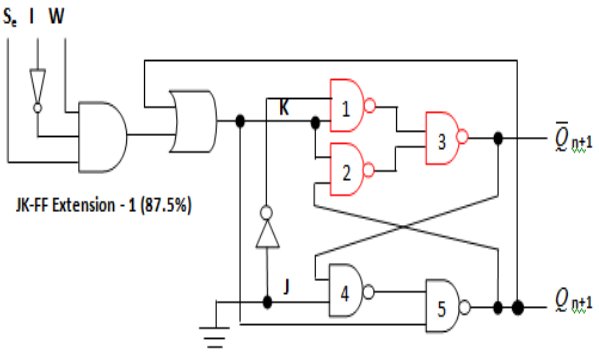

Figure 4(b): Logic Circuit Diagram of Memory Element for JK-FF Extension – 1 at 87.5% utilization

7 DATA PRESENTATION AND THE RESULTING DESIGN OF XY-FF EXTENSION AT 100%

Similarly, the same analysis is repeated for XY-FF-No Rest at 100% as presented in Table 6.1.

Table 6.1: Truth Table of a Memory Element on an XY-FLIP FLOP at (100%)

S/N	S_e	I	W	Q_n	Q_{n+1}	$Q_n \rightarrow Q_{n+1}$	X	Y		X	Y	Q_n	Q_{n+1}
0	0	0	0	0	0	0→0	0	1		0	0	0	1
1	0	0	0	1	1	1→1	1	0		0	0	1	0
2	0	0	1	0	0	0→0	0	1		0	1	0	0
3	0	0	1	1	1	1→1	1	0		0	1	1	0
4	0	1	0	0	0	0→0	0	1		1	0	0	1
5	0	1	0	1	1	1→1	1	0		1	0	1	1
6	0	1	1	0	0	0→0	0	1		1	1	0	1
7	0	1	1	1	1	1→1	1	0		1	1	1	0
8	*1*	*0*	*0*	*0*	*0*	*0→0*	*0*	*1*		*XY-FF; No Rest (100%)*			
9	*1*	*0*	*0*	*1*	*1*	*1→1*	*1*	*0*					
10	*1*	*0*	*1*	*0*	*0*	*0→0*	*0*	*1*					
11	*1*	*0*	*1*	*1*	*0*	*1→0*	*d*	*d*					
12	*1*	*1*	*0*	*0*	*0*	*0→0*	*0*	*1*					
13	*1*	*1*	*0*	*1*	*1*	*1→1*	*1*	*0*					
14	*1*	*1*	*1*	*0*	*1*	*0→1*	*d*	*d*					
15	*1*	*1*	*1*	*1*	*1*	*1→1*	*1*	*0*					

The values of X & Y are plotted into their respective K-Maps as shown in Table 6.2 from where the corresponding logic equations 7.1 and 7.2 are derived.

Table 6.2: K-Maps for X & Y terminals of XY-FF; No Rest at 100%

K-Map for X					K-Map for Y				
X= Q_n ..... (7.1)					Y = $\bar{Q}_n$..... (7.2)				
	S,I					S,I			
WQ,	00	01	11	10	WQ,	00	01	11	10
00	0^0	0^4	0^{12}	0^8	00	1^0	1^4	1^{12}	1^8
01	1^1	1^5	1^{13}	1^9	01	0^1	0^5	0^{13}	0^9
11	1^3	1^7	1^{15}	d^{11}	11	0^3	0^7	0^{15}	d^{11}
10	0^2	0^6	d^{14}	0^{10}	10	1^2	1^6	d^{14}	1^{10}

NOTE:

From Table 6.2, it can be seen that X and Y are equal to Q_n and $\overline{Q}_n$ respectively. This configuration cannot be used to design **basic memory element** because the logic equations (7.1) & (7.2) are not functions of the required inputs (S_e, I & W) which are to be used to SELECT (S_e) the desired location, to WRITE (W) the required DATA (I) into a storage device. Hence, the configuration cannot be used as a storage device.

8 SUMMARY OF MEMORY ELEMENTS DESIGN

The summary of Basic Memory Elements of all the different Flip Flop Configurations with respect to memory cell characteristics as analyzed in this paper is presented in Table 7.1.

Table 7.1: Summary of the Different Memory Element Designs

S/N	TYPE OF FLIP FLOPS	STORAGE DEVICE
1.	Basic Memory Element made of SR-FF will be active only when SR = 00, 01 & 10 (50%)	This is the conventional SR-FF used to build Storage Media
1.	JK-000, 001 Rest (75%)	This is the conventional JK-FF used to build Storage Media
2.	JK-FF Extension – 0; One Rest (87.5%)	This can be used to build Storage Media
3.	JK-FF Extension – 1; One Rest (87.5%)	This can be used to build Storage Media
4.	XY-FF; No Rest (100%)	This cannot be used to build Storage Media

NOTES:

1. Though XY-Flip Flops; No Rest at 100% cannot be used to build Storage Devices, but they may still be useful in other digital application areas yet to be examined. This is beyond the scope of this paper.
2. JK-FF Extension – 0 and JK-FF Extension – 1 Flip Flops; One Rest at 87.5% as Memory Elements component parts may have speed advantage over SR/JK-Conventional Flip Flops when the number of transitions required to complete a propagation route in Flip Flop configuration is examined or compared. Comparative performance analysis of the different Flip Flop configurations is a future research area to be looked into.

9. CONCLUSION

From our analysis in this paper, it is evidence that JK Flip Flop Extension with resting state at 87.5% active state utilization can be used to build storage media at enhanced speed performance because the gates involved in the design is fewer than those used in the design of conventional Flip Flops; while the Flip Flop 'No Rest state' at 100% active state utilization cannot be used to build storage devices, but they may still be useful in other digital application areas yet to be examined. Efforts should be geared towards investigating the of XY-Flip Flops at 100% active states utilization in other to ascertain their usefulness in digital device applications since it has been confirmed in this paper that they cannot be used to build Computer Storage Devices.

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