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REVIEW ON 2:4 DECODER BY REVERSIBLE LOGIC GATES FOR LOW POWER CONSUMPTION

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Abstract - ***In day today world, as the technology is developing so rapidly the designing of the systems are becoming more and more compact. In some systems even if the circuits are not compact; still there is a need of less power consumption. In a microprocessor/ microcontroller based systems, the most commonly used block is the instruction set decoder. Hence; it will be not wrong if we say the instruction set decoder consumes more power. Thus optimizing the power of this block will be helpful to reduce the overall power consumption of the system. Thus proposed plan for this paper is the use of reversible logic gate based design to reduce power consumption of instruction decoder. Reversible logic gates work on the principle; that only buffers are used for implementation. A buffer consumes less amount of power when compared to normal CMOS gates. Combination of buffers to form logic gates will consume a minimal amount of power when compared with normal CMOS based implementation. Thus using reversible gates in construction of instruction decoder will consume less amount of power as compared to normal CMOS based gates design.***

Keywords - *Logical Gates, Decoder, Reversible logic, Reversible gates.*

1. Introduction

Now a day's power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. Chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products. Decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. Applications of decoders are wide; they include data de-multiplexing, memory address decoding, seven segment display etc. A decoder is a simple circuit that converts a code into a set of signals. It is named as decoder because it changes the big coded data into different simple combinations which can be used to drive any signal, but we will begin our study of encoders and decoders because they are simpler to design. Active instructions occur only within a sub-set of all instructions.

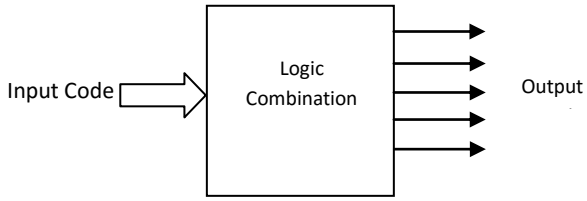

Fig: Conceptual Diagram of Decoder

A common type of decoder is the line decoder which takes an n-digit binary number and decodes it into 2^n data lines. The simplest is the 1-to-2 line decoder.

1.1 Reversible Gates

In a reversible logic gate there is always a unique input associated with a unique output and vice versa. When reversible gates operates; they never erase any information, and consequently, a computation based on reversible logic can be run forward to obtain an answer, the answer copied, and then the whole computation undone to recover all the energy expended apart from the small amount used to copy the answer at the mid-way point.

Reversible logic synthesis is the basis of quantum information technology. According to the reversible network's no fan-out and no feedback constraint condition and limitation, reversible logic synthesis is to use reversible logic gate given to implement the relevant reversible logic network meanwhile make the cost as low as possible. Reversible logic gate cascade is one of the key issues of the reversible logic synthesis. Reversible logic gate network is the number of the input and output are equal and input vectors and output vectors are one to one mapping reversible logic gate collection. Therefore, the input vectors state can only be reconstructed by the output vectors, which are described by the way of the function as following: the function is reversible, if every input vectors of function can only be mapped by only one output vector. An *n* variables reversible function can also be defined as integer set {0, 1, *n*, 2*n* *1} self-mapping.

Reversible logic synthesis is the important aspects of the reversible computing research meanwhile reversible logic synthesis is the basis of quantum information technology. According to the reversible network's no fan-out and no feedback constraint condition and limitation, reversible logic synthesis is to use reversible logic gate given to implement the relevant reversible logic network meanwhile make the cost as low as possible. Reversible logic gate cascade is one of the key issues of the reversible logic synthesis. Reversible logic gate network is the number of the input and output are equal and input vectors and output vectors are one to one mapping reversible logic gate collection. Therefore, the input vectors state can only be reconstructed by the output vectors, which are described by the way of the function as following: the function is reversible, if every input vectors of function can only be mapped by only one output vector. An *n* variables reversible function can also be defined as integer set {0, 1, *n*, 2*n* *1} self-mapping.

1.2 NOT GATE

Reversible logic gate's simplest example is the NOT gate. It simply inverts the bit value it handles**.** Not gate is 1-input/1-output gate.

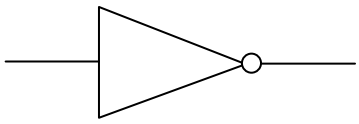

Fig: NOT Gate

1.3 SWAP GATE

Swap Gate simply exchanges the bit values given at input**.** In quantum computing it is not compulsory that a circuit may have any physical wires connecting the gates together. Instead a circuit can be merely a visual specification of a sequence of gate operations with time increasing from left to right in the circuit diagram as successive gates are applied.

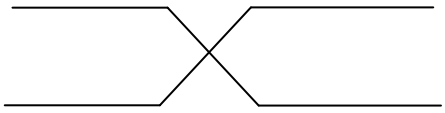

Fig: Swap Gate

1.4 CNOT GATE

A reversible gate of considerable importance in quantum computing is the 2-bit controlled-NOT gate (CNOT). The effect of the "controlled" NOT gate is to flip the bit value of the second bit if and only if the first bit is set to 1.

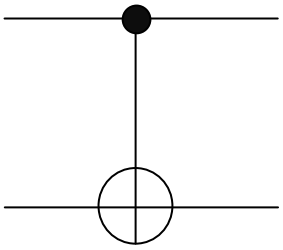

Fig: CNOT Gate

Thus by using such reversible gates we can make the power consumption to reduce. As compared to the general logical gates; if we design any circuits with the reversible gates the resultant power will always be less than that of logical gates.

2. Literature Review

Ritajit Majumdar [1] In her article proposed a novel design of 2:4 decoders and has used it to build a 3:8 decoder. The quantum cost of an n: 2n decoder will reduce by use of their 2:4 decoder blocks. As for n input signals, the number of output signal will be 2n, still the increase in the number of gates will be linear in respect to the number of output signals. She also conclude that; use of other gates such as TR gate, Peres, or Toffoli gate the number of gates will be twice as high also the quantum cost will be nearly doubled. In the same manner the number of garbage outputs for all these gates also increases. Since every Fredkin gate has one garbage output; according to the author the design proposed in her paper cannot be optimized further by using the basic gates like Peres, Toffoli or TR gates.

Landauer [2] showed that the heat generated during computation is not due to the processing of bits, but due to the loss of information. Wiping of each bit of information causes a kTln2 amount of heat dissipation where k is the Boltzmann constant = 1.3805 _ 10^23 J/K and T is the temperature in absolute scale. While this heat may be negligible for a single wipe of information, in modern VLSI design, where many chips are arranged in small region and millions of instructions are processed per second, the information loss and consequently the heat generation is formidable.

Bennett [3] later showed that this heat dissipation can be avoided by using reversible computation. This proof by Bennett has led to an extensive research on reversible logic theory. The most prominent applications of these logics are seen in quantum computation, DNA computing, nanotechnology and low power CMOS design. Quantum logic gates are used to compose Quantum Networks- each gate performing an elementary unitary operation on one, two or more than two state quantum systems called qubits. Each qubit represents an elementary unit of information corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum

arithmetic must be built from reversible logic components. Quantum cost, delay, number of constant inputs and garbage outputs are the most important cost metrics of reversible computing [3]. The outputs which are present only to maintain reversibility and do not perform any useful operations are called as Garbage outputs. Number of gates is not a good measure of cost, since more than one gates can be taken together to form a new gate, thus reducing the gate count.

Wu-An Kuo, TingTing Hwang, and Allen C.-H. Wu [4] they evaluated the effectiveness of power reduction on the Power stone benchmarking set for instruction decoding method. He used Synopsys Prime Power to compute the power dissipation (both dynamic and leakage power dissipation). The simulation was done on ARM Verilog code at the speed of 20MHz. Then the switching activities were fed into Prime Power to calculate power consumption. The results show that the proposed instruction-decoding method achieves on an average of 26.71% in power reduction as compared to the original instruction decoder and 15.69% improve.

Vanshikha Singh and Rajesh Mehra [5] stated the DA formulation employed for two separate blocks weight update block and filtering operations they demonstrated that the area is reduced in the full custom design of the decoder circuit from standard cell layout and the semi custom based layout of the decoder. The power is reduced in the semi custom design from standard cell layout but increased in the full custom design.

Mohammed H. A. Khan[6] In his paper "Reversible Realization of Quaternary Decoder, Multiplexer, and Demultiplexer Circuits" DA formulation employed for two separate blocks weight update block and filtering operations requires larger area and is not suited for higher order filters therefore causes reduction in the throughput. These problems have been overcome by efficient distributed formulation of Adaptive filters. LMS adaptation performed on a sample-by-sample basis is replaced by a dynamic LUT update using a weight update scheme [6].

Ranjan Kumar Singh, and Rakesh Jain[7] In their proposed design, they achieved low power consumption after applying adiabatic techniques on 2:4 decoder designed circuit for high-performance DSP applications and integrated circuits. 2:4 decoder circuits were designed using LOGICAL GATES into MOS. Their proposed 2:4 decoder provides noticeable consumption in power and high speed operation. In this paper they've achieved less power consumption in 2:4 decoder circuits than conventional decoder design.

K.V Manoj and M.Amarnath Reddy [8] in there paper they presents the primitive reversible gates that are gathered from the references and made the adder as an application of Reversible gates. Their paper led to extend towards the digital style development mistreatment reversible logic circuits with pass junction transistor logic which helps to form an occasional power circuits.

3. Proposed Work

In this paper we will be proposing the design of 2:4 Decoder with the use of Reversible Gates to reduce the power of the decoder and also this will help in power reduction of the overall system. The figure given below gives the concept of reducing power of the system.

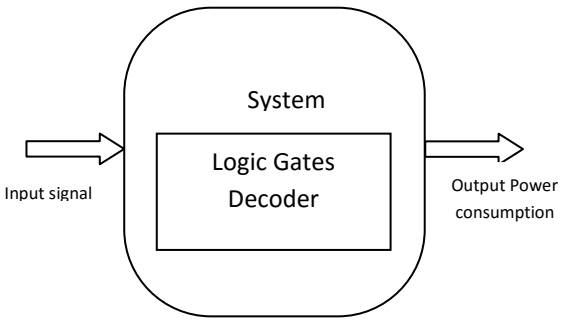

Fig: Power consumption of System using simple Decoder

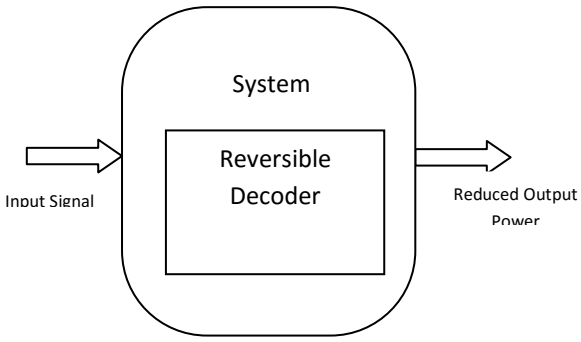

Fig: Reduced Power consumption of System using Reversible Decode

The main objective for this paper is to design a low power decoder which will definitely reduce the power consumption of whole system.

4. Conclusion

From the above proposed plan it can be expected to achieve less delay, and also reduced number of gates. It might happen that the area for the design will increased but the main purpose is to reduce the power which will definitely work using this design. Also; it is possible that if the power is reduced then the temperature will also get reduced. Thus we propose the above design for low power consumption for decoders.

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BIOGRAPHIES

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