International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 04 | April-2016 www.irjet.net p-ISSN: 2395-0072

Phase Locked Loop Design for Fast Phase and Frequency Acquisition

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Abstract--- The specific property of fast locking of PLL is required in many clock and data recovery circuits. The most versatile application of the phase locked loops (PLL) is for clock generation and clock recovery in microprocessor, networking, communication systems, and frequency synthesizers. Phase locked-loops (PLLs) are commonly used to generate well-timed on-chip clocks in high performance digital systems. Modern wireless communication systems employ Phase Locked Loop (PLL) mainly for synchronization, clock synthesis, skew and jitter reduction. Because of the increase in the speed of the circuit operation, there is a need of a PLL circuit with faster locking ability. Hence there is a necessity of a PLL which must operate in the GHz range with less lock time. This paper presented a PLL with redesigning of individual blocks. The PLL is designed using 180 nm CMOS technology for high performance with 1.8 V power supply.

Keywords--- Phase Locked Loop (PLL), Phase Frequency Detector (PFD), Charge Pump (CP), Low Pass Filter (LPF), Voltage Controlled Oscillator (VCO)

I. INTRODUCTION

A Phase Locked Loop (PLL) is a closed loop feedback system that sets a fixed phase relation between its output clock phase and reference clock phase. It is the heart of the many modern electronics as well as communication systems. The time at which PLL's output frequency matches the input frequency is known as locking time of PLL. This fast locking property is required in many clock and data recovery circuits. A plenty of the researches have been conducted on the redesign of phase locked loop (PLL) circuit and still the research is going on this topic. Most of the researches have conducted to realize a higher lock range PLL with lesser lock time and have tolerable phase noise. PLLs find wide application in several modern applications mostly in advance communication and instrumentation systems. In this work mainly the faster locking of the PLL is concentrated by properly choosing the circuit architectures and parameters. The optimization of the VCO circuit is also carried out in this work to get a better frequency precision. This paper presents a PLL with designing of each block to achieve fast locking time with reduced power consumption, less jitter and phase noise.

II. BASICS OF PLL

A PLL is a feedback system as shown in figure1, compares the output signal with the input signal. The comparison is performed by a phase frequency detector.

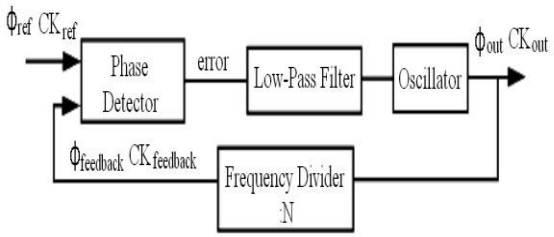


Fig 1: Block diagram of Phase Locked Loop

The basic building blocks of a Phase locked Loop (PLL) are Phase frequency detector (PFD), Charge Pump (CP), Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO) in a feedback loop through a frequency divider. The role of phase frequency detector is to generate a digital signal (difference or error signal) which drives the charge pump to either increase the control voltage of the VCO or decrease it or keep it without change. The charge pump then converts this digital signal into an analog signal. This analog signal has high frequency signal as well as low frequency signal. Then this high frequency signal is filtered out by a low pass filter and applied to the voltage controlled oscillator. This VCO output frequency is divided by the divider N.

III. IMPLEMENTATION OF PLL

A. Phase frequency detector (PFD):

PFD compares the phase and frequency of the two input signals and generates an error signal which is proportional to the phase deviation between them. It detects both phase and frequency differences. Depending upon the phase and frequency deviation, it generates two output signals. If there is a phase difference between the two signals, it generates "UP" or "DOWN" synchronized signals. The block diagram of PFD is as shown in figure2 below.

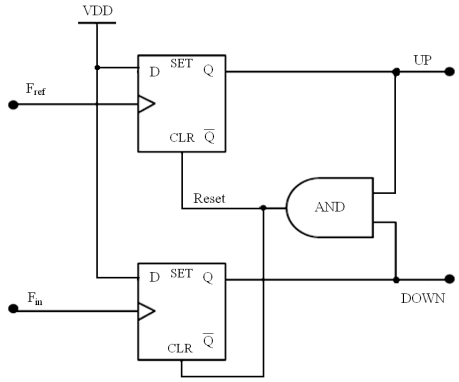


Fig 2: Block diagram of traditional PFD

B. Charge pump & Loop filter:

The Charge pump circuit converts the phase or frequency difference information into a voltage. It is used to combine both the outputs of the PFD and give a single output which is fed to the input of the filter. It gives a constant current. The low pass filter converts undesirable high-frequency (ac) components to desirable dc components. Thus, provides a steady control voltage or the dc level to operate the VCO. The schematic diagram of the charge pump circuit with loop filter is shown in the figure3 below.deviation between them. It detects both phase and frequency differences. Depending upon the phase and frequency deviation, it generates two output signals. If there is a

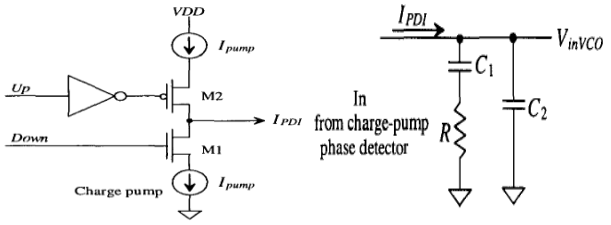


Fig 3: Loop filter with Charge pump

C. Voltage Controlled Oscillator (VCO):

The voltage controlled oscillator is the circuit block where the control voltage of CP controls the oscillator's output frequency so that it matches the reference signal frequency. The Schematic diagram of

Current starved voltage controlled oscillator (CSVCO) is as shown in the figure4 below.

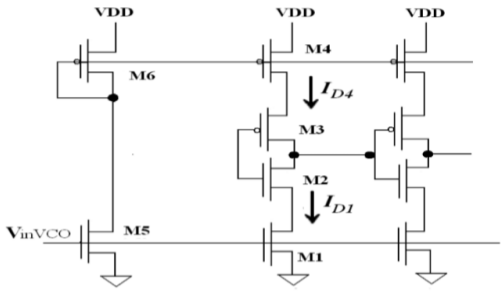
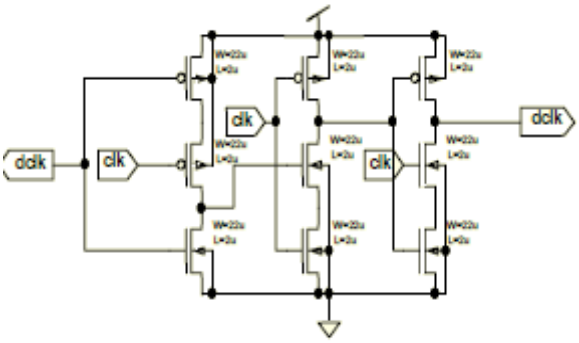


Fig 4: Schematic diagram of CSVCO

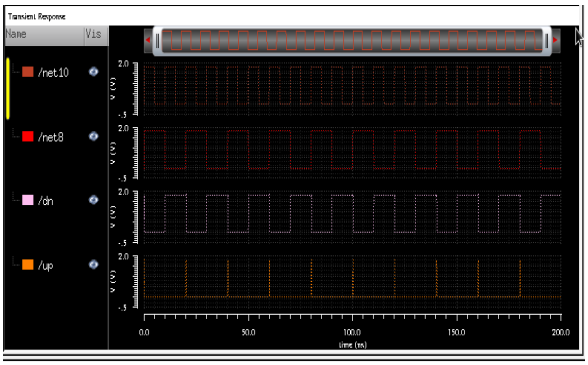
D. Frequency Divider:

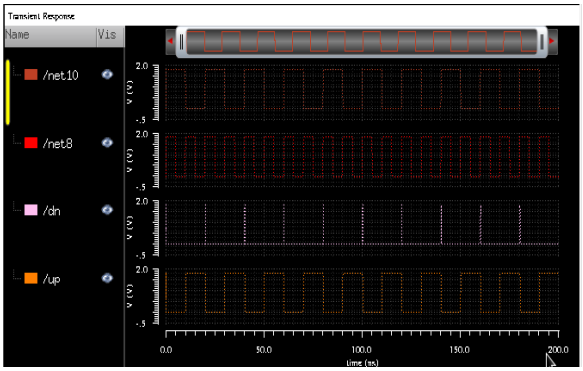
The frequency divider in the PLL circuit forms a closed loop. It scales down the frequency of the VCO output signal. The output of the VCO has to be divided before it is fed back to the input of the PLL. It divides the reference clock signal by N and provides an output pulse signal for every N cycles of reference clock signal. The frequency divide-by-2 counter is as shown in the figure5 below.



IV. SIMULATION RESULTS

The outputs of Phase Frequency Detector are as shown below:



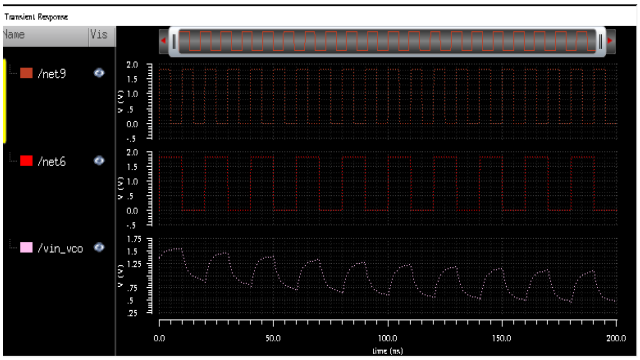


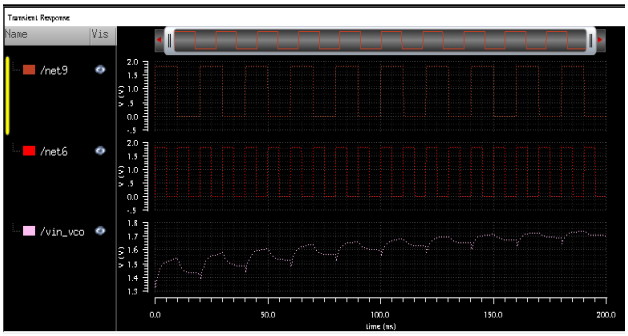
To achieve good PLL performance a charge pump is proposed which has following characteristics:

- Increased output voltage.
- This charge pump show charging waveform when UP signal is high and discharging when DOWN signal triggers high.
- Low Power consumption.

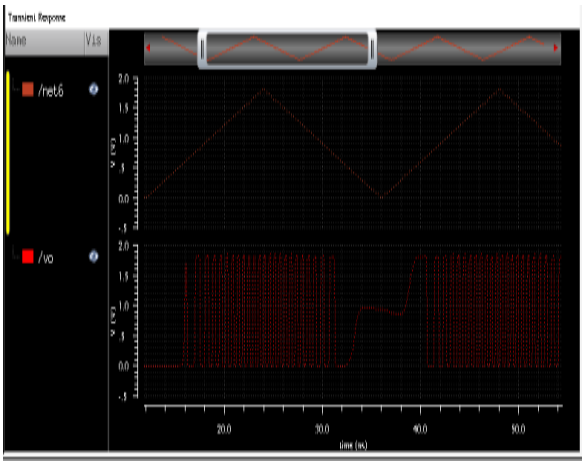
The outputs of Charge pump with loop filter are as below:

Fig 5: Frequency divide-by-2





The output of vco is shown below:



The output of frequency divider is shown below:

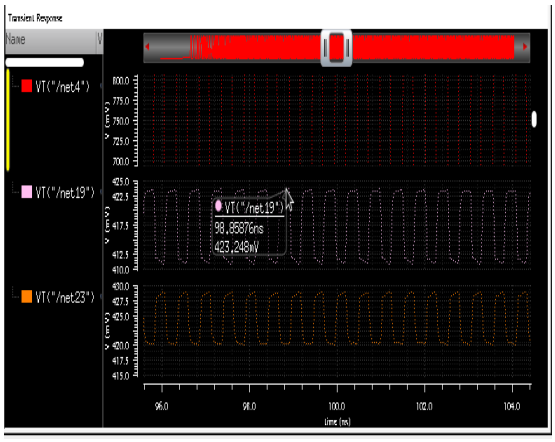


TABLE 1: PLL DESIGN PARAMETERS

Pll design speciations And parameters	value
Power supply	1.8v
Divider circuit	By 2
Charge pump current	600 uA
Capacitor c1	15pf
Capacitor c2	1.5pf
Resistor	1 kΩ
Technology	180 nm
Lock range	100 MHZ
Lock time	280.6ns

Thus by combining all these individual blocks a PLL is proposed which has following properties:

- Very less locking time
- Low power consumption
- Less Delay
- Reduced phase noise
- Less Jitter

CONCLUSITION

In this paper, the fast locking and low power PLL has been designed and simulated using Gpdk 180 nm technology of cadence tool for analysis of phase and frequency. For these specific properties of PLL a charge pump of current mirrored power consumption is used with appropriate parameters of PFD, LPF and VCO. Thus the PLL is designed with a very less locking time of 250.6ns and it is observed to consume a power of 11.0mW.

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