International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 05 | May-2016 www.irjet.net p-ISSN: 2395-0072

IMPLEMENTATION OF A FULLY FUNCTIONAL MEMORY CONTROLLER ARCHITECTURE FOR A XILINX FPGA

Abhilash C N[1], Ramana Reddy K V[2], Amaresha S Khasabag[3]

[1]*PG Scholar, Digital Electronics, VTU, VTU Extension Centre UTL technologies LTD, Bangalore*

[2] *Assistant Professor, VTU Extension Centre UTL technologies LTD, Bangalore*

[3] *Assistant Professor, VTU Extension Centre UTL technologies LTD, Bangalore*

Abstract-*In computers the word memory refers to the computer hardware device, which can be used to accumulate information data for direct access within the computer. A memory controller is a digital design that manages the flow of data going in and out of the memory devices which are in contact with the controller. DoubleDataRateSynchronousDynamicRandomAccessMemory (DDRSDRAM) which is widely used memory duetoitsspeedburstaccessandpipelinefeatures and hence due to these features it isthemost commonly used memoryincomputers. This paper describesaDDRSDRAM controller that can be used to create the command signals which are necessary for memory refresh, read and write operations.Thedesign of the controller isdonein a verilog HardwareDescriptionLanguage (HDL)and the tool used to simulate the verilog code is Xilinx Integrated Synthesis Environment (ISE) DesignSuite14.2.*

Keywords-Memory, Memory controller, FPGA, Xilinx ISE, Verilog HDL.

1. INTRODUCTION

TheDDRSDRAMwhich is usually called asDDR,increasesthebandwidthofthememoryby a factor of two because, it transfers two data'sper clock cycle i.e. on both the positiveandnegativeedgesoftheclocksignal. TheDDR isacomplete synchronousimplementationofcontroller hence it is assigned the name Synchronous DRAM (SDRAM).

The designed memory controller contains the logic which is required to read and write a Dynamic Random Access Memory (DRAM) and also the logic needed to perform the refresh operation of the DRAM. The refresh logic is required because the DRAM is made up of only one transistor and a capacitor. Thus, constant refreshes of DRAM is necessary, if constantly not refreshed the DRAMdrops the information data written to it. This happens because the capacitor continuously loses its charge hence the data will be lost and in a short duration the stored information data will be vanished. Hence, there is a need for refresh in these kinds of dynamic memories.

Double Data Rate (DDR) memory controllers are more complex than the Single Data Rate (SDR) controllers, but the added advantage in the DDR controllers is that, this controller can transfer two data's in the same time where the SDR controller can transfer only one data. This can be achieved by not compromising the memory cell's clock speed or the width of the bus. But this advantage comes at the cost of larger hardware requirement when compared to SDR controller [4].

The Xilinx ISE design suite 14.2 is used to write the verilog codes for the memory controller which is compatible only for the FPGA produced by Xilinx. Hence, Spartan-3E FPGA is selected which incorporates a DDR SDRAM interface, while designing the controller in the tool using verilog coding.

2. BLOCK DIAGRAM

The block diagram in Figure 1shows the top level view of the controller when interfaced to a FPGA and an external memory. The controller gets the input signals from the FPGA system interface and using it, it generates certain signal for the external memory by which the read, write operations are controlled. The various input and output signals of the controller are: clk, reset_n, sys_add sys_adsn, sys_r_wn,sys_dmsel, sys_dly_200us are inputs to the controller and sysd_rdyn, sys_init_done, ddr_csn, ddr_rasn, ddr_casn, ddr_wen, ddr_cke, ddr_add, ddr_ba, ddr_dqm are the prime outputs of the controller. The signals sysd, ddr_dq and ddr_dqs act as both input and output to the controller.

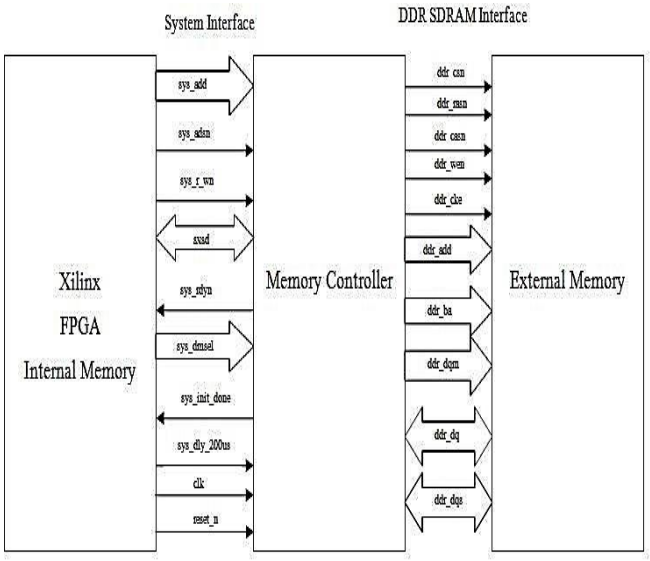

Figure 1 Block Diagram of Controller Showing the Interface with the FPGA and External Memory.

3. MEMORY CONTROLLER ARCHITECTURE

The memory controller architecture as shown in Figure 2 comprises three main components.

1. Main Control Module: It is designed by using two state machines which generate states for the other two modules of the controller. Based on these states the signals for the memory are generated. The module also controls the read, write and refresh operation depending on the outputs of the state machine. Hence it is assigned the name main control module.
2. Signal Generation Module: It generates the signals necessary to select a particular address in the memory. Using these signals whether to perform read or write operation on the memory is decided. The signals by this module is generated based the inputs from the main control module.
3. Data Path Module: The data path module as the name indicates provides a data path between the FPGA and the external memory. This module gets the inputs from the command FSM of the main control module using which it decides either to read or write the data i.e. based on the outputs of the previous module it selects either the read data path or the write data path.

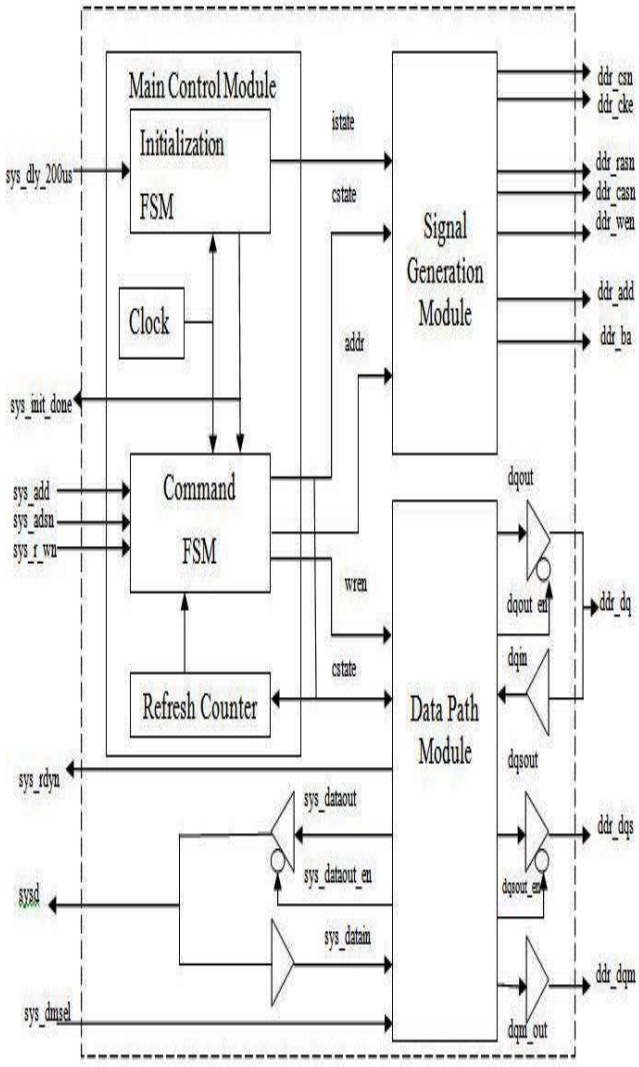

Figure 2 Memory Controller Architecture.

4. RESULTS

The simulation result for the designed architecture of the memory controller obtained from the Xilinx ISE 14.2 tool is given in Figure 3. The Figure 4 shows the top level RTL schematic and the complete schematic of the design showing all the internal blocks in the design is depicted in the Figure 5. The Table 1 gives the device utilization summary report which is also obtained from the Xilinx tool for the selected Spartan 3E FPGA for whichthe device is targeted on.

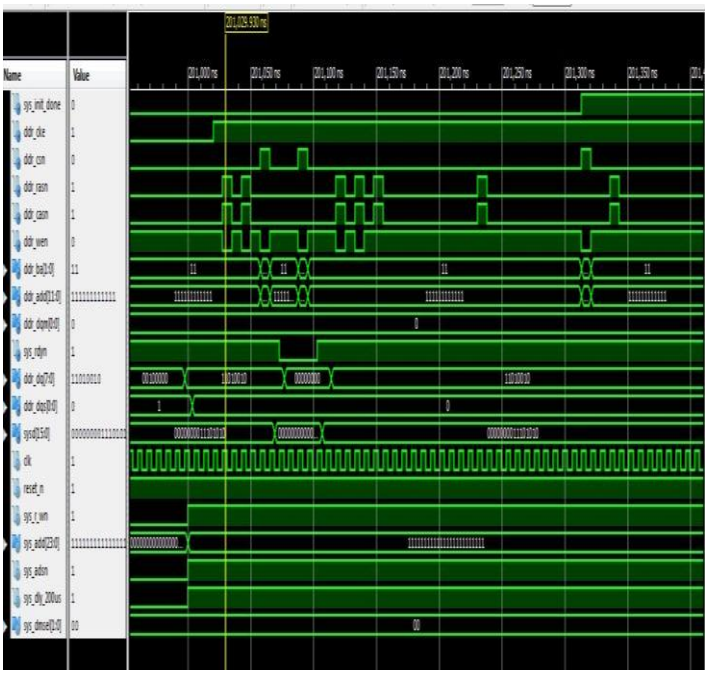

Figure 3 Simulation Result for the Controller Architecture.

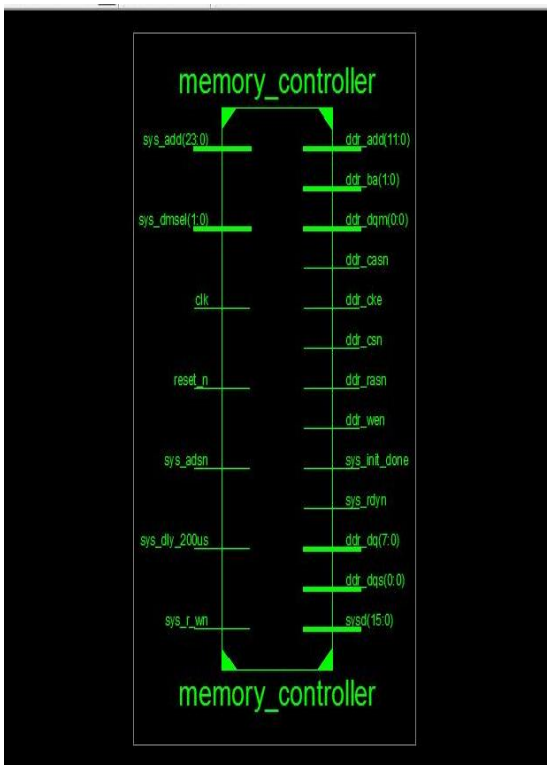

Figure 4 Top Level RTL Schematic of the Controller.

Figure 5 Detailed Schematic of the Controller.

Table 1 Device Utilization Summary Report Obtained for Spartan 3E FPGA.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	104	4656	2%
Number of Slice Flip Flops	143	9312	1%
Number of 4 input LUTs	131	9312	1%
Number of bonded IOBs	76	232	32%
Number of GCLKs	1	24	4%

5. CONCLUSION

A fully functional memory controller targeted at Spartan 3E FPGA is designed in verilog HDL and the simulation result is obtained using the Xilinx ISE design suite 14.2 tool. The schematics of the complete designed architecture and the summary report which indicates the device utilization are also generated.

REFRENCES

[1] Veena H K, Dr. A H Masthan Ali, "Design and Implementation of High Speed DDR SDRAM Controller onFPGA",International Journal of Engineering Research and Technology (IJERT) Vol. 4, Issue 7, July 2015.

[2] Sushil Kumar Pachauri, SuvendraSahoo, "Design and Implementation of High Performance Dynamic Memory Controller", Advance in Electronic and Electric Engineering, Vol. 4, Issue 6, 2014.

[3] SonaliAshokkumar Patel, Santoshkrishna M, "Design of DDR SDRAM Controller for Embedded System", Journal of Information, Knowledge and Research in Electronics and Communication Engineering, vol. 2, Issue 2, October 2013.

[4] Dr.Anu Gupta, VaibhavGogte, Gaurav Jain, Shivani Bathla, "A Comparative Exploration of Architecture of Single Data Rate and Double Data Rate SDRAM for an Efficient Implementation", Proc. of Int. Conf. on Advances in Electrical & Electronics 2011.

[5] Spartan-3E FPGA Starter Kit Board User Guide, UG230 (v1.2) January 20, 2011.Available at http:// www.xilinx.com.

[6] DDR SDRAM MT46V32M16 Datasheet 512Mb: x4, x8, x16 DDR SDRAM Features.Available at http;//www.micron.com.

[7] https://en.wikipedia.org/wiki/Xilinx.