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High Speed, Low Power Viterbi Decoder for Wireless Communication

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Abstract -*In wireless communication, low power encoders and Decoders are highly beneficial. This work presents Hybrid method Viterbi decoder which has less delay in data transmission compared to trace back type and register exchange type. Also it needs very less power and area. The Viterbi algorithm is a widely used algorithm for decoding of convolution codes. The algorithm helps to find a path of the trellis diagram, in which the sequence of output symbols is nearly equal to the received sequence. for this purpose , the decoder measures the distance to the received symbols sequence by calculating path metric for each path.The branch metric calculates metric distance between the received noisy symbol and the output symbol of the state transition. The accumulated metric associated with the sequence of transitions (path) to reach a state is computed by ACSU . When more than one path arrives to a state, ACSU selects the path with the lowest metric value, which is the survivor path. SMU (survivor memory unit) stores the information that permits to trace back from a state to the previous one. Hybrid unit is incorporated between ACS unit and SMU. In Hybrid method number of memory blocks are reduced. This in turn reduces the area requirement. The two clock cycle is used, in which one is for trace back the information and another for storing the information in register block. This leads to a major gain in speed of data correction along with low power. The overall System will be designed using HDL language and simulation.*

Key Words: BRANCH METRIC UNIT (BMU), ADD COMPARE AND SELECT UNIT (ACSU), SURVIVOR MEMORY UNIT (SMU), HARDWARE DESCRIPTION LANGUAGE (HDL)

1.INTRODUCTION

A convolution code allows an efficient hard-decision. It has been widely used in many wireless communication systems to improve the output signal quality of the communication channels. The most frequently used decoding algorithm for Convolutional codes is Viterbi algorithm. The increased use of wireless technology has brought a huge change the way communication is done in modern world. With this increased availability the dependency on the communication systems has increased to transmit information in faster way and with higher accuracy. Because the communication channels in wireless systems is much noisy than wired systems, voice and data must have forward error correction coding to reduce the introduced during wireless data transmission. Wi-Fi is generally used as an effective medium to exchange data wirelessly. Viterbi decoding, can be used to improve performance of wireless communication channels.

The Viterbi Algorithm, is widely used for predicting and finding problem in digital communications and signal processing. It is used to decode sequential error control codes and to detect signals in communication channels with memory, thereby enhancing the performance of digital communication systems. Convolutional codes are the most commonly used error correcting codes in noisy channels. They have a good correcting ability even on very bad channels. They are most widely used in satellite communications. Convolutional encoding is quite easier procedure but the decoding of a Convolutional code is a complex procedure. Various classes of algorithms are used for this purpose.

The Viterbi decoding algorithm was proposed in 1967 by Viterbi. It is a decoding technique for Convolutional codes in memory-less noisy channels. This algorithm can be used to solve most of problems detected while designing communication systems. The Viterbi decoding algorithm provides a maximum-likelihood decoding. It identifies a code word that provides maximum the conditional probability of the received code word and the decoded code word.

1.1 PRELIMINARY RESEARCH

In the preliminary research it has been found that the constraint length associated with the input bits are large, hence it needs to implement the larger constraint length with lesser hardware and lesser computations for decode the original data. So the proposed method uses Hybrid method of Viterbi decoder which will lover down the power consumption and increase the speed of operation.

1.2 CONVOLUTIONAL ENCODER

To convolutionally encode data, start with k memory registers, each holding 1 input bit. Unless otherwise specified, all memory registers start with a value of 0. The encoder has nmodulo-2 adders (a modulo 2 adder can be implemented with a single Boolean XOR gate, where the logic is: 0+0 = 0, 0+1 = 1, 1+0 = 1, 1+1 = 0),and n generator polynomials, one for each adder (see figure below). An input bit m1 is fed into the leftmost register. Using the generator

polynomials and the existing values in the remaining registers, the encoder outputs n symbols. These symbols may be transmitted or punctured depending on the desired code rate. Now bit shift all register values to the right (m1 moves to m0, m0 moves to m-1) and wait for the next input bit. If there are no remaining input bits, the encoder continues shifting until all registers have returned to the zero state (flush bit termination).

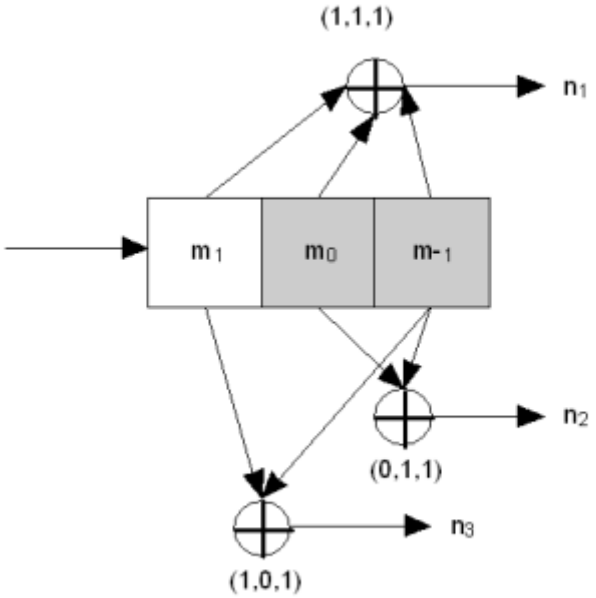

Fig -1: Convolutional Encoder with K=3

The figure 1 above has a rate $1/3$ (m/n) encoder with constraint length (k) of 3. Generator polynomials are G_1 = (1,1,1),G_2 = (0,1,1), and G_3 = (1,0,1). Therefore, output bits are calculated (modulo 2) as follows:

$n_1 = m_1 + m_0 + m_{-1}$

$n_2 = m_0 + m_{-1}$

$n_3 = m_1 + m_{-1}$.

2.1 VITERBI ALGORITHM

The Viterbi is a maximum likelihood decoding algorithm for Convolutional codes. When the hamming distance which is used to compute the probability of received signal is called as "Minimum distance decoding" or Maximum likelihood decoding algorithm." In general forward, stop and reverse is a process of "maximum likelihood sequence" generation. The Viterbi algorithm uses the trellis diagram to compute the path metric value (accumulated distance) from the received sequence to the possible transmitted sequences. The total number of such trellis paths increases exponentially with the number of stages in the trellis. It causes potential complexity and memory problems.

2.2 VITERBI DECODER

A Viterbi decoder consists of three major parts:

A. Branch metric unit

The branch Metric Unit consists of EXOR Gate and 3-bit counter.BMU compares the received data signal with the expected data code with the help of EXOR Gate and it will count the number of the differing bits through 3-bit counter. The 3-bit counter is designed by cascading the DFF output of one flip flop is given as the clock input to the other flip flop.

B. Add compare and select unit

The Add compare and select Unit which is the second main block in Viterbi decoder. which adds the output of the branch Metric to the corresponding path metrics the added result that is new path metric is stored in the Path Metric Memory. The Add Compare Select unit is a collection of ACS units. An each stage of ACSU receives output of two Branch Metric Unit and two path metrics.

C. Survivor Memory Unit

The Survivor memory unit is designed by using the serial-in-serial-out shift register and the length of the shift register depends on the length of the convolution encoder. It is possible to form registers by collecting the flip-flops in the vertical direction or in the horizontal direction.

Figure 2 below shows the general architecture of Viterbi Decoder.

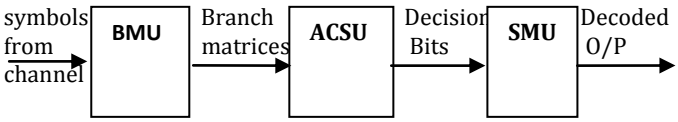

Fig -2: Architecture of Viterbi Decoder.

2.3 DECODING METHODS

There are two basic methods of Viterbi decoder register-exchange method and the trace back method. The register exchange is very easy to understand, and works well for small constraint lengths. The trace back method is a bit more difficult, but works well for longer constraint length codes. So the proposed method is the combination of the two methods i.e. the register exchange method and trace back method called Hybrid method.

A. Trace back Method

Trace back method stores the decisions from the ACS into a RAM. Later, the decisions are read out. The best path is determined by reading backwards through the RAM, and tracing a path backwards through the trellis. This reads the bits out in backwards order. Further, several reads are required to trace backwards far enough to find where the

paths have merged. The trace back method is as shown in Fig.4.1.

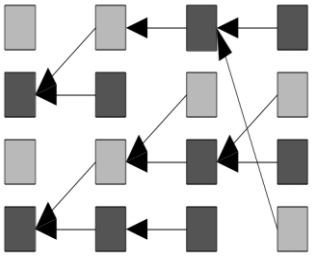

Fig -2: Trace back Method

B. Register Exchange Method:

In Register Exchange Method, a register is assigned to each state contains information bits for the survivor path throughout the trellis. The register keeps the partially decoded output sequence along the path. The register exchange method eliminates the need to trace back since the register of final state contains the decoded output. This approach results in complex hardware and high switching activity due to the need to copy the content of all the registers from state to state. The register exchange method is fairly basic each state has an N bit register associated with it. The best path is loaded into this register each cycle. This largely prevents the use of RAM. At the same time, the best path data is very easy to access. Register exchange method is as shown in Fig.3.

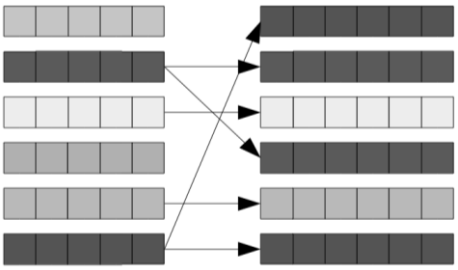

Fig -3: Register Exchange Method

C. Hybrid method:

In this method register exchange and trace back method is combined, therefore the name Hybrid register exchange method, which reduces further the switching activity and power. Here we are using a property of trellis is that, if we go forward for m cycles then the data bits will be the corresponding state bits irrespective of the initial state from where the data gets transferred. To find the initial state we have to trace back through an m cycles by observing the survivor memory. And then transfer the partial decoded data from initial state to the next state which is m cycle later and not a subsequent cycle. Now if the trellis is strongly connected, then the states on survivor path will correspond to the input bits. Register exchange method requires high memory storage. In Hybrid method the memory operation is not at every cycle, and it gets reduced by a factor of m. Also the shifting of data from one register to another is reduced that is the switching activity will reduce. Hybrid method is as shown in Fig.4.

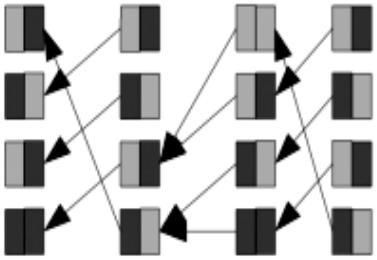

Fig - 4: Hybrid Method

3 RESULTS

The proposed design of hybrid Viterbi decoder is coded in VHDL language using XILINX 13.1. The obtained results are shown below.

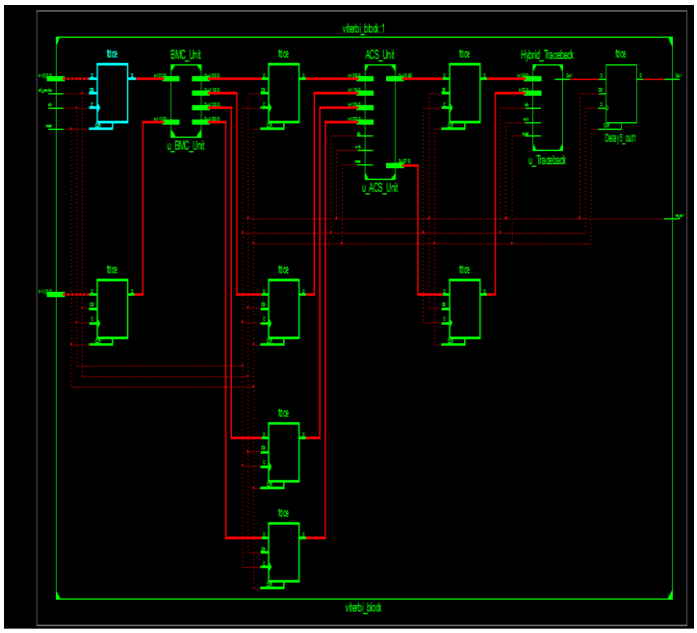

Fig - 5: RTL Schematic of Viterbi Decoder

Table -1: Device utilization summary

Device Utilization Summary			
Logic utilization	Used	Available	Utilization
Number of Slice Registers	3,673	184,304	1%
Number of fully used LUT flip flop pairs	1,856	5,535	33%
Number of Sliced LUT'S	4,418	92,152	4%
Number of bonded IOBs	11	540	2%
Number of BUFG/BUFGMUXs	1	16	6%

Above table 1 describes the device utilization summary of proposed Viterbi Decoder.

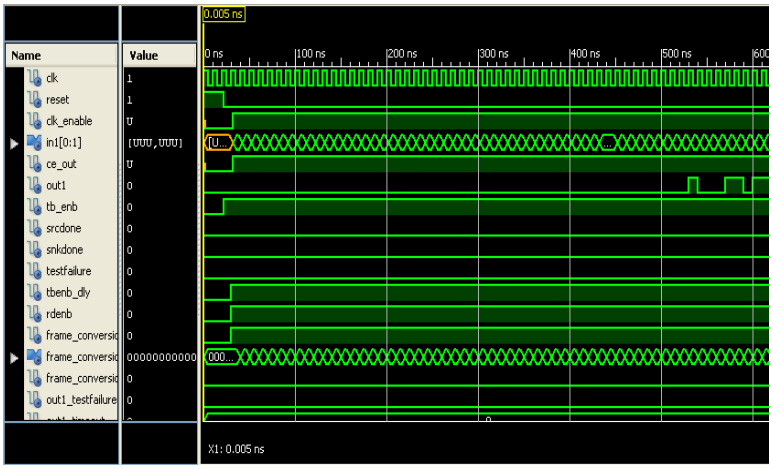

Fig - 6: Output of proposed Viterbi Decoder

The above work requires 113 mW power and Processing frequency of 110MHZ and requires maximum period of 18.742 ns. Also it is a Memory less Design.

4. CONCLUSIONS

The proposed system is designed to reduce the complexity associated with Viterbi decoding technique. Also by using Hybrid method of decoding by combining register exchange and traceback method, the memory utilization is simplified, thereby reducing the power requirement of the system and improving the speed of the system.

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