

Electromagnetic transient analysis of saturated iron-core superconducting fault current limiter and DVR

Y. Naga Vamsi Krishna¹, k.kamala devi²

¹Pg scholar, Department of EEE, Bapatla engineering college, Andhra Pradesh, India.

²Assistant Professor, Department of EEE, Bapatla engineering college, Andhra Pradesh, India.

Abstract – Saturated iron-core super conducting fault current limiter offers outstanding technical performances in comparison with other fault current limiters. Based on the actual structure, equivalent magnetic structure was proposed. In order to calculate the current limiting inductance Newton iteration method and fundamental magnetization curve were used during simulation. During faults due to the rise in current levels sags and swells were observed. In the grid operation voltage fluctuations and short circuits are two major problems. In this paper a new concept for limiting fault current by using SISFCL and to diminish voltage fluctuations dynamic voltage restorer were used. Comparisons carried out theoretically and electromagnetic transient simulation model of these devices were built in Matlab/simulink. The transient behavior of these devices in simulation tests illustrates that proposed method is valid and correct.

Key Words: Electromagnetic transient analysis, Newton iteration method, saturated iron core, Superconducting fault current limiter (SISFCL), Dynamic voltage restorer (DVR), Pulse width modulation technique.

1. INTRODUCTION

Overall electric current loading on the transmission system has been rapidly climbing to meet the growth in demand for electricity. In response to ever growing needs for electricity, power producers have been expanding the power grids continually, particularly with the proliferation of independent power producers (IPP's). Technical advancements and promotions of various types of renewable energy generation have also led to a large number of distributed generators (DG's) connected to the power grids. However, this fast expansion of generation capacity obscures a hidden issue, which must be resolved: the potential fault current levels keep increasing as the source impedances are lowered due to the paralleled connections of the growing number of generators which is shown in fig 1. As a result, the potential short-circuit current levels increase substantially, approaching the limits of the devices in existing power systems, including the cables, switchgears, protection devices, and loads. Specifically, if the fault current levels exceed the interruption ratings of existing protection devices, such as fuses and circuit breakers, the

equipment will suffer serious damage. In extreme cases, failure to interrupt fault current may destroy insulation of conductors and oil-filled equipment, causing fire or explosion.

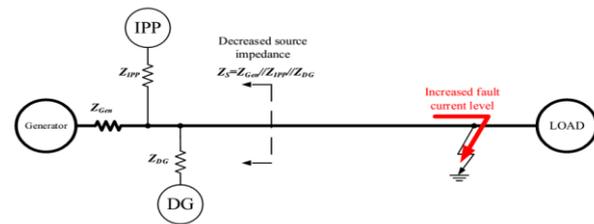


Fig 1: Parallel IPP and DG decrease source impedance and increase potential fault current level on the power system

Various techniques have been proposed to mitigate the increasing fault current issues like bus splitting, multiple circuit breaker upgrading, current limiting reactor, sequential breaker tripping. While each technique has its own advantage and disadvantage, our proposed model is best in comparison with all these conventional methods as shown in the fig 2.

Solution/method	Advantage	Disadvantage	Relative cost	Relative cost to SFCL
New sub station	Provides for future growth	Expensive and lengthy to install	Most expensive	SFCL is less expensive
Bus splitting	Separate sources of load current	Separate sources of load current from load centres and undermines system reliability	High if split bus is not installed	SFCL less expensive
Multiple circuit breaker upgrade	Most direct solution with no adverse side effects	Difficult to schedule outages; bus work reinforcement also needed	High to medium, depending on number of breakers	SFCL less expensive than most multiple breaker upgrades
Current limiting reactor	Easy to install	Voltage drop and power losses	Medium to low	SFCL cost higher
Sequential breaker tripping	No major hardware installation involved	Expands impact of fault to wider range of system	low	SFCL cost higher

Table 1

Fig 2: comparison of SISFCL with conventional methods

Under the situation, superconductive fault current limiters (SFCLs) have been considered as a good solution to cope with the large fault current [1].

The superconducting fault current limiter has been categorized into two types: quench and non quench types [2]. The quench-type SFCL relies on the transition of superconducting material from superconducting to normal conducting state when a fault occurs [3]. Hence, the quench-type SFCL suffers from many problems, such as slow fault response and long recovery time. The saturated iron-core superconducting fault current limiter (SISFCL), one of the non quench-type SFCLs, is based on the non-linear

characteristic of magnetic cores' permeability. The SISFCL can realize instantaneous reaction and return to normal operation quickly after the fault being isolated [4]. The theoretical analysis of SISFCL is given in section 2.

Voltage fluctuations and short circuit problems become a major issue at all the levels of power sector. Usually single line to ground fault occurs in the power system which results in terms of voltage sag. This is mainly due to the usage of sensitive and critical loads. Faults in power system can cause voltage sag or swell in the entire system or major part of it. In addition, harmonics, voltage transients, flickers are also one of the voltage quality problems [5].

Voltage sag can occur at any instant of time ranging from 0.1 to 0.9 p.u and that lasts for half a cycle to one minute [6]. Voltage sag can be either balanced or unbalanced which mainly depends on type of fault. The main sources of voltage sag are any type of fault in power system or by the starting of large motor loads. Mainly, voltage sags are considered as major threats to the power quality. Similarly voltage swells occurs at any instant of time ranging from 1.1 to 1.8 p.u and that lasts for half a cycle to one minute. But voltage swells are less frequent compared to that of voltage sags which are mainly produced because of sudden switching off of large loads or energization of capacitor banks [7].

Due to these disturbances, system may undergo shutdown or fail including large voltage and current imbalances in the system. So in order to curb these unwanted disturbances we need a special custom power device called dynamic voltage restorer is introduced in section 3. There are FACT devices available like DSTATCOM, SVC, SMES, SVG, TCR, DVR etc., out of which DVR is the best solution for effective and efficient compensation of voltage sags and swells due to following reasons.

- (a) Compared to SVC, DVR has better capability of controlling active power flow.
- (b) Because of its high maintenance and replacement cost, DVR is preferred over UPS.
- (c) SMES is high cost and has lower energy capacity compared to that of the DVR.
- (d) DVR is smaller in size and lower cost when compared to DSTATCOM.

So the two concepts proposed in this paper were best solutions in comparison with other technologies. The SISFCL model proposed in this paper to reduce fault current acts as a current limiting device while subsequent DVR is used as a voltage controlled device. The analysis is carried out individually in order to understand better for different types of faults are given in this paper.

2 SATURATED IRON-CORE SUPERCONDUCTING FAULT CURRENT LIMITER

A typical SISFCL mainly consists of three parts: iron cores, ac coils and dc superconducting coils, as shown in Fig. 3. In the normal operation condition, the dc current in superconducting coil drives both iron cores into deep saturation. As the low permeability of saturation region, the

inductance of SISFCL is very small in normal operation condition. When a fault occurs, the high ac current drives the working points of two iron cores to be out of saturation alternately each half cycle. Since the permeability of the cores increases significantly, a high impedance value is obtained to limit the fault current [8], [9].

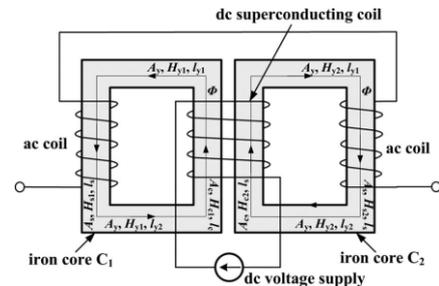


Fig 3: Basic sketch of the saturated iron-core superconducting fault current limiter.

The SISFCL addressed in this paper uses loose coupling structure. The high-voltage section (ac coils) and low-voltage section (dc superconducting coil) are separated to make the structure more compact. The two separated iron cores include central cylinders, yokes and side cylinders, which have different cross-sectional areas A_c , A_y and A_s . Central cylinders are surrounded by the dc superconducting coil, and side cylinders are surrounded by the ac coils which are connected into the power system to limit fault current. The electromagnetic transient process of the three independent single-phase SISFCL are the same, hence we just take one for example in this paper.

In terms of the basic diagram of the magnetic circuit shown in Fig. 3, the magneto motive forces (MMF) of magnetic circuits C_1 and C_2 are satisfied with the (1) and (2) respectively according to the law of magnetic circuit.

$$H_{s1}l_s + H_{y1}l_y + H_{c1}l_c = N_{ac}i_{ac} + N_{dc}i_{dc} = F_1 \quad (1)$$

$$H_{s1}l_s + H_{y2}l_y + H_{c2}l_c = N_{ac}i_{ac} - N_{dc}i_{dc} = F_2 \quad (2)$$

Where l_s , l_y and l_c are the mean lengths of the side cylinder, the yokes and the central cylinder in each magnetic circuit;

$$l_y = l_{y1} + l_{y2};$$

H_{s1} , H_{s2} , H_{y1} , H_{y2} , H_{c1} , H_{c2} are the magnetic field strengths of the side cylinders, the yokes and the central cylinders in magnetic circuits C_1 and C_2 respectively; N_{ac} and N_{dc} are the turns of ac windings and dc windings respectively; i_{ac} and i_{dc} are the currents of ac windings and dc windings; F_1 and F_2 are the magneto motive forces in the two iron cores respectively.

According to the equivalence principle, the equivalent excitation currents of the two iron cores are satisfied with

$$N_{ac}i_{ac} + N_{dc}i_{dc} = N_{dc}i_{\mu 1} \quad (3)$$

$$N_{ac}i_{ac} - N_{dc}i_{dc} = N_{dc}i_{\mu 2} \quad (4)$$

Where $i_{\mu 1}$ and $i_{\mu 2}$ are the equivalent excitation currents. Because the cross-sectional area of central cylinders yokes and side cylinders in each iron core are different in the same magnetic flux, their corresponding magnetic field strengths are in different value. For simplicity, we can decompose the equivalent excitation currents of the two iron cores into three parts respectively.

$$i_{\mu 1} = i_{\mu 1.s} + i_{\mu 1.y} + i_{\mu 1.c} \quad (5)$$

$$i_{\mu 2} = i_{\mu 2.s} + i_{\mu 2.y} + i_{\mu 2.c} \quad (6)$$

And meet the following conditions

$$H_{s1}l_s = N_{dc}i_{\mu 1.s}, H_{y1}l_y = N_{dc}i_{\mu 1.y}, H_{c1}l_c = N_{dc}i_{\mu 1.c} \quad (7)$$

$$H_{s2}l_s = N_{dc}i_{\mu 2.s}, H_{y2}l_y = N_{dc}i_{\mu 2.y}, H_{c2}l_c = N_{dc}i_{\mu 2.c} \quad (8)$$

The three equivalent excitation currents $i_{\mu 1.s}$, $i_{\mu 1.y}$ and $i_{\mu 1.c}$ (or $i_{\mu 2.s}$, $i_{\mu 2.y}$ and $i_{\mu 2.c}$) are determined by the nonlinear B-H curves of the three independent iron cores. Based on above analysis, the complete equivalent magnetic circuit was illustrated in Fig. 4

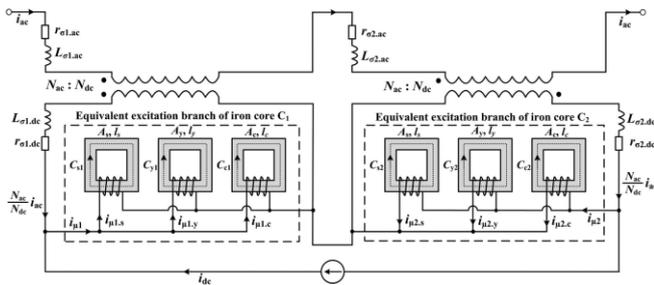


Fig 4: Equivalent magnetic circuit of two iron cores.

The current-limiting inductances L_{μ} of the SISFCL equal to the parallel inductance values of these three independent parts

$$L_{\mu} = L_{\mu 1} + L_{\mu 2} = (L_{s1} // L_{y1} // L_{c1}) + (L_{s2} // L_{y2} // L_{c2}) \quad (9)$$

Where $L_{\mu 1}$ and $L_{\mu 2}$ are the actual inductances of the two iron cores; L_{s1} , L_{s2} , L_{y1} , L_{y2} , L_{c1} , L_{c2} are the excitation inductances of the equivalent magnetic circuits shown in Fig. 4.

For any closed iron core with coils shown in Fig. 4, the equivalent inductance L can be deduced as [2]

$$L = \frac{N^2 \mu A}{l} \quad (10)$$

Where N is the coil turns, A is the cross-sectional area, l is the mean length, μ is magnetic permeability. Since the values of N , A and l are all constant, the current-limiting inductance L_{μ} will be obtained as long as the magnetic permeability μ of each iron cores can be estimated with high accuracy. Based on the above analysis, the electromagnetic transient simulation of the SISFCL can be realized in the following steps. First, i_{ac} , i_{dc} , N_{ac} and N_{dc} are all known quantities in, i.e., the MMF F_1 and F_2 can be calculated in each step of the

simulation. Second, according to the MMF values F_1 and F_2 , the magnetic flux of the iron cores Φ_{C1} and Φ_{C2} can be estimated by solving nonlinear equations. Third, the magnetic permeability μ_{s1} , μ_{s2} , μ_{y1} , μ_{y2} , μ_{c1} , μ_{c2} can be obtained based on the fundamental magnetization curve of the iron core. Finally, the current-limiting inductance L_{μ} can be calculated by (9).

The algorithm for matlab simulation is as shown in fig 5. Flux value can be obtained by using newton iteration method.

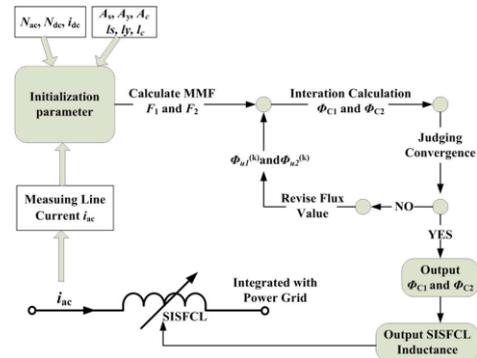


Fig 5: Algorithm process in Matlab/Stateflow.

The parameters of the simulated transmission line were from reference [6]. Based on magnetic circuit analysis and nonlinear equation solution shown in Fig. 4, the transient performance of the SISFCL during short-circuit faults was simulated in the paper. In simulation, $N_{ac} = 26$, $N_{dc} = 660$, $i_{dc} = 600A$, $A_c = 0.8 \text{ m}^2$, $A_y = 0.6 \text{ m}^2$, $A_s = 0.4 \text{ m}^2$. When a single-phase-to-ground fault occurred at 0.1s, the SISFCL started to limit fault current. Figs. 5 and 6 showed the waveforms of the magneto motive forces F_1 , F_2 and magnetic flux Φ_{C1} and Φ_{C2} in the two iron cores of the SISFCL. The MMFs and magnetic flux of the two iron core were about $3.96 \times 10^5 \text{ (A} \cdot \text{turns)}$ and 1.298 Wb respectively before the fault. The model diagram is simulated by using variable inductor which will varies in accordance with current as shown in the Fig 6. By using a switch a control logic is used in a way such that very low impedance is offered during normal condition and at the time of fault it will choose in accordance with the current thus offering a prominent function. Uniform random number block has one min and one max value in which our inductance will vary according to the severity of the fault.

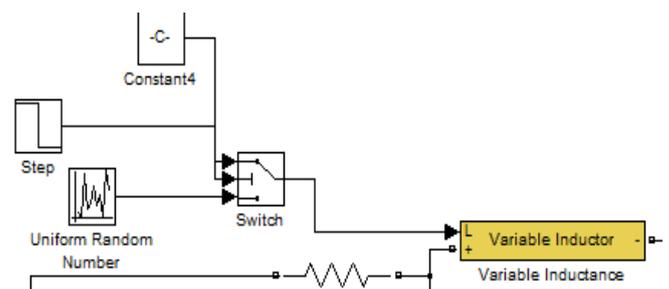


Fig 6: Control circuit used in simulink model for variable inductance

3 DYNAMIC VOLTAGE RESTORERS

The main function of DVR is to inject the desired voltage quantity in series with the supply with the help of an injection transformer whenever a voltage sag is detected. It is normally installed in a distribution system between the supply and the critical load feeder at the point of common coupling (PCC). Other than voltage sags and swells compensation, DVR can also added other features like: line voltage harmonics compensation, reduction of transients in voltage and fault current limitations.

The basic elements of a DVR consists of injection boost transformer, harmonic filter, storage device, voltage source converter, dc charging circuit, control and protection system as shown in fig.7.

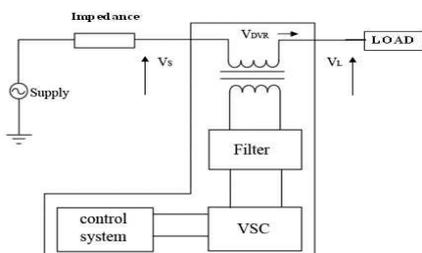


Fig 7: Basic structure of DVR

The DVR has three modes of operation which are: protection mode, standby mode, injection/boost mode.

protection mode: If the over current on the load side exceeds a permissible limit due to short circuit on the load or large inrush current, the DVR will be isolated from the systems by using the bypass switches (S_2 and S_3 will open) and supplying another path for current (S_1 will be closed).

Standby Mode: (VDVR = 0) In the standby mode the booster transformer's low-voltage winding is shorted through the converter. No switching of semiconductors occurs in this mode of operation and the full load current will pass through the transformer primary

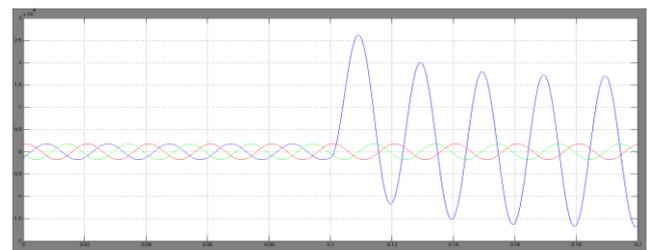
Injection/Boost Mode: (VDVR≠0) In the Injection/Boost mode the DVR is injecting a compensating voltage through the booster transformer after the detection of a disturbance in the supply voltage

The simulink diagram for dynamic voltage restorer is using pulse width modulation technique and PID controller for controlling circuit and using IGBT as a voltage source converter. Utilizing the power electronic device and small DC reactor causes a negligible voltage drop on the FCL circuit. When a fault occurs PCC voltage goes to drops and sensors detects that dropped voltage and compare to reference p.u voltage value with relational operator generates switching pulse to turns-off the power electronic switch.

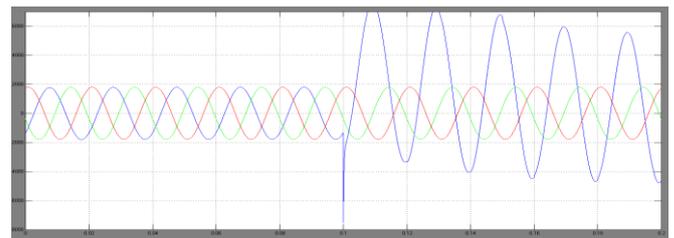
4 Simulation Results And Analysis:

4.1 Current Limitation:

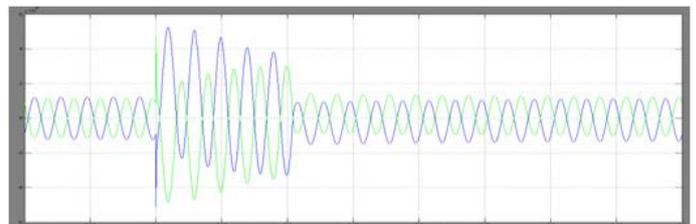
The simulation results shown in the fig 9(a) shows the fault current approximately 25k amps with single phase to ground fault while our proposed sisfcl is not present in the system. With the induction of SISFCL, it limits the fault current to almost 7k amps as shown in fig 9(b).MMF and Flux waveforms are also shown in fig 9(c), 9(d) respectively.



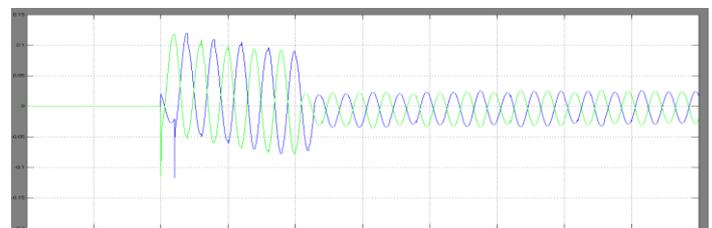
(a)



(b)



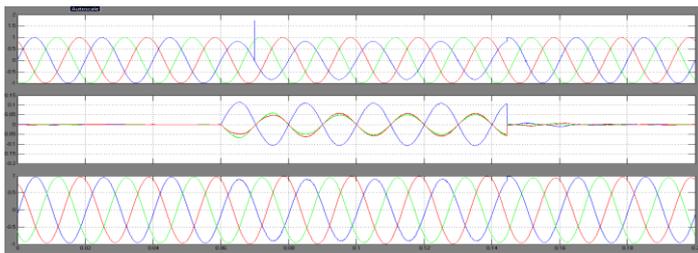
(c)



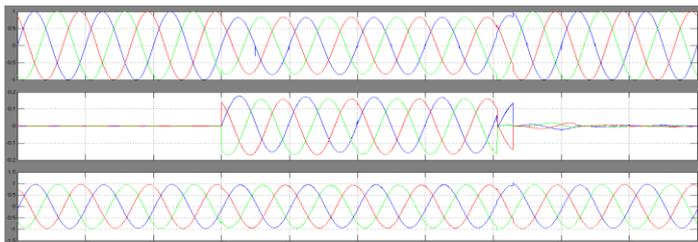
(d)

Fig 9. (a) LG fault without SISFCL (b) LG fault with SISFCL (c) MMF waveform (d) Flux waveform

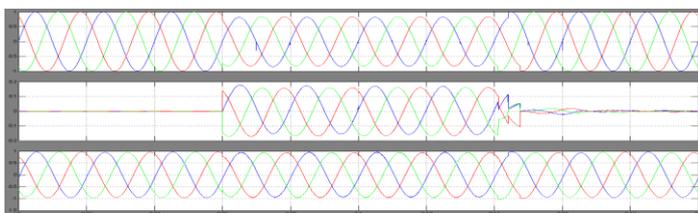
The simulation results shown in fig 10 are the various fault conditions of dynamic voltage restorer which shows that DVR offering required compensating voltage.



(e)



(f)



(g)

Fig 10. (e) Single line to ground fault with DVR (f) LLL fault with DVR (g) LLLG fault with DVR.

3. CONCLUSIONS

A novel equivalent magnetic circuit was proposed in this paper to analyze the transient behavior of SISFCL based on the mmf and flux relation of two iron cores. By using Newton iteration method flux is obtained based on mmf and finally current limiting inductance is obtained. DVR is also proposed in order to mitigate the voltage fluctuations which were quite commonly observed during faults. This paper finally concludes the performance of SISFCL to curb fault levels very effective out of all available fault current limiters and performance of DVR is efficient in restoring voltage fluctuations in its respective category after observing the working of these two devices independently by using matlab/simulink. The behavior of SISFCL and DVR have illustrated that proposed method is valid and correct. The combination of SISFCL and DVR can be used as both current and voltage controllers and simulink analysis is being used in real-time applications

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BIOGRAPHIES

Author 1: Y.Naga vamsi krishna, completed his B.Tech in GIET,Rajahmundry in the year 2013 and currently pursuing his master degree in Power Systems in Bapatla Engineering College,Bapatla.

Author 2: K.Kamala devi, completed her B.Tech in A.N.U in the year 1993 and her master degree in power system engineering in A.N.U in 2003 and currently working as assistant professor in department of EEE,Bapatla engineering college,Bapatla.