

Five Level Inverter to reduce Harmonics

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Abstract - With the development in controlling technology, demand for the efficient power systems is increased in the market. It is difficult to achieve efficient power system by using traditional approach & arrangement of power component. Voltage converters, Inverters & UPS are most commonly used power sources. These sources mainly comprises of inverter block so demand for highly efficient, reliable and compact inverters is increasing in market. So as to achieve these requirements multi-level inverter technology are evolving. The multilevel inverters are suitable for various high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum , faithful output, size & efficiency. This paper deals with a five-level converter topology that follows this trend. In five-level, topologies and a theoretical power loss comparison as compare with two level inverter with the proposed solution is realized.

Key Words: Multilevel inverter, Two level inverter, Five level inverter.

1. INTRODUCTION

Currently two level & three level inverter topology are used widely. Level of inverter topology depends on the different voltage level available in the supplied DC source. Two & three level inverter topology is used in various applications such as in Uninterruptable Power Supply (UPS); Frequency converter (FC) & Inverters use for home appliances. It is also used at some other power conversion devices.

Here we are proposing the five level inverter topology which helps to reduce the harmonic content of the converters output voltage, which will reduce power losses, size and cost of filter circuit & leading to increase in efficiency of the inverter.

Five level inverter topology can replace the two level & three level inverters with addition of control mechanism with advantages of better efficiency, size & cost. So five level inverter can directly used in same field with its advantages. Multilevel topologies allows to reduce the harmonic content of the converter output voltage, allowing the use of smaller and cheaper output filters. Moreover, these topologies are usually characterized by a strong reduction of the switching voltages across the power switches, leading in the reduction of switching power losses and electromagnetic interference (EMI) [1]. In this paper, full-bridge topology with two additional power switches is used. Two diodes in series are connected across conventional bridge & common point of diodes is connected to the midpoint of the dc link. Additional power switched are used to obtain different DC voltage levels. MATLAB/SIMULINK software is used to simulate five level & two level inverter topology.

2. PROPOSED FIVE-LEVEL SINGLE-PHASE SOLUTION

Fig. 1 shows proposed converter. This converter architecture is known as the H6 bridge & was originally developed in [2], combination with a suitable PWM strategy in order to keep common-mode voltage constant.

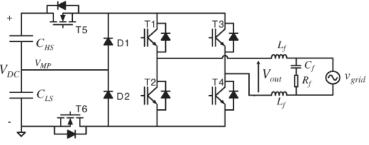


Fig. 1: Proposed converter

2.1 Working Principle:

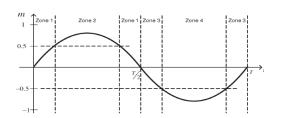
The converter is constituted by full bridge inverter with an additional bidirectional switch (realized with an IGBT and four diodes), employed to connect the midpoint of the dc link to the converter output. The energy efficiency of this solution is potentially very high [2]; however, the capacitor's voltage balancing is not taken into account. A variation with the positive rail of a full-bridge can be connected either to the dc link or to the midpoint of the dc-link capacitors. Only six devices are needed, and the maximum number of conducting devices is three. However, the balancing of the dc-link capacitors is a serious issue and limits the field of application to a reactive compensator [3].

Basic working principle of the propose five level inverter topology can be explain in brief by stating that input DC to the inverter bridge can be varied by the switching the mosfet T5 & T6. DC voltage require at the input is in propionate to the output sine wave require [4]. This can be explained with help of below table.

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International Research Journal of Engineering and Technology (IRJET)e-IIVolume: 03 Issue: 08 |Aug - 2016www.irjet.netp-II



OUTPUT VOLTAGES IN THE DIFFERENT WORKING ZONES

Zone	m	Output Voltages
Zone 1	0 < m < 0.5	V_{MP} and 0
Zone 2	0.5 < m < 1	V_{DC} and V_{MP}
Zone 3	-0.5 < m < 0	$-V_{MP}$ and 0
Zone 4	-1 < m < -0.5	$-V_{DC}$ and $-V_{MP}$

Fig. 2: Output sine wave (Zone marking) & voltage require at different Zone

The output voltage of the converter can be written as Vout = mVdc [5][6]. Depending on the modulation index value, the power converter will be driven by different PWM strategies. As a matter of fact, it is possible to identify four operating zones (see Fig. 2), and for each zone, the output voltage levels of the power converter will be different [7][8].

2.2 Actual Working with Zones:

With reference to the schematic in Fig. 3, Fig. 4, Fig. 5 & Fig. 6 the behaviour of the proposed solution is shown for a whole period of the grid voltage, i.e., of the modulation index [9]. During the positive semi period the transistors T1 and T5 are ON and T2 and T3 are OFF.

With reference to Fig. 3 in Zone 1, T5 is OFF and T6 commutates at the switching frequency, whereas in Zone 2 refer fig 5, T5 commutates at the switching frequency and T6 is ON. During the negative semi period the full-bridge changes configuration, with T1 and T5 OFF and T2 and T3 ON [10][11]. With similarity to Zone 1 and 2, in Zone 3 T5 commutates while T6 is OFF, and in Zone 5 T5 in ON and T6 commutates. Fig 3 shows proposed five-level PWM strategy for Zone 1.

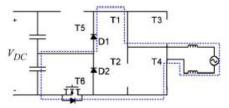


Fig. 3: Active phase for zone

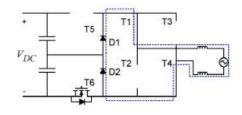


Fig. 4: Freewheeling phase for zone 1

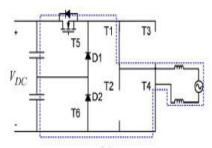


Fig. 5: Active phase for zone 2

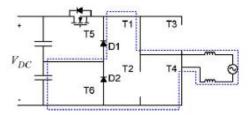


Fig. 6: Freewheeling phase for zone 2

3. Simulation In MATLAB SIMULINK

Two level & Five level inverter simulation is done in MATLAB SIMULINK & results of same are recorded.

Fig. 7 and Fig. 10 represents power circuit of Two & Five level inverter respectively. As shown in fig. 10 two switching devices are added in the series of DC source which are operated to achieve variable DC voltage applied to inverter IGBT bridge.

Fig. 8 & Fig. 11 shows the PWM signals used to drive the IGBT of Two level & five level inverters respectively. Two additional PWM signals highlighted in Fig. 11 are used to switch the devices connected in series of input DC supply. Switching operation of these devices is explained in section 2.1 & 2.2.

Fig. 9 & Fig. 12 shows the output waveform before output LC filter of two & five level inverter respectively. As shown in Fig. 12, Waveform near to sine wave is achieved due to switching devices in series of DC voltage which helps us to achieve output sine waveform with minimum inductor in output filter.

3.1 Two Level Inverter

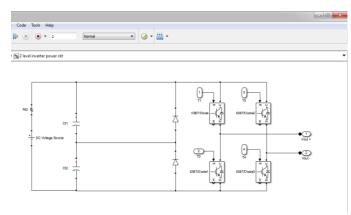


Fig. 7: Power Circuit Two Level Inverter

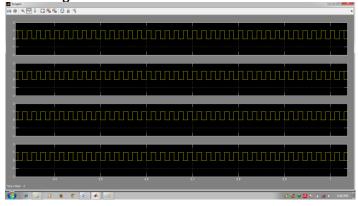


Fig. 8: PWM Generated For Two Level Inverter

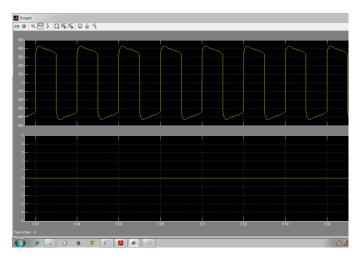


Fig. 9: Output waveform before filter Two Level Inverter

3.2 Five Level Inverter

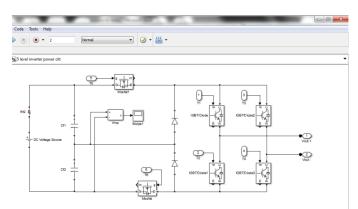


Fig. 10: Power Circuit Five Level Inverter

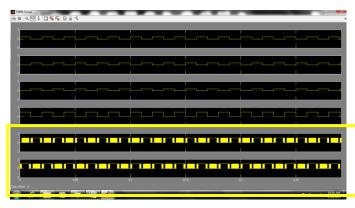


Fig. 11: PWM For Five Level Inverter

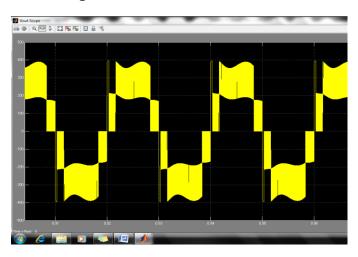


Fig. 12: Output waveform before filter Five Level Inverter



Fig. 13 & Fig. 14 shows output waveform of the Two Level & five Level inverter respectively. We need to higher value of inductor in two level inverter to achieve the same output sine waveform as achieved in Five level inverter,

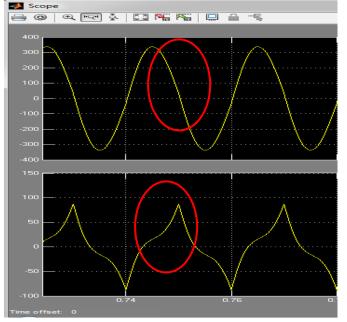


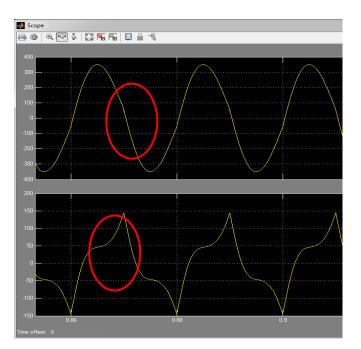
Fig. 13: Output waveform after filter with L 5500mH of Five Level Inverter

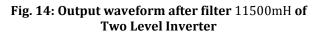
Table-1 shows comparative study of Two & Five level inverters in terms of efficiency & inductor value in the output filter circuit. Reduction of inductor value helps to achieve better efficiency due to reduced losses. Addition of two switching devices makes control part more complex compared to Two Level inverter.

Parameter	Two Level	Five Level
Inductor Use in output	11500mH	5500mH
filter		
Efficiency at 25% Load	86%	96%
Efficiency at 50% Load	86%	96%
Efficiency at 75% Load	89%	98%
Efficiency at 100% Load	89%	98%
Size of Inverter	Large	Small
Control Complexity	low	High

Table -1: Comparison with two level (filter & efficiency)

Fig. 15 shows the filter arrangement for both two & five level inverter. As shown in Table-1 value of inductor is different in Two & Five level inverter. Fig. 15 also shows the arrangement for measuring output efficiency & observing output waveforms. Final Output waveforms are shown in the fig 13 & 14.





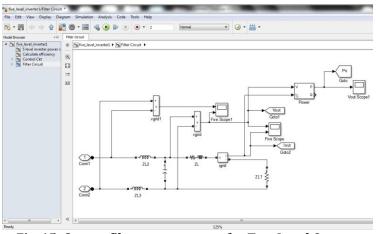


Fig. 15: Output filter arrangement for Two Level & Five level inverter

4. Conclusion

Simulation of Two Level & Five Level inverter carried out in MATLAB SIMULINK. It is observed that by using Five level inverter topology we can reduce inductance value of an inductor used in output filter of inverter which results increase in efficiency & reduce size as well as cost of inverter



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