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Synthesis and Simulation of a Three Input Binary AND Gate using Behavioral Level Modelling

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Abstract - *Illustrating the Synthesis and simulation of a three input binary AND Gate using behavioral level modelling with considering the output as a register instead of using case or conditional statements.*

The paper is a further advancement my published journal paper "Synthesis and Simulation of Binary AND Gate using Behavioral Level Modelling" in "International Referred Journal of Engineering and Science (IRJES)".

***Key Words*: AND gate, Verilog HDL[1] Behavioral level modelling[2], Xilinx 14.7, Synthesis and Simulation.**

1. INTRODUCTION

Basically we all are familiar with binary logic gates as these are the building blocks of digital circuits either complex or simple.

So basically here I am showing how a very important multiplicative operative i.e. a binary AND with three inputs can be implemented by CAD tools i.e. is synthesised and simulated using Xilinx 14.7 software.

[1] *Verilog HDL, standardized as IEEE 1364, is a behavioural and a structural case- sensitive hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits at the register-transfer level (RTL) of abstraction.*

[2] *The module is implemented in terms of desired design algorithm without concern for the hardware implementation details.*

2. CIRCUIT DIAGRAM AND TRUTH TABLE OF A THREE INPUT AND GATE

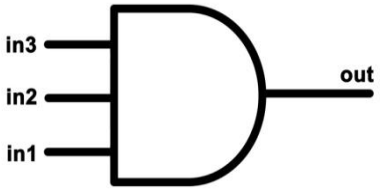

Fig.1. Circuit Symbol of Three input AND Gate

Table -1: Truth Table of a Three input AND Gate

Input in1	Input in2	Input in3	Output out (out=in1.in2.in3)
0	0	0	0
0	0	1	0
0	1	0	0
1	0	0	0
1	1	0	0
0	1	1	0
1	0	1	0
1	1	1	1

3. IMPLEMENTATION

In the implementation of a three input AND gate using behavioural level modelling, module name is myandgate with inputs: in1, in2, in3 and output: out. The output here is taken a register continuing with assigning the inputs with always statement and using relative operator to perform logical AND operation.

4. VERILOG HDL DESCRIPTION

4.1. Module Program:

```
module myandgate(out,in1,in2,in3);

input in1,in2,in3;

output out;

always @ (in1,in2,in3)

 begin

out=in1&in2&in3;

end

endmodule
```

The module program of Verilog HDL serves the purpose for providing the binary AND gate schematic layout.

4.2. Test Bench/ Simulation Program:

```
module myandgatetest;

reg in1,in2,in3;

wire out;

myandgate uut (out,in1,in2,in3);

initial

begin

$monitor ($time,"in1=%b,in2=%b,in3=%b,
out=%b",in1,in2,in3,out);

#100 in1=0; in2=0; in3=0;

#100 in1=0; in2=0; in3=1;

#100 in1=0; in2=1; in3=0;

#100 in1=1; in2=0; in3=0;

#100 in1=1; in2=1; in3=0;

#100 in1=0; in2=1; in3=1;

#100 in1=1; in2=0; in3=1;

#100 in1=1; in2=1; in3=1;

end

endmodule
```

The simulation/ test bench program associates the module program to verify the logical combinations of the gate.

5. ANALYSIS ON XILINX 14.7

5.1. Module Program and its obtained Schematic

```
20  //////////////////////////////////
21  module myandgate(out,in1,in2,in3);
22  input in1,in2,in3;
23  output out;
24  reg out;
25  always @ (in1,in2,in3)
26  begin
27  out=in1&in2&in3;
28  end
29  endmodule
30
```

Fig.2. Module Program in Xilinx

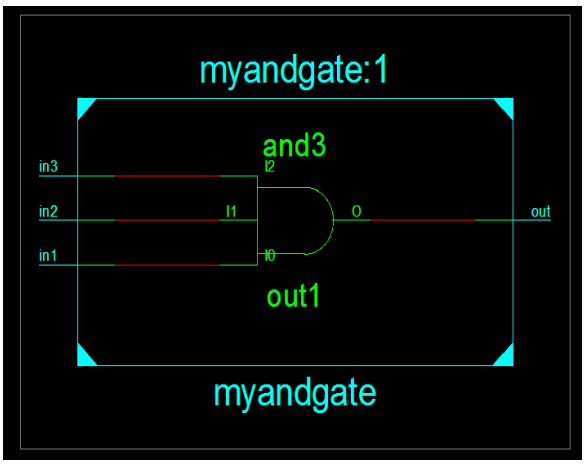

Fig.3. Synthesised Output

5.2. Test Bench/ Simulation Program and its obtained logical Simulated Verification Outputs

```
24
25  module myandgatetest;
26  reg in1,in2,in3;
27  wire out;
28  myandgate uut(out,in1,in2,in3);
29  initial
30  begin
31  $monitor ($time,"in1=%b,in2=%b,in3=%b,out=%b",in1,in2,in3,out);
32  #100 in1=0;in2=0;in3=0;
33  #100 in1=0;in2=0;in3=1;
34  #100 in1=0;in2=1;in3=0;
35  #100 in1=1;in2=0;in3=0;
36  #100 in1=1;in2=1;in3=0;
37  #100 in1=0;in2=1;in3=1;
38  #100 in1=1;in2=0;in3=1;
39  #100 in1=1;in2=1;in3=1;
40  end
41  endmodule
42
```

Fig.4. Simulation Program

Observed Simulated Outputs:

a. With inputs in1=0, in2=0, in3=0 and output out=0

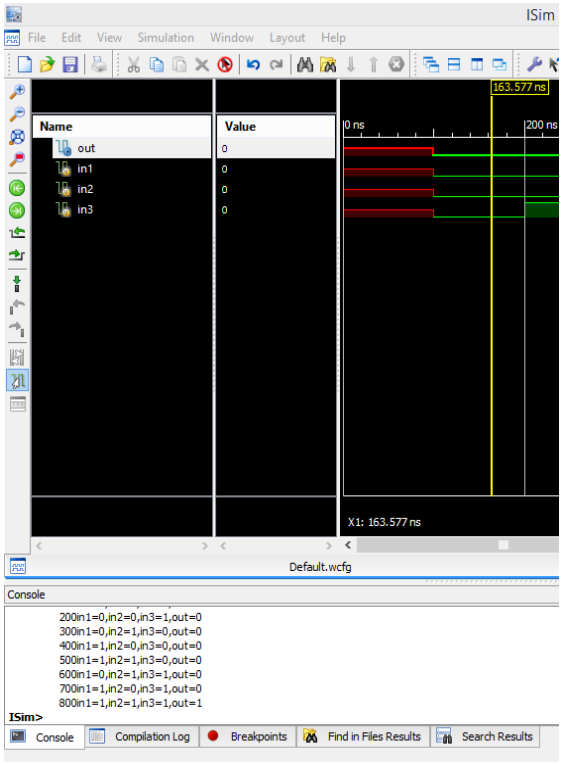

Fig. 5.1.

b. With inputs in1=0, in2=0, in3=1 and output out=0

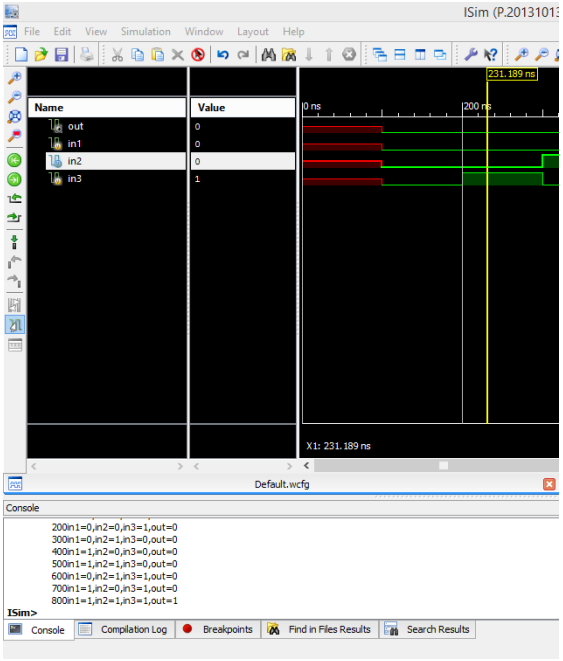

Fig. 5.2.

c. With inputs in1=0, in2=1, in3=0 and output out=0

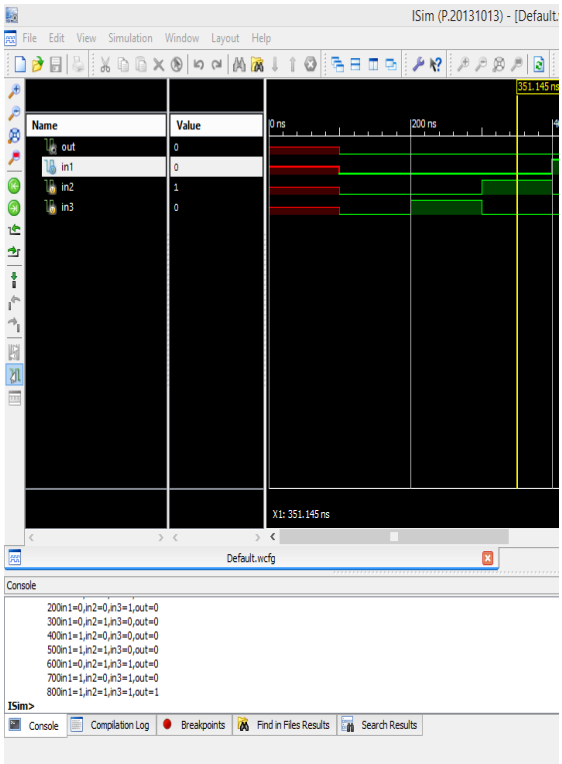

Fig. 5.3.

d. With inputs in1=1, in2=0, in3=0 and output out=0

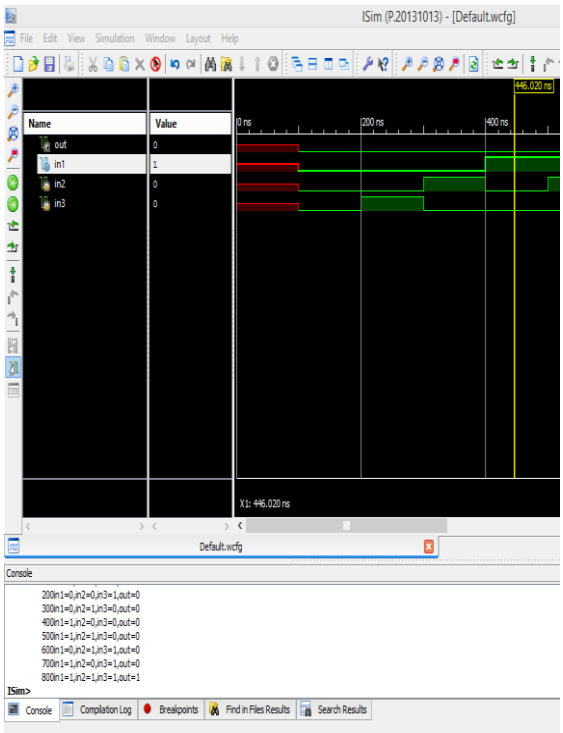

Fig. 5.4.

e. With inputs in1=1, in2=1, in3=0 and output out=0

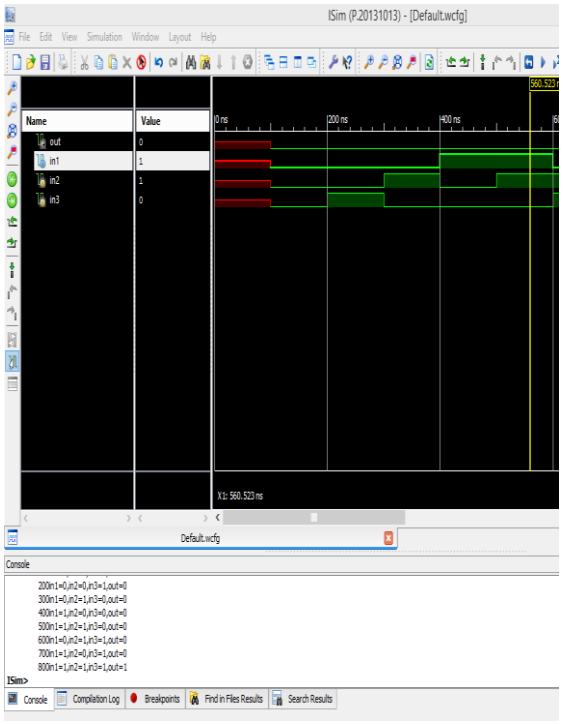

Fig. 5.5.

f. With inputs in1=0, in2=1, in3=1 and output out=0

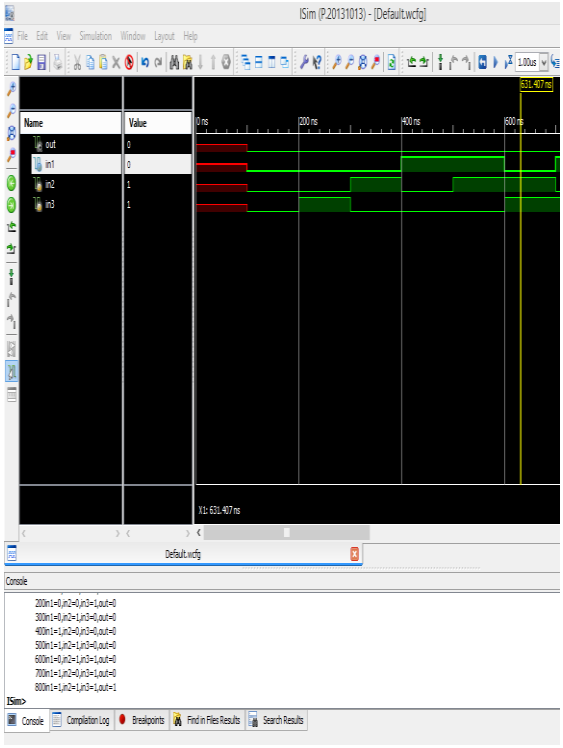

Fig. 5.6.

g. With inputs in1=1, in2=0, in3=1 and output out=0

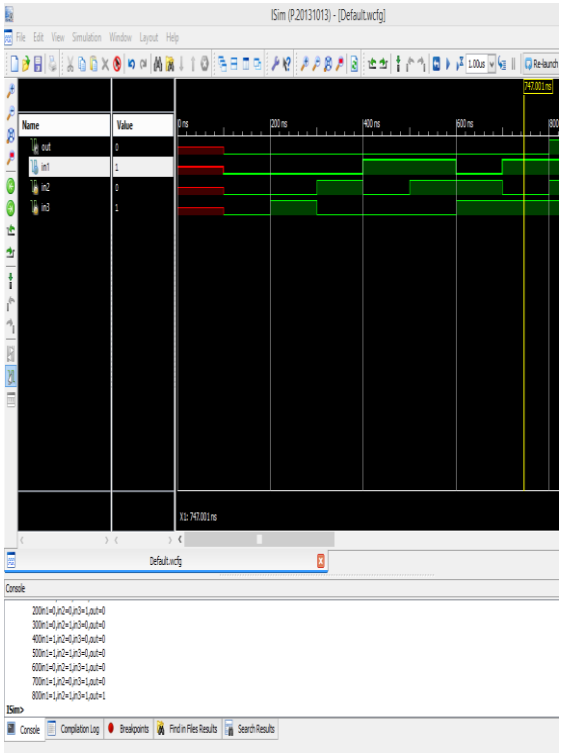

Fig. 5.7.

h. With inputs in1=1, in2=1, in3=1 and output out=1

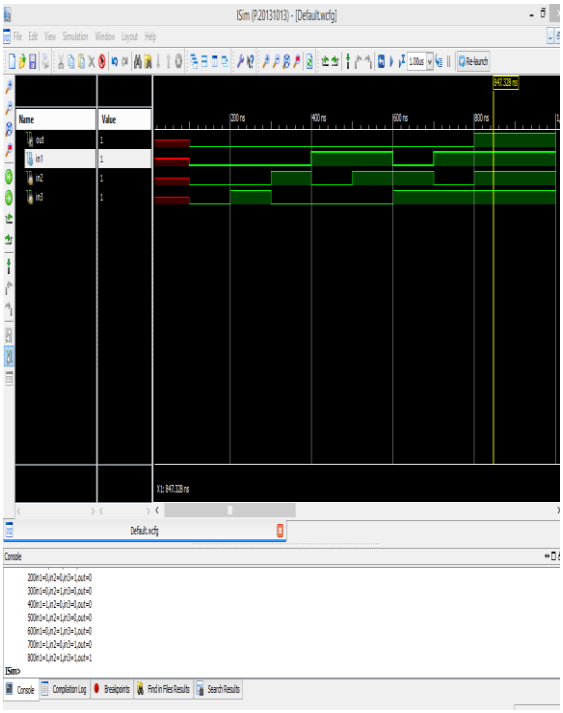

Fig. 5.8.

6. FUTURE SCOPE

Basic programming descriptions can be made easier which can be helpful in developing complex VLSI circuits with more number of inputs and also leading to its futuristic approach with using CAD tools.

7. CONCLUSION

Convincingly it has been observed that a three input binary AND gate can be easily simulated and synthesized by considering the output as a register in the module program, other than using casing or conditional statements in Behavioral level modelling.

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BIOGRAPHY

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