

# LOW POWER LOGIC CIRCUIT BASED ADIABATIC LOGIC USING VTCMOS

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**Abstract** - Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly been fueled by the fact that as circuits get smaller and faster, their energy dissipation greatly increases a problem that an adiabatic circuit promises to solve. Most research has focused on building adiabatic logic out of CMOS. However, current CMOS technology, though fairly energy efficient compared to similar technologies, dissipate energy as heat, mostly when switching. Two logic families i.e. CMOS logic and adiabatic logic have been analyzed and implemented. The simulation was conducted in Tanner EDA. Finally the power consumption is estimated and compared.

**Key Words:** Adiabatic logic, Carry looks ahead adder (CLA), low power, leakage, CMOS, substrate biasing.

## 1. INTRODUCTION

The demand for implementing ultralow power digital systems in many modern application, such as mobile systems, sensor networks and implanted biomedical systems, has increased the importance of designing logic circuits in subthreshold regime. These emerging applications have low energy as the primary concern instead of performance, with the eventual goal of harvesting energy from the environment. In subthreshold logic [2]-[4], circuits operate with a supply voltage  $V_{DD}$  lower than the transistor threshold voltage  $V_T$  and utilize the subthreshold leakage current as the operating current. Conventional CMOS logic circuits utilizing subthreshold transistors can typically operate with a very low power consumption[9], which is mainly due to the dynamic power consumption and is quadratically dependent upon the supply voltage as  $C_L f V_{DD}^2$  (where  $C_L$ ,  $f$  and  $V_{DD}$  are the load capacitance, operating frequency and the supply voltage, respectively).

Recently, adiabatic logic (or energy recovery logic) [5]-[7] style has emerged as a promising approach in strong inversion regime, to reduce dynamic power consumption significantly without sacrificing noise immunity and driving ability. These circuits achieve ultralow energy consumption by steering currents across devices with low voltage differences and by gradually recycling the energy stored in their capacitive loads, especially in low-frequency regime. Since the performance requirements are quite relaxed in many of these energy-efficient sub threshold applications

[2], [4], we believe that the adiabatic style can be used efficaciously in a sub threshold regime to make the circuit more energy efficient.

In general, the design of adiabatic logic requires a deep knowledge of the main features of the adopted logic style, such as power dissipation, leakage current impact of temperature variation, operating frequency, and noise immunity. In this paper, the behaviors of adiabatic logic in sub threshold regime are discussed in depth. To demonstrate the workability of the adiabatic logic circuits in sub threshold regime, a 4-bit carry look ahead adder (CLA) unit is adopted as a reference circuit.

## 2. SUBTHRESHOLD ADIABATIC LOGIC

### 2.1 Basic Model of MOSFET in Sub threshold Regime

Using EKV model [8], the I-V characteristics of the sub threshold pMOS device can be expressed by

$$I_{sub} = I_0 e^{\frac{(V_{SG}-V_{TH})}{n_p V_T}} \left( 1 - e^{-\frac{V_{SD}}{V_T}} \right) \quad (1)$$

Where  $I_0 = 2\eta_p \mu_p C_{ox}(W/L)V_T^2$ .  $V_{SG}$ ,  $V_{SD}$ , and  $V_{TH}$  are source to gate, source to drain, and threshold voltage of pMOS, respectively.  $V_T = (k T / q)$  is thermal voltage,  $\eta_p$  is sub threshold slope factor, and  $\mu_p$  is the mobility of pMOS device. In sub threshold regime, the threshold voltage ( $V_{TH}$ ) depends on source-to-drain voltage ( $V_{SD}$ ) through body effect and drain-induced barrier lowering. Considering these effects, threshold voltage can be expressed as follows:

$$V_{TH} = V_{T0} - \gamma V_{SB} - \eta V_{SD} \quad (2)$$

Here,  $V_{T0}$  is the threshold voltage at zero bias and  $\gamma$  and  $\eta$  are the body effect and drain-induced barrier lowering coefficient, respectively. The Drain Induced Barrier Lowering coefficient ( $\eta$ ) [8], which is a unit less quantity, can be expressed as

$$\eta = 1 / (2 \cosh(L_{eff}/2l_t)) \quad (3)$$

Where  $l_t = (\epsilon_{Si} T_{ox} X_{Dep} / \beta \epsilon_{ox})^{1/2}$  and

$$\gamma = \sqrt{(2q\epsilon_{Si} N_A / C_{ox})} \quad (4)$$

For conventional CMOS configuration (source and body are tied together), (1) can be expressed as

$$I_{sub} = K_p \exp\left(\frac{V_{SG}}{n_p V_T}\right) \left(1 - \exp\left(-\frac{V_{SD}}{V_T}\right)\right) \quad (5)$$

Where  $K_p = I_0 \exp(-V_{T0} - \eta V_{SD} / n_p V_T)$ . For the sake of simplicity, let us further simplify the magnitude of  $K_p$  by assuming,  $\eta V_{SD} / n_p V_T \ll 1$ . The value of  $\eta$  can be obtained directly from the 45-nm PTM model file. Putting the model parameters in (3) and (4),  $\eta$  will be slightly less, approximately 0.0039. Hence, we set,  $\eta \rightarrow 0.004$  for pMOS and nMOS both, thermal voltage,  $V_T = 26 \text{mV}$  at  $27^\circ\text{C}$ ,  $n_p = 1.62$ ,  $V_{SD}$  lies in the range of few milli volts to hundreds of milli volts depending on the  $V_{SG}$  of the pMOS device. In the case of a pMOS device, we get  $K_p \approx I_0 \exp(-V_{T0} / n_p V_T)$ .  $K_p$  and  $K_n$  Differ due to imbalance in zero biased threshold voltage ( $V_{T0}$ ), mobility ( $\mu$ ), sub threshold swing ( $n$ ), and soon. In 45-nm technology, as  $I_0$  for pMOS and nMOS are  $1.16$  and  $0.55 \mu\text{A}$ , respectively,  $K_p$  and  $K_n$  will be obtained by putting the value from PTM 45-nm metal gate/high- $K$  model file [11]. Hence,  $K_p \sim 1.25$  and  $K_n \sim 8.79 \text{pA}$ . By changing ( $W/L$ ) ratio, we can also tune  $K_p$  or  $K_n$  as these are directly proportional to the aspect ratio of transistors.

### 2.2 Behavior of MOSFET under ac Supply Voltage in Sub threshold Regime

In adiabatic logic circuits, ramp type supply voltage is used to slow down the charge transport mechanism [5], [10].

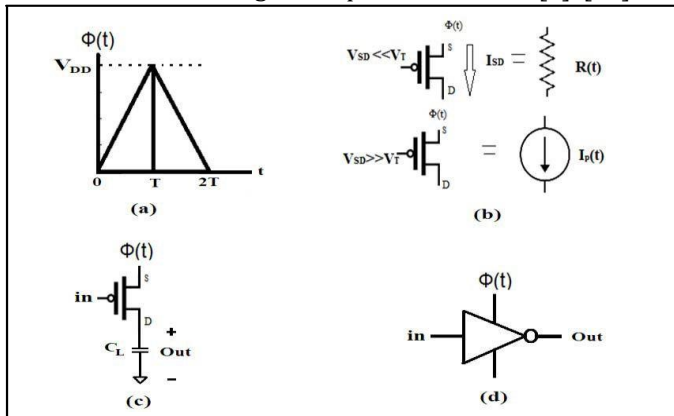


Fig. 1. (a) Clock supply voltage. (b) Equivalent circuit of pMOS under low and high  $V_{SD}$ . (c) SAL inverter circuit. (d) SAL inverter symbol.

Hence, the supply clock plays the pivotal role. A ramp type supply voltage  $\phi(t)$  is considered in Fig. 1(a), which gradually swings in between logic0 (Gnd potential) and logic1 ( $V_{DD}$ ) in time duration  $2T$ , where  $f (=1/2T)$  is the supply clock's frequency. The power supply waveform  $\phi(t)$  can be divided into charging phase, when  $\phi(t)$  ramps up from 0 to  $V_{DD}$  in  $0$  to  $T$  unit time and discharging phase when  $\phi(t)$  ramps down from  $V_{DD}$  to  $0$  in  $T$  to  $2T$  unit time. Considering the charging phase, the voltage at any time instant can be expressed as

$$\phi(t) = V_{DD}(t/T) \quad (6)$$

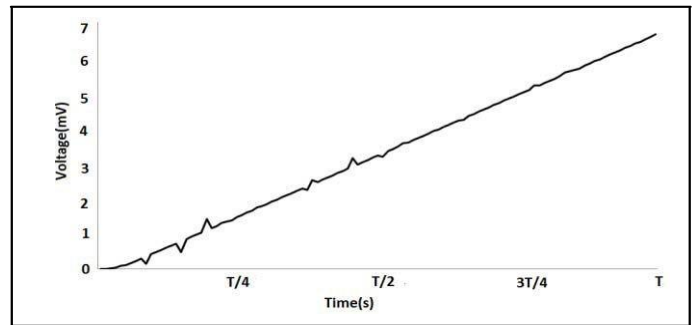


Fig.2. Variation of  $V$  with respect to time.

### 2.3 Impact of Parasitic Gate Capacitances on Variable Supply Voltage

In a sub threshold digital CMOS circuit, the gate capacitance of the transistor varies if the supply voltage ramps up (charging phase) or down (discharging phase). Due to this, a negligible amount of energy is transferred from variable supply voltage to the inputs, causing an on adiabatic loss. This non adiabatic loss of energy also brings noise or some unwanted spikes in output node voltages. Since during adiabatic switching, MOSFETs are kept under low drain to source voltages, the total gate capacitance ( $C_G$ ) of a pMOS device can be expressed as

$$C_G = C_{GD} + C_{GS} \quad (7)$$

Where  $C_{GD}$  and  $C_{GS}$  are the gate to drain and gate to source capacitances, respectively. If can be assumed that initially the gate voltage and supply voltages are at zero potential. When the supply voltage ramps up, within a short time span, the gate voltage rises gradually from 0 to  $V_{DD}$ . As a result, the total  $C_G V_{DD}$  amount of charge flows to the gate node, causing a  $0.5 C_G (V_{DD})^2$  of energy loss. When the supply voltage reaches the peak of  $V_{DD}$ , the drain to gate voltage ( $V_{DG}$ ) and the source to gate voltage ( $V_{SG}$ ) become zero, causing a current flow from the gate node to the input line. The energy associated during this event is  $C_G V_{DD}^2$ . As a result, a  $0.5 C_G (V_{DD})^2$  energy flows from the gate node to the input.

### 2.4 Impact of Leakage for Variable Supply Voltage

As leakage current is one of the pivotal concerns in sub threshold regime, total leakage energy dissipations in SAL along with the conventional one are given. Hence, leakage current is assumed to flow through the pMOS device for higher drain to source voltage drop. Under this condition, for the half clock period of supply voltage,  $\phi(t)$ , the total leakage energy Dissipation Across a pMOS can be expressed as

$$E_{leak, ad} = \int_0^{T/2} K_p \exp\left\{\frac{V_{DD}}{n_p V_T} \left(\frac{t}{T} - 1\right)\right\} \phi(t) dt \quad (8)$$

Assuming  $V_{DD} / n_p V_T \gg 1$ , we get

$$E_{leak, ad} \approx \exp\left(\frac{-V_{DD}}{n_p V_T}\right) \left\{\frac{TK_p n_p V_T}{2} \left(1 - \frac{2n_p V_T}{V_{DD}}\right)\right\} \quad (9)$$

Considering the constant dc supply voltage having the same value as the peak of  $\phi(t)$ , the total leakage across a pMOS device can be expressed as

$$E_{leak,conv} = V_{DD}TKp \quad (10)$$

### 2.5 Delay Calculation

As SAL is efficacious where instead of performance, power dissipation is major concern. For example, in implanted biomedical systems, the circuits remain active for a very small span of time and remain idle for most of the time. In such operations, much lower frequency ranges are required. Therefore, in SAL, minimization of power dissipation is the pivotal issue. Hence, we address the delay in SAL though it would be few times larger than that in the conventional one. In SAL-based digital circuits, output nodes follow the supply clock very closely during the charging and discharging periods and the output waveforms get the same pattern as the supply voltage. In general, delay can be calculated between a change in an input (50% of  $V_{DD}$  on input) and a low-to-high or high-to-low change in the output (50% of  $V_{DD}$  on input). As the supply voltage ramps up and down linearly in between 0 and  $V_{DD}$ , propagation delay would be roughly  $T/2$ , where  $2T$  is the width of total supply clock. In the worst case corner, SS and worst temperature 80 °C less than 1% variation in delay is observed where the time period is 10  $\mu$ s. Therefore, in worst case process variation of chip and die, delay would not be affected significantly. A 3% relative delay variation has been observed with three sigma variation on the path. Though process variations do not affect the propagation delay of SAL, increasing the frequencies can minimize the propagation delay. Increasing supply voltage also enhances the speed a bit. Simultaneously, power dissipation must increase with speed. However, we should keep in mind that minimizing power dissipations would be more important than decreasing the delay in SAL.

### 3. Subthreshold Adiabatic logic based 4 bit CLA

In this section, design and analysis of SAL-based 4-bit CLA are given to show the workability and the feasibility of the proposed logics. After verifying the logical functionality, we implemented an SAL-based standard cell library, consisting of common digital gates, such as buffer/inverter, two-input and three-input functions, complex gates, and special gates like half and full adder, which are necessary to implement the 4-bit CLA. For example, to implement a NAND or a NOR gate, simply the pull-up network can be placed between the supply clock and the output load capacitors, whereas an AND or an OR gate can be implemented using the pull-down network between the supply clock and the output load capacitors. In case of a NAND structure, for every input combination except  $A = B = 1$ , the output node voltage will follow the supply clock closely, and we get a triangular output waveform. When  $A = B = 1$  through parallel pMOS transistor, leakage currents will flow as the transistors will behave almost as a constant current source. A very small

amount of charge will be stored across the load capacitor, i.e., instead of ground potential, very small voltage will be dropped across the output.

Hence, we implemented the sum ( $S_i$ ) in three stages to avoid delay mismatching with the carry generation. In SAL-based 4-bit CLA, every stage will be controlled by the supply clock. Like the conventional approach, the expression of the  $i$  th sum and the  $(i+1)$  th carry output can be given as

$$S_i = A_i \oplus B_i \oplus C_i,$$

$$C_{i+1} = A_i B_i + (A_i \oplus B_i) C_i$$

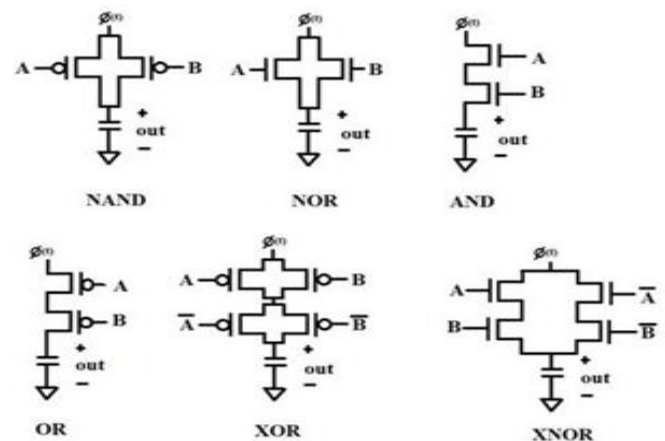


Fig 3. Logical structure of basic SAL logic gate.

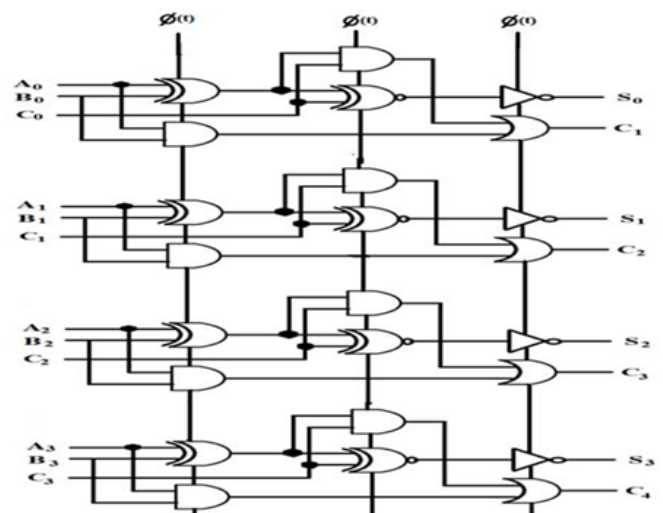
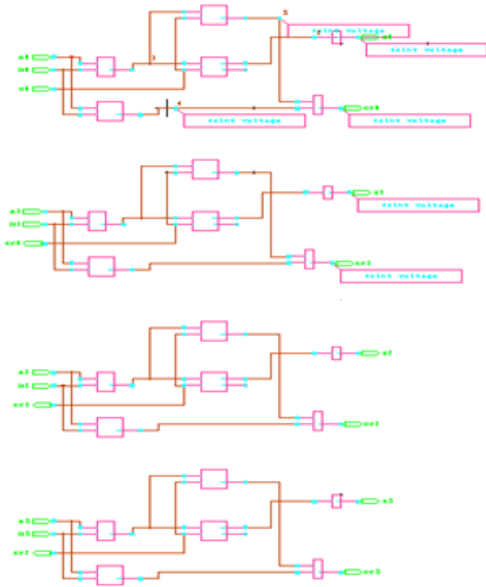


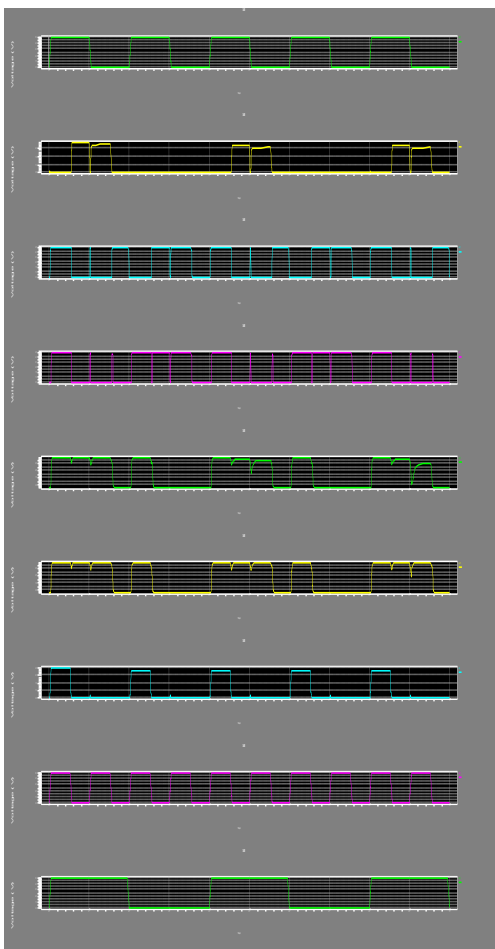
Fig 4. Logical structure for 4 bit CLA

### 4. Simulation Results

#### 4.1 Layout of 4 Bit SAL based CLA



#### 4.2 Output



### 4.3 Comparison table

S.NO	Gates Name	CMOS Logic (in Watts)	Adiabatic Logic (in Watts)
1	AND Gate	5.537651e-004	4.709910e-004
2	OR Gate	1.216141e-003	9.671850e-008
3	NAND Gate	2.087821e-004	8.292000e-008
4	NOR Gate	2.243673e-004	1.341909e-006
5	XOR Gate	1.734818e-003	6.853403e-004
6	XNOR Gate	2.430037e-003	1.124347e-003
7	Half Adder	3.084999e-003	1.375516e-003
8	Full Adder	9.031094e-003	2.463585e-003
9	D Flip Flop	4.798298e-003	1.267636e-004
10	4 bit CLA	1.223646e-001	3.493855e-002

### 5. CONCLUSIONS

This work proposes an adiabatic logic technique that would reduce the power consumption. The main idea behind adiabatic design is to transfer charge between circuit capacitance and a time varying power clock source. This scheme enables the charge transfer to occur in a controlled manner, limiting the currents and thus decrease the energy dissipation across the active devices. The simulation result shows that the adiabatic 4 bit carry look ahead adder circuit consumes very low power.

## 6. Future work

### 6.1 Variable Threshold CMOS (VTCMOS)

One of the efficient methods to reduce power consumption is to use low supply voltage and low threshold voltage without losing speed performance. But increase in the lower threshold voltage devices leads to increased sub threshold leakage and hence more standby power consumption. Variable Threshold CMOS (VTCMOS) devices are one solution to this problem. In VTCMOS technique threshold voltage of the low threshold devices are varied by applying variable substrate bias voltage from a control circuitry.

VTCMOS technique is very effective technique to reduce the power consumption with some drawbacks with respect to manufacturing of these devices. VTCMOS requires either twin well or triple well technology to achieve different substrate bias voltage levels at different parts of the IC. The area overhead of the substrate bias control circuitry is negligible. It will completely to remove the negative feedback voltage within the circuit. The negative feedback voltage will get dissipated through ground

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