

Design of Complex Multiplier for FFT implementation using Vedic Mathematics

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Abstract - Multiplication of complex number finds numerous applications in Science and Engineering. Complex multiplication design can be the most time and area consuming operations in DSP. Hence, an attempt is made in this paper to reduce the complexity of complex multiplier by using Vedic mathematical techniques. Vedic mathematics contains 16 sutras which are mathematical short hands for range of operation covering basic arithmetic's, algebraic and trigonometric operation to more complex calculus operation. Out of 16 sutras two sutras are used for multiplication. Traditionally, the complex multiplier suffer from low speed due to more number of partial product and carry propagation. A complex multiplier is designed using Urdhva Tiryagbhyam sutra. The results prove that the proposed vedic multiplier is faster than the conventional multiplier. A 8 point radix 2 Decimation in Frequency(DIF) Fast Fourier Transform(FFT) algorithm is implemented using the proposed vedic multiplier.

Key Words: Complex Multiplier, Vedic Mathematics, Urdhva Tiryagbhyam sutra, Partial product reduction, Fast Fourier Transform.

1.INTRODUCTION

FFT is a highly elegant a

nd efficient algorithm, which is still one of the most used algorithms in speech processing, communications , frequency estimations, etc, one of the most highly developed area of DSP. FFT is an algorithm proposed by Cooley and Turkey in 1965.It is a highly efficient procedure for computing the DFT[1] of finite series and requires less number of computations than that of direct evaluation of DFT. FFT is based on decomposition and breaking the transforms and combining them to get the total transform. It makes use of symmetry and periodicity properties of twiddle factor W_N to effectively reduce the DFT computation time[2] . Addition and multiplication are the two major arithmetic operations involved in the computation of the FFT algorithm. The design of the complex multiplier influences the overall computational complexity of the FFT algorithm. Hence vedic mathematics is used in the design of complex multiplier to reduce the computational complexity, area and power. In this paper a complex multiplier is designed using Urdhva-Tiryagbhyam sutra.

1.1 VEDIC MATHEMATICS

Vedic mathematics is a book written by the Indian Hindu Priest Bharati Krishna Tirthagi and first published in 1965[3]. Vedic mathematics is a collection of techniques, sutras to solve mathematical arithmetic in easy and faster way It consists of 16 sutras (Formulae) and 13 sub-sutras (sub-formulae) which can be used for problems involved in arithmetic, algebra, geometry and calculus[4]. From all the 16 sutras in the ancient vedic mathematics Nikilam Navatashcaramam Dashatah sutra and Urdhuva-Tiryagbyam sutra can be used for complex number multiplication[5]. The meaning of this Nikilam is "All from 9 and the last from 10". Nikilam sutra can also be applied to large numbers. Urdhuva-Tiryagbyam method is another method used for multiplication. Urdhuva means " Vertically and crosswise". Vertically means straight above multiplication and crosswise means diagonal multiplication and taking their sum. It has the advantage that it reduces the multi bit multiplication into single bit multiplication and addition[6]. This results in the generation of all the partial products in one step which further reduces carry propagation that occurs from LSB to MSB during the process of addition. . It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in generation of partial products and their summation is obtained using UrdhvaTiryakbhayam.. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers.

1.2 COMPLEX MULTIPLIER

Multiplication of two complex number is a very frequent operation in many signal processing algorithms. A complex multiplier is a combination of real number and imaginary number.[7] In general two complex numbers $(a+jb)$ and $(c+jd)$ are multiplied as follows $(a+jb)(c+jd)=(ac-bd)+j(ad+bc)$. Fig. 1 shows the block diagram of the complex multiplier. Here 4 multipliers and 3 adder/subtractor blocks are used. At first the two complex numbers $(a+jb)$ and $(c+jd)$ are fed as input to the multiplier as shown in Fig.1 . The multiplier generates the partial products ac, bd, ad and bc . Then the sum and the difference between the partial

products are computed using adder and subtractor respectively.

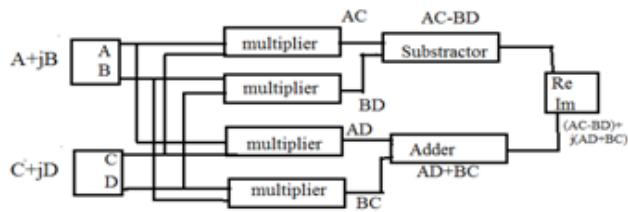


Fig-1: Basic block diagram of complex multiplier

2. Fast Fourier Transform

The general formula used to compute the N point DFT of the sequence is

$$X(k) = \sum_{n=0}^{N-1} x(n)W_N^{kn} \quad k = 0, 1, 2, \dots, N-1$$

$$W_N = e^{-j\frac{2\pi}{N}}$$

DIT(Decimation in Time) and DIF(Decimation in Frequency) are computationally intensive algorithms used to compute the DFT[8]. The two algorithms exploit the symmetry and periodicity property of the phase factor. Moreover the computational efficiency of the algorithm is made possible by adopting divide and conquer approach. The divide and conquer technique is a powerful tool that reduces the complexity by dividing the problem into a number of sub problems. The answers of the sub problems are glued recursively to obtain the result of the larger problem. The N point DFT is decimated into smaller DFT's. The Fig.2 shows the signal flow graph of 8 point radix 2 Decimation in Time algorithm. The arithmetic complexity of N² in the direct computation of DFT is reduced to Nlog₂N resulting in the improvement of speed in the computation of DFT. The input is in the bit reversed order and the output is in the normal order. Here the DFT is computed in 3 stages[9]. The first stage computes four two- point DFT, then second stage computes two four-point DFT and the final stage combines the two four point DFT to compute the eight point DFT. At every stage a complex number is multiplied with the twiddle factor and then added and subtracted with the other complex number. This basic computation is shown in Fig.3 called butterfly diagram of 2 point radix 2 DIT FFT algorithm

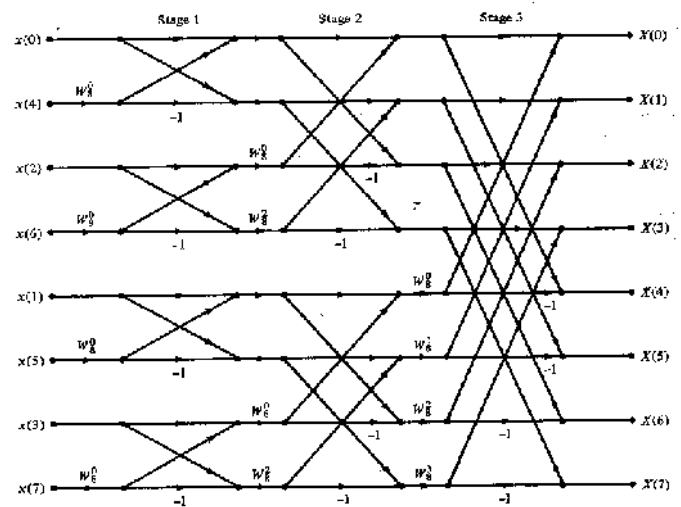


Fig.2 Signal flow graph of radix 2 DIT-FFT algorithm

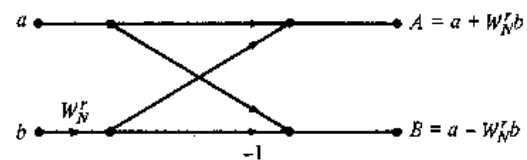


Fig.3 Butterfly diagram of DIT-FFT algorithm

The choice of multiplier used in the design of the FFT influences the computational complexity and hence the overall performance of the FFT. This paper proposes a complex multiplier using vedic mathematics.

3. RESULTS

In this paper vedic and Booth multipliers are designed to compare the performance parameters. The results prove that the application of vedic algorithm to multiplication reduces the area and power dissipation of the multiplier. Vedic multiplier exhibits a considerable improvement in operating frequency when compared to the Booth multiplier. Similarly the design of the proposed complex multiplier using vedic algorithm with divide and conquer approach shows considerable improvement in area, power and operating frequency when compared to the complex multiplier designed using Booth algorithm. The proposed complex multiplier is coded in HDL and simulated using modelsim .Fig.4 and Fig.5 shows the simulation results of Booth multiplier and vedic multiplier respectively. The multipliers are synthesized using Quartus II.

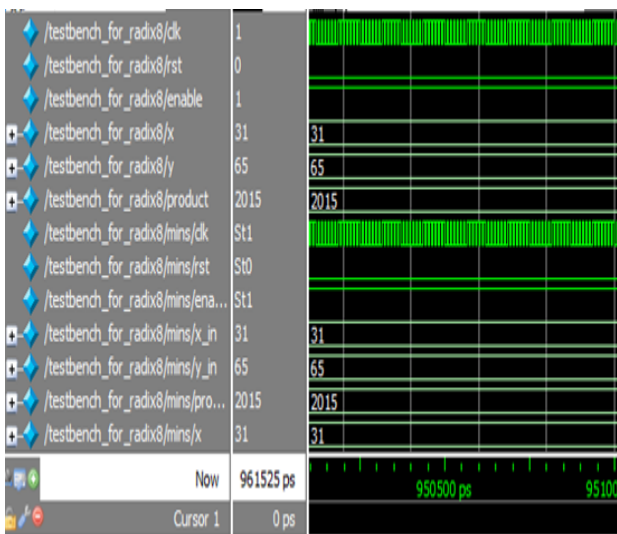


Fig.4 Simulation result of Booth multiplier.

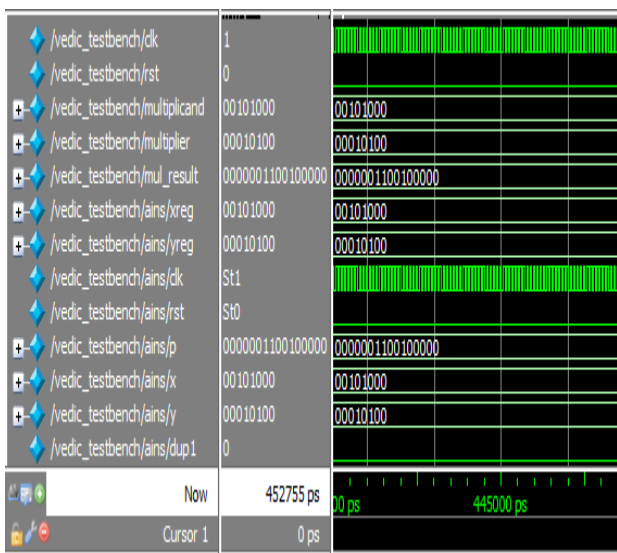


Fig.5 Simulation result of vedic multiplier.

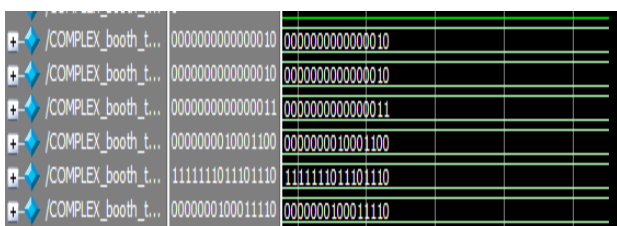


Fig.6 Simulation result of complex multiplier using Booth algorithm

Fig.6 and Fig.7 shows the simulation results of the complex multiplier designed using Booth algorithm and vedic mathematics.

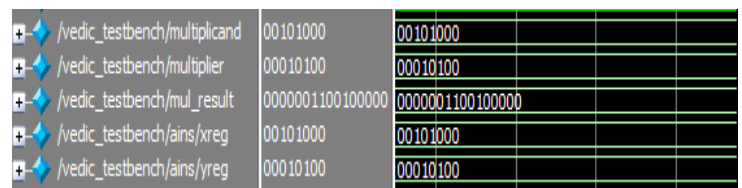


Fig.7 Simulation result of complex multiplier using vedic mathematics

The performance of all the units designed are compared based on area, operating frequency and thermal power dissipated. From the results tabulated from Table.1 it is clear that the area of the proposed complex multiplier is less when compared to the conventional multiplier.

Table -1: Flow summary and Power report using Quartus II

MULTIPLIER	AREA(logic elements)	SPEED MHZ	POWER (mW)
VEDIC MULTIPLIER	203	496.03	63.75
BOOTH MULTIPLIER	226	227.43	86.72
COMPLEX MULTIPLIER USING VEDIC	1629	439.37	84.59
COMPLEX MULTIPLIER USING BOOTH	1675	214.13	92.37

An efficient 8 point radix 2 Decimation in Frequency FFT is implemented using the proposed vedic multiplier. The DIT FFT algorithm is coded in HDL and simulated using Modelsim. Fig.8 shows the simulation result of DIT-FFT algorithm.

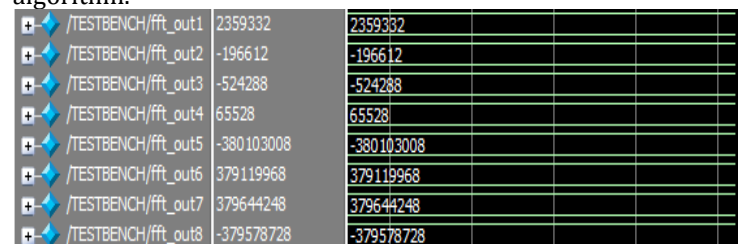


Fig.8 Simulation result of radix 2 DIT-FFT algorithm.

Table 2 summarizes the area, speed and power of the 8 point radix 2 DIT FFT algorithm using the proposed complex multiplier

Table 2: Flow summary of DIT FFT

AREA(logic elements)	SPEED (MHz)	POWER DISSIPATION (mW)
1000	439.37	92.47

4. CONCLUSION

In this paper, complex multipliers are designed using vedic mathematics and Booth algorithm. The results prove that vedic mathematics is more efficient than booth algorithm. Performances are compared in terms of area, speed and power dissipation. The performance of the proposed multiplier is greatly improved due to the reduction in the number of partial products. The divide and conquer technique used in the design increases the operating speed of the proposed complex multiplier. The results in Table 1 reveals that the implementation of the conventional multiplier requires more area and power. Moreover the operating speed of the proposed vedic multiplier is high when compared to the conventional multiplier. A 8 point radix 2 DIT FFT algorithm is implemented using the high speed complex multiplier designed using vedic mathematics

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