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REDUCING POWER, LEAKAGE AND AREA OF STANDARD CELL USING LECTOR STACK

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Abstract: *Dynamic power, spillage, and area are the important factor of the ASIC. in this paper we decrease these factors using different approach .this approach depends on an outline of edge rationale entryways (TLGs), it was jointed with customary standard-cell configuration stream. The edge entryway acts as a multi-input, single output, edge-activated flip flounder, which controls the capacity during edge clocking. A little number of cells can register an arrangement of the capacities. For this the leakage current due to sub threshold voltage was reduce. The leakage power in digital circuits was unavoidable. So we use two techniques for reducing the leakage power which are Transistor stacking and self-adjustable voltage level circuit. In scaling technology, the power density increases 40% for every generation. So every design needs application and product based technique.*

Key Words: Logic decomposition, low power (LP), technology mapping, threshold logic, MTCMOS.

1. INTRODUCTION

Logic synthesis and restructuring to reduce switching activity, gate sizing, technology mapping, retiming, and voltage scaling are a few ways to reduce the leakage. The transistor stacking is the well-known technique to reduce the power due to leakage. Thus, it was used in micro architectures, memory, compilers, OS and other digital circuits. In this paper, a TLG methodology is used for solve the problems in the ASIC design.

This methodology includes the circuit architecture, circuit library and the set of functions. The library cells, and a technology mapping algorithm using TLGs.

The resulting circuit that is hybrid circuit has the combinational of conventional logic gates and threshold logic cells. It gives the result of the circuit and their conventional logic equivalents. First we have known architecture, operation, and characteristics of pNAND cells and then we analysis to connect the pNAND cells into a general ASIC circuit. From this connection we reduce the power and leakage in the circuit without any tenner in performance. Since the hybrid circuits will consist of conventional standard cells (e.g., NAND, NOR, AOI, MUX, and so on) and pNAND cells.

2. NEW ARCHITECTURE FOR A THRESHOLD GATE

For a threshold gate here we use a different logic method that is used PNAND cells with different ways. Another way is used during clocking in PNAND cells referred as multi-input edge-triggered flip- flop.

2.1. Lector Technique:

To solve these problems we go for lector logic Basic principle. It was used in stack effect only. In this technique two extra transistors (one PMOS and one NMOS) are used .it was placed between pull down and pull up network. These extra transistors are control their self so it was also called as Leakage Control Transistors (LCT). The gate of each Leakage Control Transistors is controlled by the source of other transistors. In this type of arrangement one of the Leakage Control Transistors always remains in its near cut off region.

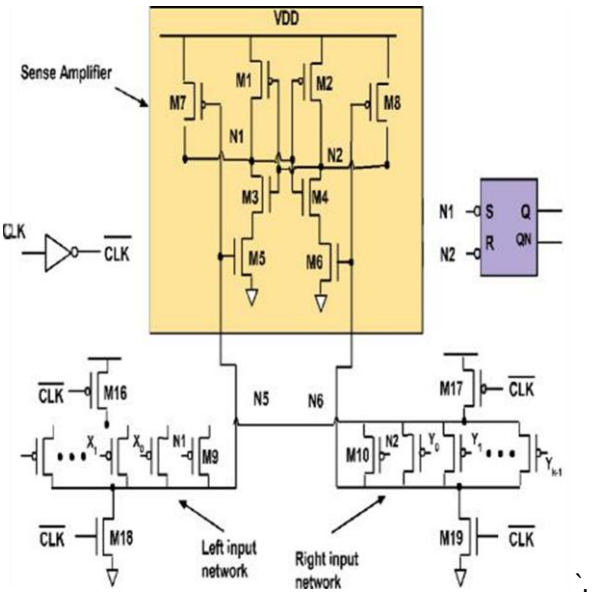

FIG- 1: Architecture of PNAND Cell

In the Lector based two input NOR gate circuit „A" and „B" are input nodes and „Y" is output node. Two NMOS transistors are connected in parallel, two PMOS transistors are connected in series and two transistors M1 (PMOS) and M2 (NMOS) are connected in series. These two transistors are Leakage Control Transistors (LCTs), which is connected between pull up and pull down network. Gate terminal of M1 is connected to source of M2 and gate of M2 is connected to source of M1.

In the digital circuits, the threshold voltage reduction was done by the voltage scaling, which was increases the leakage current and also increases the static power dissipation.

A lector technique was remit the leakage current without any grow in the dynamic power dissipation. In the past circuits uses the LCT method which was not fully connected with other transistors any one transistor not connected, these transistors are increase the overall power.

3. LEAKAGE REDUCTION TECHNIQUES:

There are two techniques was used to reduce the leakage current better than the past technique. One is transistor stacking and another one is self-adjustable voltage level circuit. Transistor stacking: Lector stack technique is a effective technique. This approach was used in both high threshold and low threshold voltage transistors, so it can be used in all VLSI circuits. Techniques for leakage power reduction can be divided into following two categories. One is state-saving technique and another one is state-destructive techniques where the current Boolean output value of the circuit might be lost. In the state-saving technique where the circuit state is retained that is it was prevent the values. In the state-destructive technique where the output values are not prevent.

3.1. Circuit working using lector stack:

In this technique, each transistor in the network is duplicated with both the transistors regard. For turn off the transistors, duplicated transistors causes the reverse bias between the gate and source. The sub-threshold current is dependent on gate bias, it was used to obtain the substantial current reduction. It overcomes the limitation with past technique by prevent the state but it takes more time to turn on. The threshold gate with k inputs, referred to as PNAND-k. It consists of three main components, Two groups of parallel PFET transistors, A sense amplifier (SA), A set–reset (SR) latch. The cell is operated in two phases one is reset where the CLK = 0 and evaluation where the CLK 0 → for the moment.

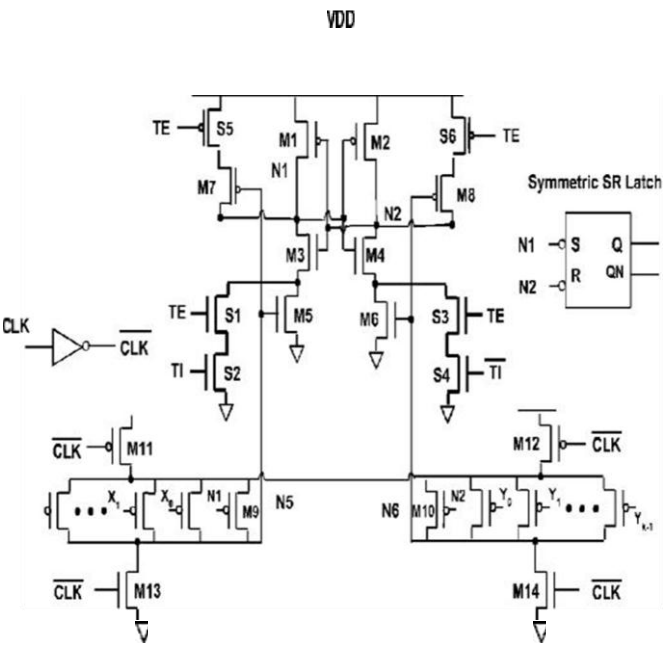

Fig-2: PNAND Cell design with scan

4. SIMULATION RESULT

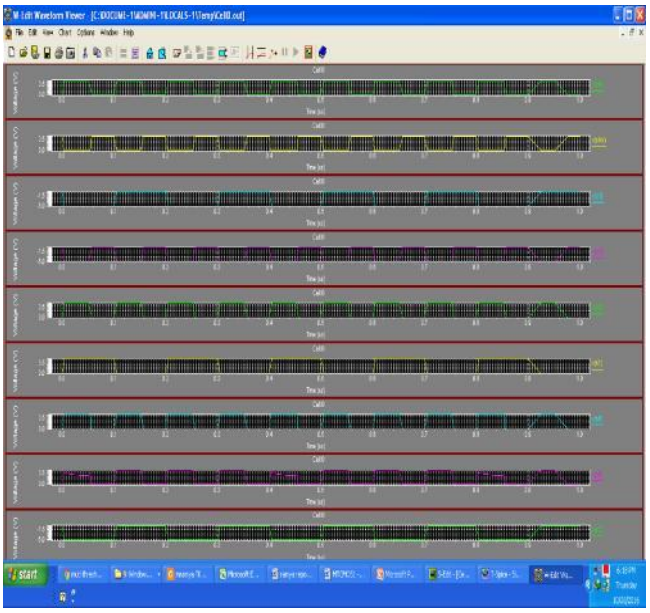

Fig.4 simulation result for pnand cell

Table-1 Variation in the Dynamic Power

Circuit	conventional	Hybrid	% Reduction
Multiplier	2.9289	1.7248	41
Filter	8.6543	4.8469	44
FPU	4.6576	3.2108	30
MIPS	6.9876	5.5251	35
AES	3.079	2.0606	33

5. CONCLUSION

The power and leakage was not fully removed from the digital circuit only reduce the amount voltage. So we use different techniques that are lector and PNAND to reduce these factors from this technique the current was decreases up to 60%.

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