

CLOSED LOOP SIMULATION AND IMPLEMENTATION OF DIGITAL INTEGRAL CONTROL OF SYNCHRONOUS BUCK CONVERTER

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Abstract - In the consumer electronic industry buck converters are the most popular converters used now-a-days. Among that Synchronous buck converters are becoming the industry standard because of their superior performance and higher efficiency. In this paper modeling and simulation of synchronous buck converter in digital mode is carried out. Now-a-days digital controllers are becoming popular because of their advantages like reprogrammability, immunity to analog component variations, flexibility etc. In digital controller the two nonlinear quantizes namely the analog-todigital converter (ADC) and digital pulse width modulator (DPWM) are used. These blocks regulate the output voltage effectively against the input voltage and load current perturbations.

Key Words: Buck Converter, Synchronous, ADC, DPWM.

1. INTRODUCTION

DC-DC converters are used to carry out the efficient transfer of energy from the input to the output of the converter. The input voltage of the converter can be stepped down (buck converter), stepped up (boost converter), or inverted (buck-boost converter). Among other converters buck converter[1] is popular because it needs very low voltages of about 5V or 3.3V which is required by the processor ICs[2]. These converters are used in applications requiring power levels from less than 1W to over 100MW [3]. The conventional buck converter typically employs a MOSFET and a freewheeling diode. These semiconductor devices have conduction losses due to their "ON "state resistances. The power losses in the converter are mainly due to diode's forward voltage of about 0.6V to 0.7V. This has lead to the development of Synchronous buck converter topology (fig 1) where the diode is replaced with another MOSFET, is often employed to meet better performance and higher efficiency. Replacing the diode with another MOSFET reduces the typical 0.5V-to-1V diode drop to about 0.3V or less, resulting in typical circuit efficiency improvements of around 5% and higher. This topology (synchronous buck converter) derives its name from the control method of the

two power MOSFETs; the ON/OFF control is synchronized in order to provide a regulated output voltage and also to prevent the MOSFETs from turning on at the same time. In order to prevent shoot-through the MOSFETs are controlled synchronously [1]. Shoot through occurs when the two MOSFETs are both on at the same time, providing a direct short to ground.



Figure-1: Closed loop control Synchronous buck converter

The output of the converter should remain stable regardless of the changes in the input voltage, load current, and age of the components. This can be achieved through the use of control circuits to regulate the dc output voltage against load and line variations. Here the control technique employed is the digital controller which consists of ADC, Digital compensator and DPWM blocks which gives the accurate results. In this work the modeling and simulation of a synchronous buck converter is undertaken. In section II the working principle of synchronous buck converter is explained. In section III the modeling of synchronous buck converter is outlined. In section IV the simulation results are discussed with the aid of MATLAB/Simulink software .And finally in section V the conclusion of the work is presented.

2. WORKING PRINCIPLE

A synchronous buck converter is a modified version of the basic buck converter circuit topology in which diode, D, is replaced by a second switch, S2. This modification is a tradeoff between improved efficiency and increased cost. The main switch is S1 and auxiliary switch is termed as

S2.When S1 is off and S2 is on, current flows upward out of the drain of S2. The advantage of this configuration is that the second MOSFET will have a much lower voltage drop across it compared to a diode resulting in higher circuit efficiency. This is especially important in low-voltage, high- current applications. The second MOSFET will have an extremely low voltage drop due to an on-state resistance as low as in terms of milliohms. This circuit has a control scheme known as synchronous rectification. The second MOSFET S2 is known as synchronous rectifier. The two MOSFETs must not be on at the same time to prevent a short circuit across the source, so a dead time is built into the switching control-one MOSFET is turned off before the other is turned on. A diode is placed in parallel with the second MOSFET to provide a conducting path for inductor current during the dead time when both MOSFETs are off.



Figure -2: Synchronous buck converter

3. MODELING OF SYNCHRONOUS BUCK CONVERTER

In all switching converters, the output voltage V(t) is a function of the input voltage Vg(t), the duty cycle D(t) and the load current, i load (t), as well as converter circuit element values[5]. The important equations that describe the operation of the converter are given below,

The current through the inductor is given by the equation,

$$diL/dt = (1/L) (VgD-iLRL-V0)$$
(1)

And the change of voltage across the capacitor is given by,

$$dvc/dt = (1/C) (iL - io)$$
 (2)

The output voltage is given by the equation

$$V0 = Vc + Resr(iL - i out)$$
(3)



Figure -3 :Functional block diagram

Figure 3 gives the functional block diagram illustrating the dependence of V on Vg, D, i $_{load}$ [5].

The buck converter model is given in figure 2. This block represents the power section modeling where inductor current and capacitor voltage are the state variables. The operation of a converter is said to be either open-loop, when there is no feedback connected to the output of the converter or closed-loop when a feedback is connected to the output of the converter. In open loop there is no way of controlling the output parameter even when unwanted perturbations occur in the input or output of the converter. In closed- loop, however, a degree of control over the output can be achieved through the use of a feedback network.



Figure- 4: Digital controller block diagram

The digital controller block diagram is shown in the fig. 4

The output voltage is compared with the reference voltage and is given to the ADC(ZOH) block which holds the value of error and this error signal is given to quantizer and the ADC limits are set. After applying ADC limits, the signal is given to PI controller and then to DAC(Digital-to-analog) quantizer, to which DAC limit is applied. Finally the output is obtained and given as pulses to the switches.



Figure- 5: Control Section

4. SIMULATION RESULTS

The results for the simulation of the synchronous buck converter are given in this section. It can be seen that the converter steps down the input voltage from 5V to 2V as expected. The transient that is common with most of the converters can be seen at the start of the simulation.



Figure-6: Output Voltage Waveform.

The unwanted transient in the output voltage has been removed and the converter steps down the voltage to 2V as expected. The above figure 6 gives the output voltage waveform. A digital integral-controlled Buck converter with the specifications listed in table-1 is studied in this paper. According to the specifications the results are verified with the simulation.

5. SPECIFICATIONS

Parameter	Value	Unit
Input voltage	5	V
Output voltage	2	V
Inductor(L)	4.7	μН
Inductor ESR (R _L)	200	mΩ
Output Capacitor(C)	10	μF
Capacitor ESR(R _c)	100	mΩ

Table-1: Specifications of the synchronous buck converter

6. HARDWARE IMPLEMENTATION

For implementing it in hardware two MOSFET switches, capacitor load resistor, buffer IC 4047, one 89S52 microcontroller board and oscilloscope is required.

Supply for the converter is taken from regulated power supply as dc voltage. This voltage is applied directly to the MOSFET switch as this waveform is pulsating dc a filter capacitor is used to remove the ripples. Filter circuit consists of inductor and capacitor. After this microcontroller is used as a feedback block and so it is given to it which controls the switching of MOSFETs. If any disturbances arise at the output of microcontroller then the signal is given to the 4047 IC chip which in turn generates the square pulses based on the received instruction by microcontroller. So a fixed dc voltage is obtained at the output.



Figure-7: Hardware Implementation

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Figure-8: Gate Pulse

The figure.8 represents the gate pulses which are given to the gate of MOSFET switch from the buffer IC 4047 which is controlled by the microcontroller.



Figure-9: Output Voltage

The figure.9 represents the output voltage obtained from the hardware of synchronous buck converter.

6. CONCLUSIONS

The modeling and simulation of a synchronous buck converter is carried out in this work. A transient and a steady-state error are observed from the result of the simulation. To solve these problems and to tackle the line and the load current variations a feedback is connected to the converter using a digital integral controller. The results show that the feedback circuit is very effective in handling the problems identified above. The transient is eliminated and the steady-state error is effectively reduced to zero. 1) M. H. Rashid, Power Electronics: Circuits, Devices and Applications, 3rd edition, Pearson, 2004

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