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Noor's Algorithmic Flow of Electronics and Communication Engineering

Noor Ul Abedin[1]

[1]*Assistant Professor, Dept. of Electronics and Communication Engineering, Deccan College of Engineering and Technology, Telangana State, India*

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Abstract – *Showcasing a simple and basic algorithm of a particular section of engineering and technology is very important as it guides the one and ones towards their role in their field of engineering and technology. This basic algorithm of electronics and communication engineering is tried to elaborate in the best possible manner so as to have a clear fundamental of the field.*

Key Words: **Analog Electronics, Digital Electronics and Communication.**

1. INTRODUCTION

There are three basic backgrounds of electronics which are analog electronics, digital electronics and communication. With the medium of a flow chart I will depict how electronics and communication engineering works realistically and how this algorithm is necessary for understanding the field of electronics and communication engineering.

2. FUNDAMENTAL BLOCKS OF ELECTRONICS AND COMMUNICATION

There are two basic fundamental blocks as everyone knows i.e.

1. **ELECTRONICS**
   - Analog Electronics
   - Digital Electronics
2. **COMMUNICATION**
   - Analog Communication
   - Digital Communication

3. ALGORITHM FLOW CHART

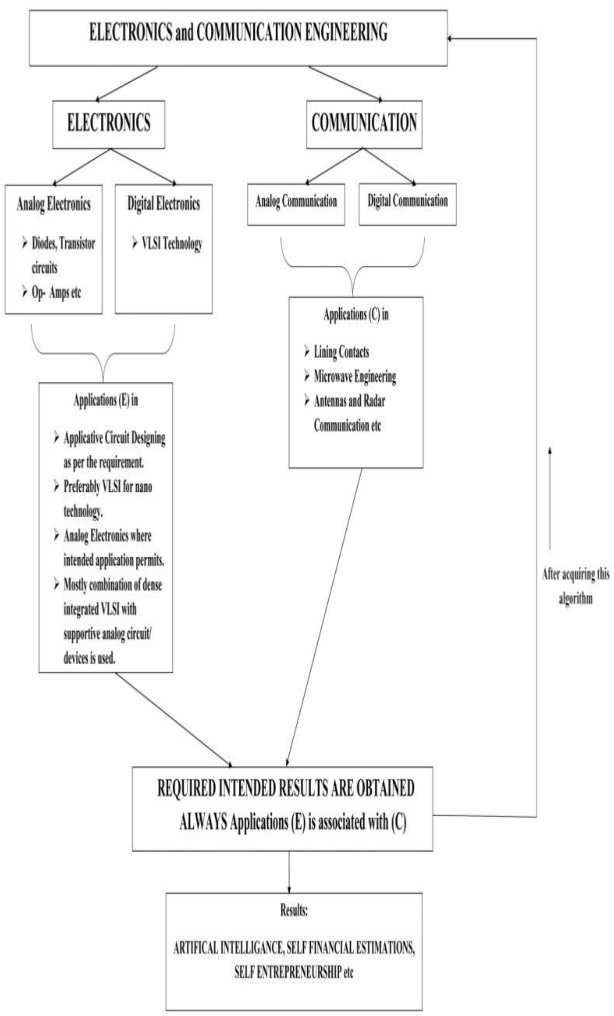

Fig.1. Noor's Algorithm Flow Chart

4. WORKING OF THE ALGORITHM

As already familiar that this field is verily related to electronics and communications i.e. at here I can say that analog electronics, digital electronics, analog communication and digital communication are interrelated/ dependent on each other depending on the intended necessity which is our ultimate aim which is feasibly obtained by the algorithm.

4.1. Analog and Digital Electronics

Preference to analog electronics is the basic fundamental engineering step towards electronics and communication as its provides us an idea how basic circuit designing using verily visible physical analog components is accomplished further providing the basic background of understanding op- amps and necessity of digital electronics.

Analog device and their circuits such as diode, transistors: BJTs, FETs are majorly used in analog electronics as the key analog elements supported by various simple and compound networks.

Major circuit works which required major analog device/ devices and their associated networks as stated above would be easily performed by using a single Op- amp IC, thus reducing the amount number of analog devices, their possible networks and also the size of the circuit.

No doubly Op- amp has eased the circuit designing but it was limited to a certain extent, this extent was been able to extended and bounded as per our needs with the help of digital electronic leading to design dense integrated circuits using CAD tools and ultimately leading to VLSI technology.

4.2. Analog and Digital Communication

Communication is the second major sector, when seeing a communication system the two analog and digital communication signals are commonly used together. As a applicative system that processes a signal uses both the signal converters the best elaboration is a DSP Processor and a TCP/ IP network.

The preference of going towards analog signals is there good performance over longer distances and the on the other hand use of digital signal makes it easier for the processor to perform their functionalities.

Therefore in many of the systems we observe the use of both analog and digital signals.

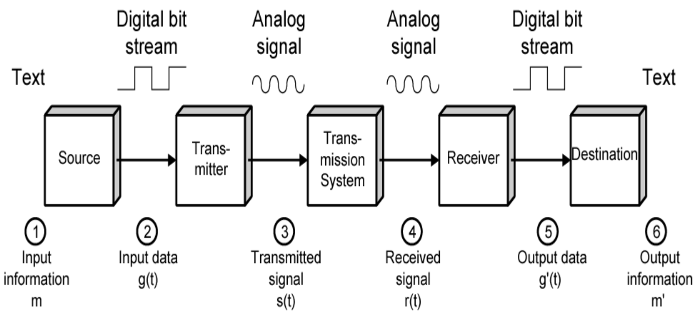

Fig.2. Data Communication System Model

4.3. Applications of Electronics (E) and Applications of Communication (C):

When the intended purpose fulfils with analog circuitry it suits the best, when dense integration/ nano circuitry is required we move onto digital circuitry and in majority of the device we give preference to a circuitry which is digital design with analog devices/ circuit. Similarly based on these the communication can be accomplished in many routes such as lining and wireless. Microwave engineering, Antennas and Radar are the major modes through which high level is accomplished.

4.4. Result

When the topologies of analog and digital are verily understood the engineer will have an exact result obtained as per his desired application and purpose.

Engineering applications such as artificial intelligence, self-financial estimation and self entrepreneurship and may more can be easily framed and executed.

5. PRACTICAL COMPARISON

Illustrating with the help of a full adder, the full adder can be implemented in by hardware selected ICs, in digital electronics the same full adder can be implemented by using HDL.

The feasibility of digitally generated full adder is more as this can be easily associated with any complex circuitry where its necessity is there and if not willingness to use can be easily removed where as analyzing these particular aspects on analog backgrounds becomes difficult and utilizes more time.

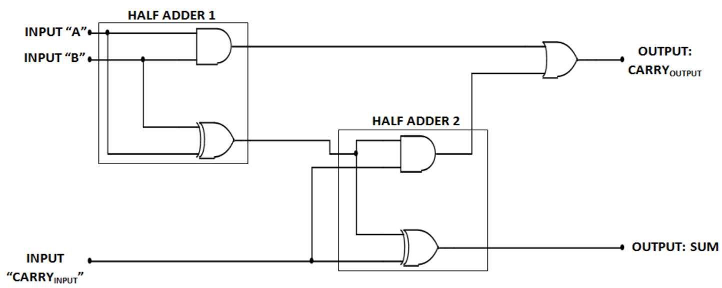

Fig.3. Full Adder Logical Circuit Diagram

Table.1. Full Adder Truth Table

INPUTS			OUTPUTS	
A	B	$CARRY_{INPUT}$	SUM	$CARRY_{OUTPUT}$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0

0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Implementing a full adder on circuit board we would require IC 7408 for AND Gate, IC 7486 for EX - OR Gate and IC 7432 for OR Gate.

Using these ICs we are able to design a full adder on board and verify its logic i.e. verifying its truth table.

The same results are easily obtained digitally with the help of writing a Verilog HDL code for full Adder. Here full adder is obtained by using two half adders h1 and h2 respectively.

Verilog HDL Description:

Module Program:

module halfadd (s, c, a, b);
input a,b;
output s,c;
assign s=a^b;
assign c=a&b;
endmodule
module fulladd (sum, carry, c, a, b);
input a, b, c;
output sum, carry;
wire w1,w2,w3;
halfadd h1(w1,w2,a,b);
halfadd h2(sum,w3,c,w1);
or (carry,w2,w3);
endmodule

```
module halfadd (s, c, a, b);
input a,b;
output s,c;
assign s=a^b;
assign c=a&b;
endmodule
module fulladd (sum, carry, c, a, b);
input a, b, c;
output sum, carry;
wire w1,w2,w3;
halfadd h1(w1,w2,a,b);
halfadd h2(sum,w3,c,w1);
or (carry,w2,w3);
endmodule
```

Fig.4.1. Full Adder module program written in Verilog HDL using Xilinx 14.7

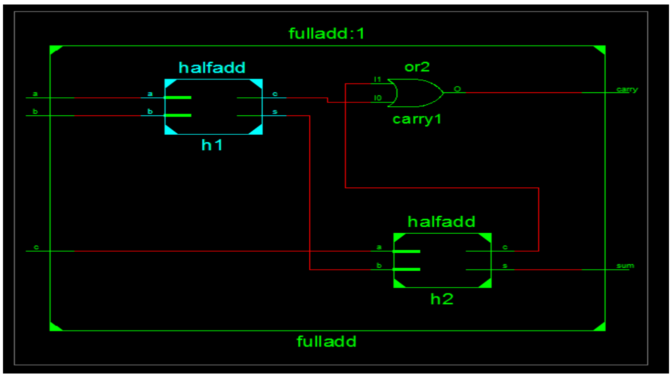

Fig.4.2. Full Adder Logical Circuit Diagram obtained after executing the module program

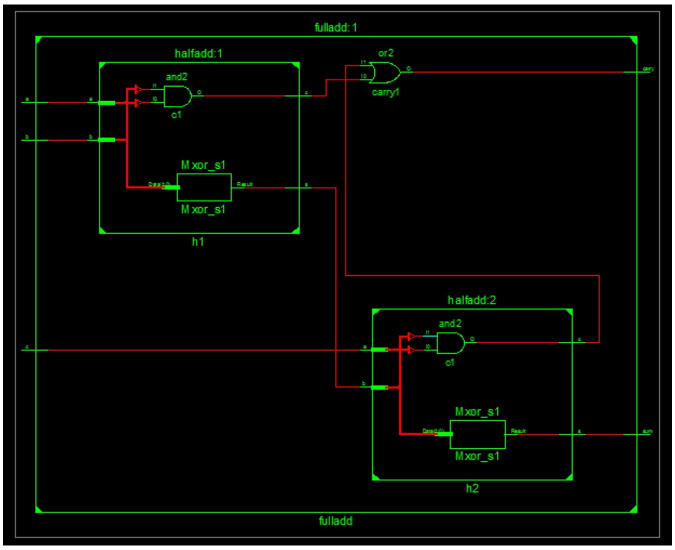

Fig.4.3. Full Adder Logical Circuit Diagram showing inner half adders gate interconnections obtained after executing the module program

Test Bench Program:

module fulladdtest;
reg a,b,c;
wire sum, carry;
fulladd uut (sum,carry,a,b,c);
initial
begin
$monitor ($time,"a=%b,b=%b,c=%b,sum=%b,carry=%b",a,b,c,sum,carry);
#100 a=0;b=0;c=0;
#100 a=0;b=0;c=1;
#100 a=0;b=1;c=0;
#100 a=0;b=1;c=1;
#100 a=1;b=0;c=0;
#100 a=1;b=0;c=1;
#100 a=1;b=1;c=0;
#100 a=1;b=1;c=1;
end
endmodule

```
module fulladdtest;
reg a,b,c;
wire sum, carry;
fulladd uut (sum,carry,a,b,c);
initial
begin
$monitor ($time,"a=%b,b=%b,c=%b,sum=%b,carry=%b",a,b,c,sum,carry);
#100 a=0;b=0;c=0;
#100 a=0;b=0;c=1;
#100 a=0;b=1;c=0;
#100 a=0;b=1;c=1;
#100 a=1;b=0;c=0;
#100 a=1;b=0;c=1;
#100 a=1;b=1;c=0;
#100 a=1;b=1;c=1;
end
endmodule
```

Fig.4.4. Full Adder test bench program written in Verilog HDL using Xilinx 14.7

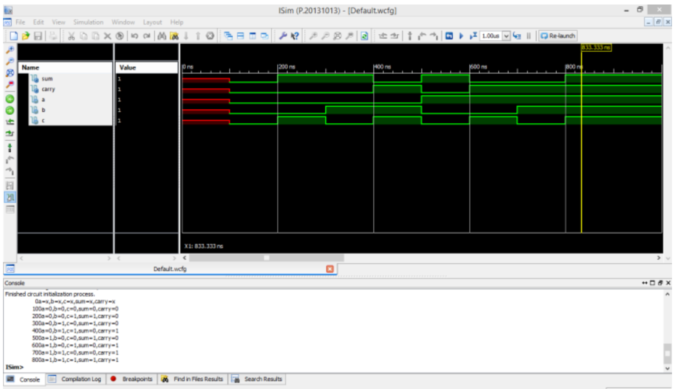

Fig.4.5. Timing diagram obtained after writing the test bench showing the logical verification of the full adder

6. FUTURE SCOPE

Engineers and Engineering students can easily be able design their own circuits and implement. It will become very easier to showcase their engineering work as per the global sections of electronics and communication engineering

7. CONCLUSION

The importance and use of analog, digital and their combined effort is understood.

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BIOGRAPHY

Mr. Noor Ul Abedin is working as an Assistant Professor in Dept. of Electronics and Communication, Deccan College of Engineering and Technology. He's field of interest are Analog and Digital Electronics. He has lectured and thought various engineering subjects which include Anlaog Electronic Devices & Circuits, VLSI Design, Networks & Circuits, Antennas & Wave Propagation, Electronic Instrumentation, Automation in Process Control, Power Electronics, Digital Electronics & Logic Design and Linear Integrated Circuits.