A Review of Reconfigurable Architecture for QAM Modulators

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ABSTRACT- Analog and digital communication both uses QAM. QAM (Quadrature Amplitude Modulation) is widely used modulation technique in the wireless communication system. As it supports the high data rate transmission and it with efficiency uses the ability and bandwidth resources. QAM is employed in several application like color TV, Wi-Max, OFDM (Orthogonal Frequency Division Multiplexing), and in digital satellite communication system. It provides the phase as well as amplitude change so that number of sub channel can be used. FPGA provides a good platform for implementations of many types of algorithms. FPGA provides Partial Reconfiguration (PR) feature, using which we can change the functionality of the FPGA so that modulation can change as per the channel condition. Due to that data rate can be adjusted and restrict to data loss This paper presents the implementation of different QAM variants in MATLAB system generator and implement it on FPGA and using Partial Reconfiguration change the modulation scheme.

Keywords: QAM, FPGA, MATLAB, PR, DATA RATE

I. INTRODUCTION

Joseph Mitola first presented the concept of SDR as a way of implementing programmable and reconfigurable radio transceivers. The main goal of SDR is to replace as many as possible analog and/or digital components in a radio system with programmable devices. It has played a huge role in guiding the development of communication systems. Digital signal processing is a key technology for the software-defined radio hardware platform as a result of which modulation and demodulation techniques have become the core of SDR technology research.

SDR has generic hardware platform through that it implement modulation and reception functions. These devices embrace field programmable gate array (FPGA), digital signal processors (DSP), general purpose processor (GPP), an application specific integrated circuit (ASIC). FPGA is economical, flexible, consumes less power as compared to DSP and is that the most viable answer to implement SDR modules. It conjointly supports altruist feature partial reconfiguration. FPGA is gaining quality for its variable applications in areas of defense, automotive, broadcasting, wireless communication etc.

SDR in the communication field and PR in VLSI domain are the recent trends, that provides nice opportunities for analysis and academic communities in enhancing and making a lot of economical ways that to leverage the utilization of FPGA to implement SDR modules. The paper offers data concerning a way to implement the foremost block of radio modulation schemes on FPGA using PR.

II. METHODOLOGY

Digital communication is widely used these days. The development of digital communications needs not a solely high performance of hardware systems however additionally flexibility in style and implementation. FPGA give flexibility for implementing completely different communication techniques. Additionally, space and power optimization may be done by using HDL (Hardware Description Language). The system-level style that has been developed recently, like System Generator, makes design tasks a lot of easier than it's ever been before. Designers will simply check algorithms, perform the whole system or modify and update diagram shortly. For this reason, system level style is taking part in a considerable role in implementing and optimization.

Commercial offered SDR system platforms are reprogrammed by code routines that run on collection hardware platforms like general Processors (GPPs) or Digital Signal Processors (DSPs). Obviously, GPPs and DSPs don't seem to be suitable reconfigurable hardware platforms for the high rate and low power constraints needed by the baseband signal processing for contemporary SDR System. FPGA will support high data rates and high information measure for current and next generations of wireless communication standards with a discount in power consumption and affordable hardware resources utilization.[2]

III. QAM (Quadrature Amplitude Modulation)

Modulation can be defined is a process in which a property of carrier signal is varied in proportionally to the information signal, whereas Digital modulation is a process by which digital symbols are transmitted into waveforms. There are various digital modulation/demodulation techniques in the communication system such as ASK, FSK, PSK, QAM etc. BUT, Quadrature amplitude modulation gives higher data rate transmission as compared to the BPSK and QPSK modulation technique. QAM is combinations of both ASK and PSK modulation technique due to that more number of subchannel can be used to transmit over a single channel. Field programmable gate array made from the semiconductor material that contains programmable logic elements (LEs) and reconfigurable interconnects to build any combinational or sequential logic functions. Hardware implemented in an FPGA can be reconfigured by programming the logic elements and interconnections for particular applications

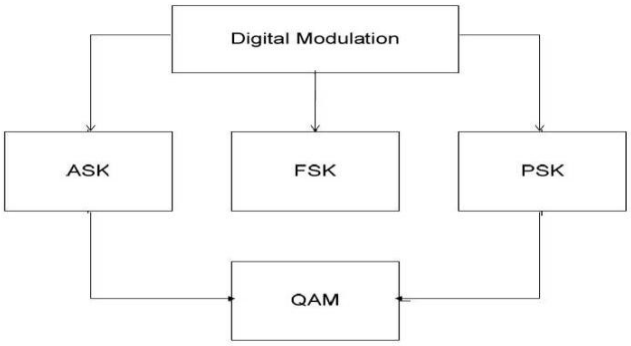

Fig. 1: Construction of QAM

Figure 1 shows, QAM is combinations of both ASK and PSK modulation scheme. In this, two message signals are applied to the separate product modulator with same carrier frequency with 90-degree phase shift. The signal S(t) consists of the sum of these two product modulator outputs as shown by,

$S(t) = A_c M_1(t) \cos(2\pi f_c t) + A_c M_2(t) \sin(2\pi f_c t)$ --(1)

4-LEVEL QAM AND 8-LEVEL QAM

For 4-QAM ($M = 2^2 = 4$ signal states) and 8-QAM ($M = 2^3 = 8$ signal states), the quantity of amplitude shifts is fewer than the quantity of phase shifts. As a result of amplitude changes are prone to noise and need bigger 'shift differences' than do phase changes, the quantity of section shifts employed by a QAM system is often larger than the quantity of amplitude shift.

Signal-space Constellation Diagrams for 4-QAM and 8-QAM:

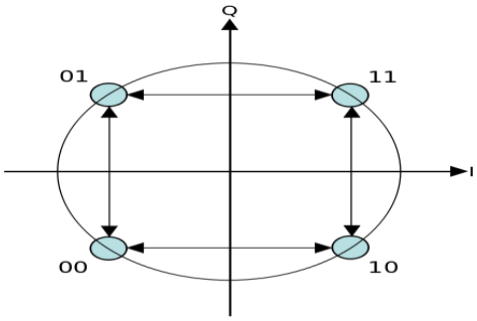

Fig. 2: 4 QAM

1 amplitude, 4 phases

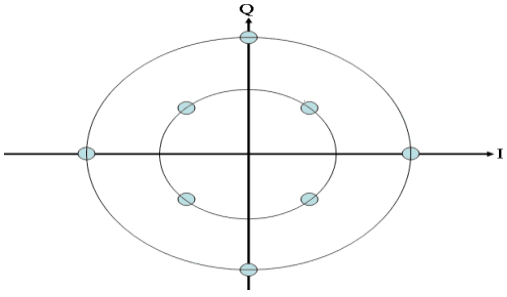

Fig. 3: 8 QAM

2 amplitude, 4 phases

III. FPGA ARCHITECTURE AND RECONFIGURATION

This section shortly justifies the essential structure of FPGA and will illustrate a selected feature that's obtainable with recent FPGA devices referred to as Partial Reconfiguration. The work is based on the use of the device and this feature.

A. FPGA design

FPGAs area unit pre-fabricated Si devices which will be electrically programmed to become virtually any reasonably digital circuit or system. FPGA carries with it Associate in Nursing array of programmable logic blocks of probably differing types, as well as general logic, memory, and multiplier factor blocks encircled by a programmable routing cloth that enables blocks to be programmable interconnected. The array is encircled by programmable input/output blocks that connect the chip to the outside world.

B. Partial Reconfiguration

FPGA technology can be suitable for on-site programming; also can be re-programmed at any number of times. The Partial Reconfiguration (PR) is the new feature available in the recent FPGA systems which modifies a subset of logic in a regular FPGA design6. The main idea is to reconfigure specific parts (or modules) of a system while the remaining part of the system remains as such and is still running. The portions of the system that are to be reconfigured are called reconfigurable modules and the parts that do not change are called static modules.

Partial reconfiguration can be done in two ways, i.e., modular based PR and difference based PR. In modular based PR, bit files for each module are loaded for during reconfiguration. However, a single partial bitstream is loaded indifference based PR which contains information about the difference between the current system and the new system. Difference based partial reconfiguration is particularly very useful when small changes have to be made to the design. Modular based design is implemented in this design.

IV. SYSTEM IMPLEMENTATION

The design flow for system implementation consists of 2 parts. Part A consists of simulation of 4 level QAM and 8 level QAM electronic equipment using MATLAB and implementation of an equivalent using System Generator Tool on FPGA while not partial reconfiguration

The system generator tool provides VHDL code, Simulink based model that successively will be synthesized, simulated and placed and routed into FPGA. Half B of style flow consists of an implementation of 4 level QAM and 8 level QAM on FPGA using partial reconfiguration.

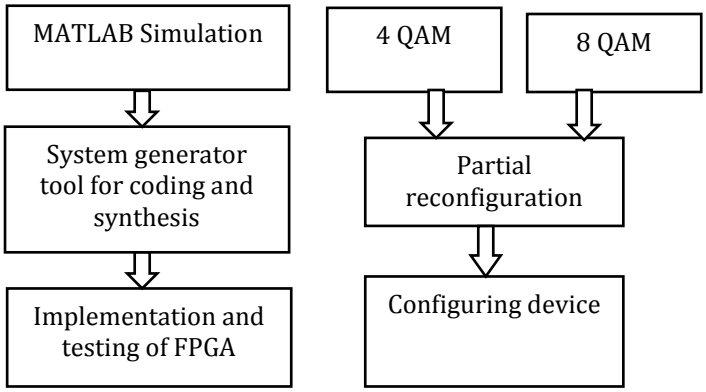

Fig. 4. Design Flow for System Implementation

V. CONCLUSION and FUTURE SCOPE

FPGA platform enumerates the convenience of implementation and provides flexibility in implementing the design with a modification in the design parameters. Conjointly it provides an occasional price, low power resolution. Further work would involve the design of M-QAM modulators on FPGA using partial reconfiguration. Use of PR feature additionally makes system straightforward and fast to adapt to the modification in the atmosphere or as per would like.

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