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A Novel Topology for a Single Phase HyperLevel Inverter using a Single DC Power Source

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Abstract - *This paper proposes a new design of a Single DC Source Multilevel inverter (SDCMI) topology as a hyperlevel inverter to reduce the total harmonic distortion of the output voltage and current. This new design converts two buck converters (BC) into a hyperlevel inverter to create n number of levels, the number of these levels can be changed without the need to change the topology structure, because the number of levels is controlled by the SPWM switching frequency. This novel topology of the proposed hyperlevel inverter in this paper was designed to produce 1000 level 220V output voltage, 50Hz with a nominal power of 1KW. The mathematical model of the proposed topology has been demonstrated in this paper.*

Key Words: multilevel; inverter; single phase; reduced switch-count; single DC source.

1. INTRODUCTION

Multilevel inverters are becoming industry's choice because of their reduced voltage stress, capability for generating an almost-sinusoidal voltage, built-in redundancy and other benefits. The general concept of operation of a multilevel inverter (MLI) involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. One clear disadvantage of MLI is the higher number of semiconductor switches required. Furthermore, implementation of conventional MLI topologies requires the control system to be more complex. Another disadvantage of MLI is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available, and series capacitors require voltage balancing [1]. Recently, a transformer-less buck converter (BC) based H-bridge topology was implemented to obtain variable DC voltage form a single DC source [2]. The disadvantage of this topology is that it requires an additional BC unit. Another topology that converts single DC source multilevel inverter (SDCMI) into a BC and MLI was proposed. However, the main disadvantage of this topology is that it is capable of producing a small number of output voltage levels with a constant duty cycle over each level time [3]. The novel topology of the single DC hyperlevel inverter (SDCHI) proposed in this paper offers in terms of number of output voltage levels, a step-based variable duty cycle and a lower total harmonic distortion (THD) for both the voltage and current output waveforms.

In this paper, a novel topology is proposed. The proposed topology of the SDCHI exhibits better performance, when compared to similar SDCMI topologies, in terms of the number of switches, current commutation path and voltage stress on the switches. The validity of the proposed topology is verified by MATLAB®/Simulink® simulations' results. The rest of the paper is organized as follows: The architecture and principle of operation in Section 2. Comparisons of the discussed topologies are presented in Section 3, and simulation results are presented in Section 4. Finally, conclusions are drawn in Section 5.

2. Architecture and principle of operation

2.1 Architecture

The basic architecture of the proposed topology of SDCHI, shown in Fig. 1, is based on the basic forward converter, sometimes called a step-down or buck converter topology [5]. The proposed topology architecture of the SDCHI consists of a single DC power source, four unidirectional switches SW1, SW2, SW3, and SW4, two inductors L1 and L2, two capacitors C1 and C2 and two diodes D1 and D2. The proposed topology architecture is capable of generating both positive and negative polarity output voltage across the load V_o. The output voltage value is proportional to the duty cycle of the control signal of SW2 and SW4, while SW1 and SW3 control the polarity of the output voltage. SW1 and SW2, shown in Fig. 1. are responsible of generating variable positive output voltage, while SW3 and SW4 are responsible of generating variable negative output voltage.

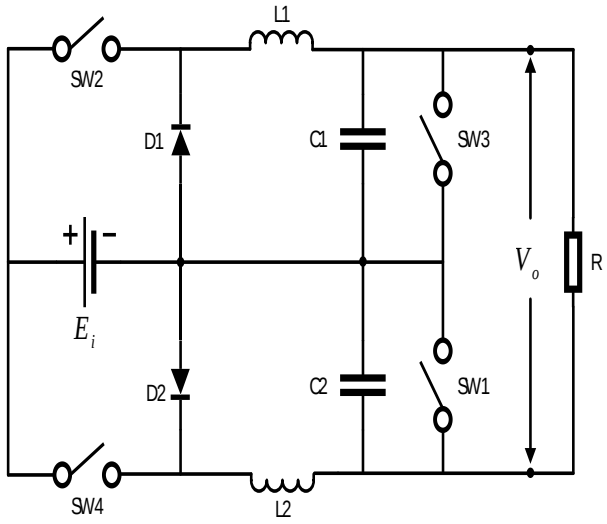


Fig -1: Structure of the proposed topology of the SDCHI

2.2 Control System Block Diagram

The switches of the SDCHI are driven by the SDCHI control system shown in Fig. 2. This simple control system consists of two main units, the pulse generator unit and the logic unit. The pulse generator unit consists of two comparators (A and B). Comparator A, compares the reference signal with zero voltage, and outputs polarity control signal that is responsible for controlling SW1 and SW3 switches. Since polarity is controlled by comparator A output, comparator B must output a PWM control signal that resembles only the positive phase of the reference signal. Hence, comparator B is a modified typical PWM generator [4] that compares the reference signal that has a certain frequency with a higher frequency saw tooth signal, and outputs the PWM control signal that is responsible for controlling SW2 and SW4 switches. The longer the switch is on, compared to the off periods, the higher the total power supplied to the load.

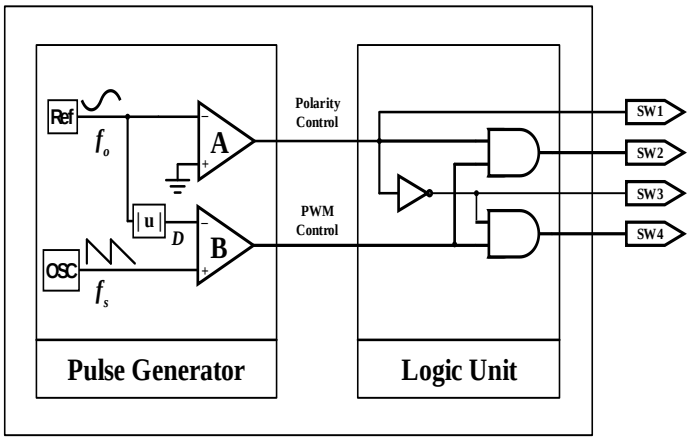


Fig -2: SDCHI control system block diagram

2.3 Operation Principle

High Side and Low Side Principle of Operation

For analysis purposes, it is assumed that components are lossless and the output voltage V_o is maintained constant because of the large magnitude of the capacitors C1 and C2 across the output. The input voltage E_i is also assumed constant, such that $E_i \geq V_o$. If all the stored energy in the inductor is transferred to the capacitor and the load before the switch is turned back on, operation is termed discontinuous inductor current, since the inductor current has reached zero. If the switch is turned on before the current in the inductor reaches zero, that is, if continuous current flows in the inductor, operation is termed continuous. In this paper, the proposed topology is assumed to operate in continuous inductor current.

The proposed topology of the SDCHI operates in a (high side, low side) switching principle. Thus, the architecture can be divided into two parts; the high side part and the low side one. Each of these sides operates in two states, resulting in four overall different states of operation for the proposed topology. These states are shown in Table 1.

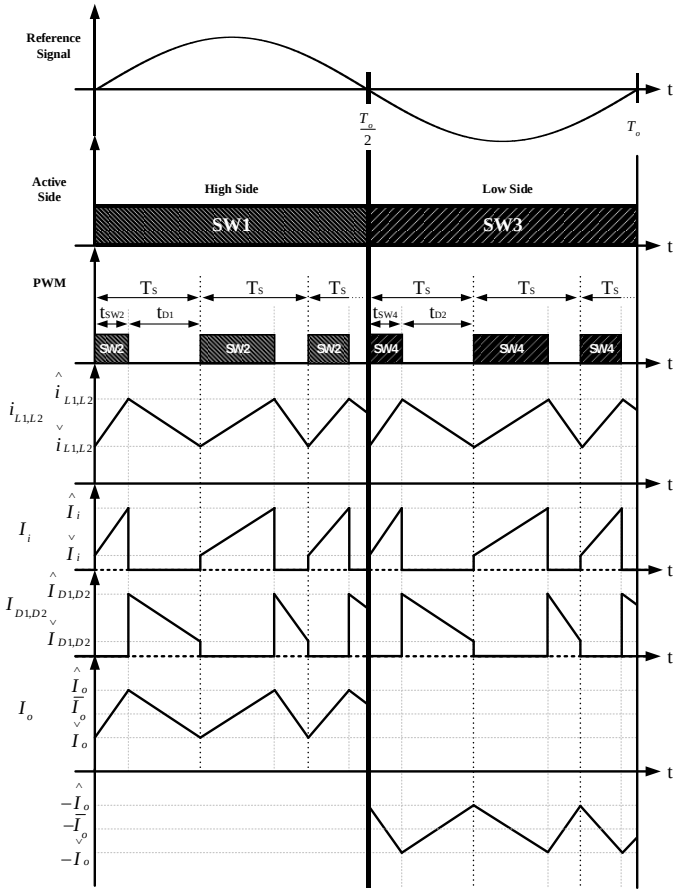
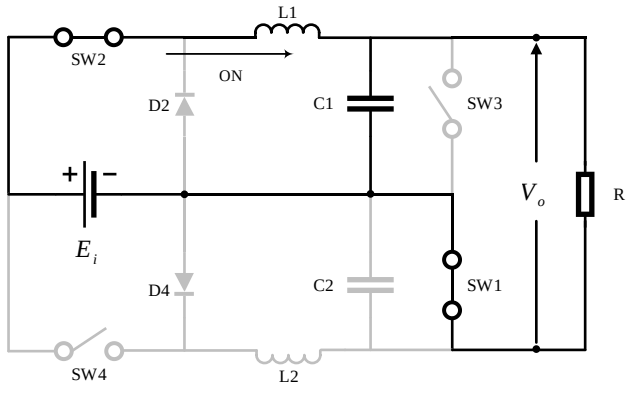


Fig-3: Waveforms of reference signal, PWM switching signals, inductors currents, input current, diodes currents and output current.

Table -1: Switching states for the proposed topology

Side	States	SW1	SW2	SW3	SW4	V_o
High Side	1	1	1	0	0	$E_i \times D$
	2	1	0	0	0	$-E_i \times (1-D)$
Low Side	3	0	0	1	1	$-(E_i \times D)$
	4	0	0	1	0	$E_i \times (1-D)$



(a)

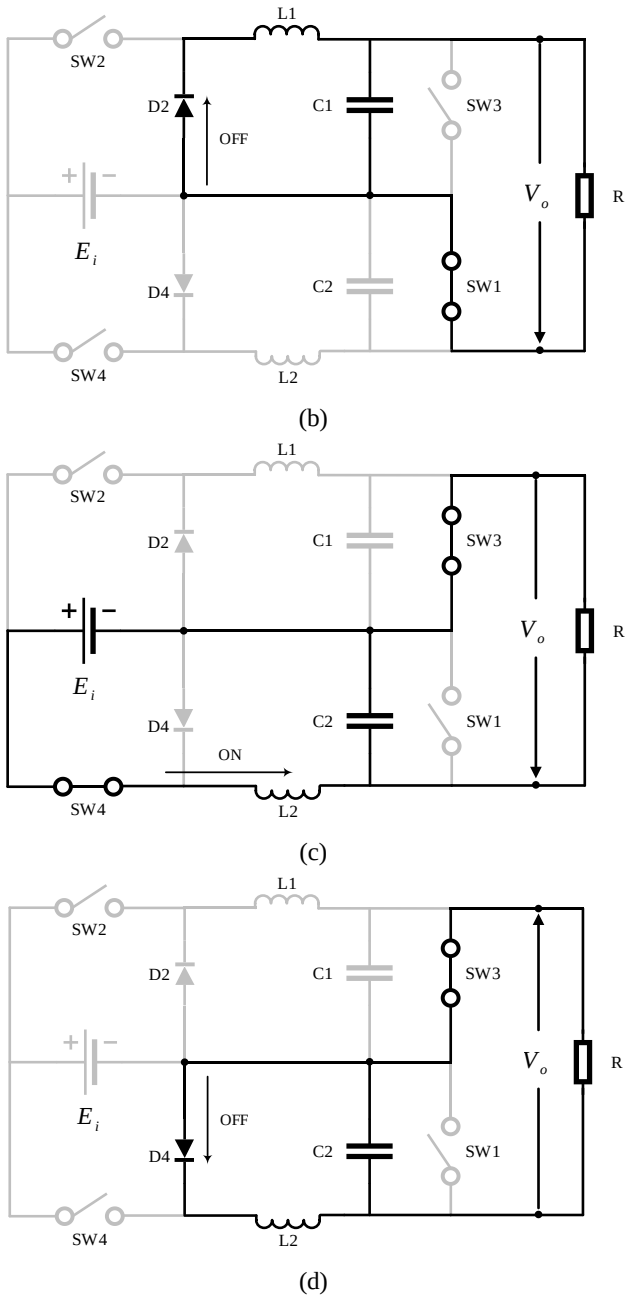


Fig -4: Schematics of switching states (see Table 1).

High side part:

The transistor SW1 is on and the input voltage E_i is chopped by transistor SW2. When SW2 is on (state 1 shown in Fig. 4.a), because the input voltage E_i is greater than the load voltage V_o, energy is transferred from the DC power source to $L1$, C1, and the load. When SW2 is turned off (state 2 shown in Fig. 4.b), stored energy in $L1$ is transferred via diode D1 to C1 and the load. The high side part shown in Fig. 3. illustrate SDCHI circuit current and switches signal waveforms for period $[0, T_o/2]$, where T_o is the period of the reference signal. The inductor $L1$ current is analyzed first when the switch SW2 is on, then when the switch SW2 is off. When transistor SW2 is turned on for period t_{SW2}, the difference between the supply voltage E_i and the output voltage V_o is impressed across $L1$.

From $V = L1di/dt = L1\Delta i/\Delta t$, the linear current change through the inductor will be

$$\Delta i_{L1} = \hat{i}_{L1} - \check{i}_{L1} = \frac{E_i - V_o}{L1} \times t_{SW2} \quad (1)$$

When SW2 is switched off for the remainder of the switching period, $t_{D1} = (T_S - t_{SW2})$, the freewheel diode D1 conducts and $-V_o$ is impressed across $L1$. Thus, using $V = L1\Delta i/\Delta t$, rearranged

$$\Delta i_{L1} = \frac{V_o}{L1} \times (T_S - t_{SW2}) \quad (2)$$

Equating equations (1) and (2) gives

$$(E_i - V_o)\, t_{SW2} = V_o (T_S - t_{SW2}) \quad (3)$$

This expression shows that the inductor $L1$ average voltage is zero, and after rearranging ($P_o = P_i$)

$$\frac{V_o}{E_i} = \frac{\bar{I}_i}{\bar{I}_o} = \frac{t_{SW2}}{T_S} = D \quad (4)$$

This equation also shows that for a given input voltage, the output voltage is determined by the transistor conduction duty cycle D and the output is always less than the input voltage. This confirms and validates the original analysis assumption that $E_i \geq V_o$. The voltage transfer function is independent of the load, circuit inductance $L1$ and capacitance C1. The inductor rms ripple current (and capacitor ripple current in this case) from equations (1) and (2), for continuous inductor current, is given by

$$i_{L1r} = \frac{\Delta i_{L1}}{2\sqrt{3}} = \frac{1}{2\sqrt{3}} \frac{V_o}{L1} (1 - D) T_S = \frac{1}{2\sqrt{3}} \frac{E_i}{L1} (1 - D) D T_S \quad (5)$$

while the inductor total rms current is

$$i_{L1rms} = \sqrt{\bar{I}_{L1}^2 + i_{L1r}^2} = \sqrt{\bar{I}_{L1}^2 + \left(\frac{\frac{1}{2}\Delta i_{L1}}{\sqrt{3}} \right)^2} = \sqrt{\frac{1}{3}\left(\hat{i}_{L1}^2 + \left(\hat{i}_{L1} \times \check{i}_{L1} \right) + \check{i}_{L1}^2 \right)} \quad (6)$$

The switch and diode average and rms currents are given by

$$\bar{I}_{SW2} = \bar{I}_i = D\bar{I}_O \quad (7)$$

$$I_{SW2\,rms} = \sqrt{D} i_{L1\,rms} \quad (8)$$

$$\bar{I}_{D1} = \bar{I}_o - \bar{I}_i = (1 - D)\bar{I}_o \quad (9)$$

$$I_{D1\,rms} = \sqrt{1 - D} i_{L1\,rms} \quad (10)$$

If the average inductor current, hence output current, is $\bar{I}_{L1}$, then the maximum and minimum inductor current levels are given by

$$\hat{i}_{L1} = \bar{I}_{L1} + \frac{1}{2}\Delta i_{L1} = \bar{I}_o + \frac{1}{2}\frac{V_o}{L1}(1-D)\,T_S = V_o\left[\frac{1}{R} + \frac{1-D}{2\,f\,L1}\right] \quad (11)$$

and

$$\check{i}_{L1} = \bar{I}_{L1} - \frac{1}{2}\Delta i_{L1} = \bar{I}_o - \frac{1}{2}\frac{V_o}{L1}(1-D)\,T_S = V_o\left[\frac{1}{R} - \frac{1-D}{2\,f\,L1}\right] \quad (12)$$

respectively, where Δi_{L1} is given by equation (1) or (2). The average output current is $\bar{I}_{L1} = \frac{1}{2}\left(\hat{i}_{L1} + \check{i}_{L1}\right) = \bar{I}_o = V_o/R$. The output power is therefore V_o^2/R which equals the input power, namely $E_i\bar{I}_i = E_i\bar{I}_{SW2}$. Circuit waveforms for continuous inductor current conduction are shown in Fig. 3.

Low Side part:

The transistor SW3 is on and the input voltage E_i is chopped by transistor SW4. When SW4 is on (state 3 shown in Fig. 4.c), because the input voltage E_i is greater than the load voltage V_o (the output voltage value during low side part operation is negative due to reverse polarity), energy is transferred from the DC power source to $L2$, C2, and the load. When SW4 is turned off (state 4 shown in Fig. 4.d), stored energy in $L2$ is transferred via diode D2 to C2 and the load. The high side part shown in Fig. 3. Illustrate SDCHI circuit current and switches signal waveforms for period $[T_o/2, T_o]$.

The inductor $L2$ current is analyzed first when the switch SW4 is on, then when the switch SW4 is off. When transistor SW4 is turned on for period t_{SW4}, the difference between the supply voltage E_i and the output voltage V_o is impressed across $L2$. From $V = L2\,di/dt = L2\,\Delta i/\Delta t$, the linear current change through the inductor will be

$$\Delta i_{L2} = \hat{i}_{L2} - \check{i}_{L2} = \frac{E_i - V_o}{L2} \times t_{SW4} \quad (13)$$

When SW4 is switched off for the remainder of the switching period, $t_{D2} = (T_S - t_{SW4})$, the freewheel diode D2 conducts and $-V_o$ is impressed across $L2$. Thus, using $V = L2\,\Delta i/\Delta t$, rearranged

$$\Delta i_{L2} = \frac{V_o}{L2} \times (T_S - t_{SW4}) \quad (14)$$

Equating equations (13) and (14) gives

$$(E_i - V_o)\,t_{SW4} = V_o\,(T_S - t_{SW4}) \quad (15)$$

This expression shows that the inductor $L2$ average voltage is zero, and after rearranging ($P_o = P_i$)

$$\frac{-V_o}{E_i} = \frac{\bar{I}_i}{-\bar{I}_o} = \frac{t_{SW4}}{T_S} = D \quad (16)$$

This equation also shows that for a given input voltage, the output voltage is determined by the transistor conduction duty cycle D and the output is always less than the input voltage. This confirms and validates the original analysis assumption that $E_i \geq V_o$. The voltage transfer function is independent of the load, circuit inductance $L2$ and capacitance C2. The inductor rms ripple current (and capacitor ripple current in this case) from equations (13) and (14), for continuous inductor current, is given by

$$i_{L2r} = \frac{\Delta i_{L2}}{2\sqrt{3}} = \frac{1}{2\sqrt{3}}\frac{-V_o}{L2}(1-D)\,T_S = \frac{1}{2\sqrt{3}}\frac{E_i}{L2}(1-D)\,DT_S \quad (17)$$

while the inductor total rms current is

$$i_{L2rms} = \sqrt{\bar{I}_{L2}^2 + i_{L2r}^2} = \sqrt{\bar{I}_{L2}^2 + \left(\frac{\frac{1}{2}\Delta i_{L2}}{\sqrt{3}}\right)^2} = \sqrt{\frac{1}{3}\left(\hat{i}_{L2}^2 + \left(\hat{i}_{L2} \times \check{i}_{L2}\right) + \check{i}_{L2}^2\right)} \quad (18)$$

The switch and diode average and rms currents are given by

$$\bar{I}_{SW4} = \bar{I}_i = D\left(-\bar{I}_O\right) \quad (19)$$

$$I_{SW4\,rms} = \sqrt{D}\,i_{L2\,rms} \quad (20)$$

$$\bar{I}_{D2} = -\bar{I}_o - \bar{I}_i = (1-D)\left(-\bar{I}_o\right) \quad (21)$$

$$I_{D2\,rms} = \sqrt{1-D}\,i_{L2\,rms} \quad (22)$$

If the average inductor current, hence output current, is $\bar{I}_{L2}$, then the maximum and minimum inductor current levels are given by

$$\hat{i}_{L2} = \bar{I}_{L2} + \frac{1}{2}\Delta i_{L2} = -\bar{I}_o + \frac{1}{2}\frac{-V_o}{L2}(1-D)\,T_S = -V_o\left[\frac{1}{R} + \frac{1-D}{2\,f\,L2}\right] \quad (23)$$

and

$$\check{i}_{L2} = \bar{I}_{L2} - \frac{1}{2}\Delta i_{L2} = -\bar{I}_o - \frac{1}{2}\frac{-V_o}{L2}(1-D)\,T_S = -V_o\left[\frac{1}{R} - \frac{1-D}{2\,f\,L2}\right] \quad (24)$$

respectively, where Δi_{L2} is given by equation (13) or (14). The average output current is $\bar{I}_{L2} = \frac{1}{2}\left(\hat{i}_{L2} + \check{i}_{L2}\right) = -\bar{I}_o = -V_o/R$. The output power is therefore V_o^2/R which equals the input power, namely $E_i\bar{I}_i = E_i\bar{I}_{SW4}$. Circuit waveforms for continuous inductor current conduction are shown in Fig. 3.

Form the previous equations, we can determine the output voltage and current equations of the proposed topology of the SDCHI for period $[0, T_o]$

$$I_O = \begin{cases} \bar{I}_{L1} & 0 \le t \le \frac{T_o}{2} \\ -\bar{I}_{L2} & \frac{T_o}{2} \le t \le T_o \end{cases} \quad (25)$$

$$V_O = \begin{cases} E_i \times D & 0 \le t \le \frac{T_o}{2} \\ -(E_i \times D) & \frac{T_o}{2} \le t \le T_o \end{cases} \quad (26)$$

Architecture components calculation

Inductor calculation

$$L = \frac{V_o \cdot (1-D)}{f_s \cdot \Delta I_L} \quad (27)$$

Capacitor calculation

$$C_{o(\min)} = \frac{\Delta I_L}{8 \times f_s \times \Delta V_o} \quad (28)$$

3. Comparison with conventional SDCMI topologies:

In this section, the proposed topology is compared to the topologies presented in [2][3]. Table 2 shows the comparison of conventional SDCMI with the SDCHI. A comparative analysis shows that, when one H-bridge is used, h=1, the SDCHI has a higher number of output voltage levels. The THD of the output voltage of the SDCMI is below 5%. According to the IEEE-519 or IEC 555-2 standard, the THD in the output voltage should be less than five percent [6]. When only one H-bridge is used (h=1), the proposed SDCLI has the lowest output voltage THD. Therefore, the proposed topology of the SDCHI achieves the most pure sinusoidal voltage and current output waveform. Performance and circuit parameters of the SDCMI and the proposed topology of the SDCHI are shown in Table 3.

Table -2: Comparison of different parameters of the proposed SDCHI with reported SDCMI

Ref	V_{block} in volt		No. of Levels		No. of levels shown in reported study	No. of switches h =1	THD %
	Exp	V_{dc} = 12V h = 1	Exp	h = 1			
[2]	$>4V_{dc}$	> 48	n	n	3 to 255	4	<5%
[3]	$4V_{dc}$	48	n	n	13	4	<5%
SDCHI	$80V_{dc}$	960	n = $\frac{T_o}{T_s}$	n	1000	4	<5%

Table -3: Performance and circuit parameters of single phase SDCMI for THD <5

Ref	V_{block} (V_{dc} = 12V)	n	N_{others}
[2]	>48	21	One DC to DC converter
[3]	48	13	Inductor and capacitor
SDCHI	960	1000	Two inductors and two capacitors

4. Simulation Results

Fig. 5. shows the schematic of the system under study. Simulations were carried out using MATLAB/Simscape (R2017a, The MathWorks Inc., Natick, MA, USA). The semiconductor switches are MOSFETs SCT30N120 with voltage and current ratings of 1200V, 45A. Table 4 lists the specifications of the SDCHI used for simulations.

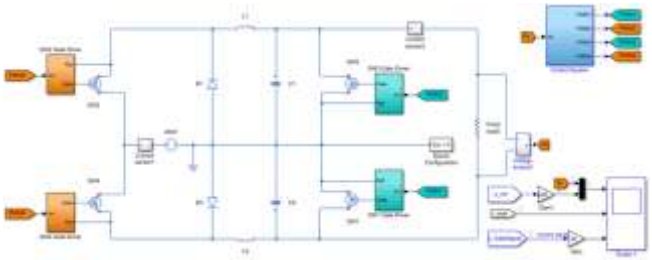


Fig-5: Simulation model of SDCHI

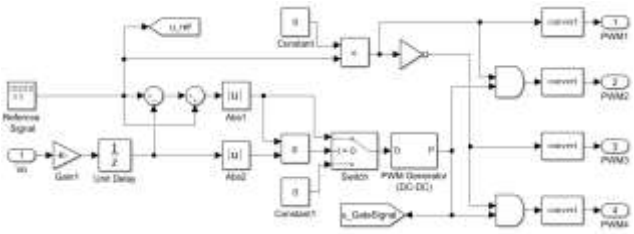


Fig-6: Simulation model of control system block

Table-4: Parameters for SDCHI simulations

Parameter	Value
Output frequency f_o	50 Hz
Switching frequency f_s	50 KHz
DC power source V_i	240 V
Inductors L_1, L_2	8.33mH
Capacitors C_1, C_2	1uF
Levels n	1000
Load R	40Ω

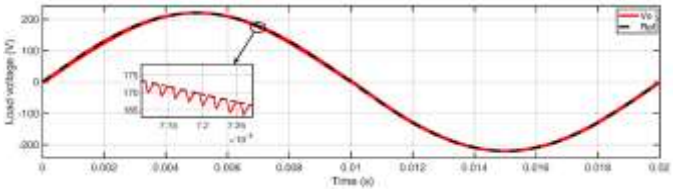


Fig. 7. Load voltage and reference signal waveforms of the SDCHI

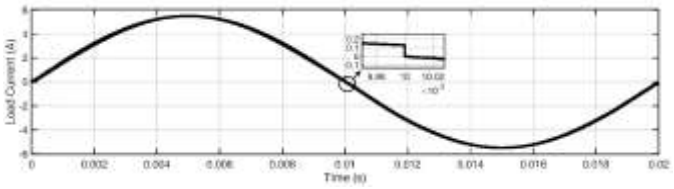


Fig. 8. Load current signal waveform

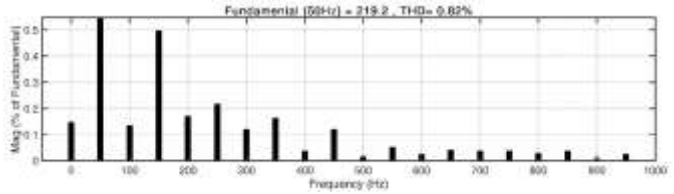


Fig-9: THD of load voltage of the SDCHI

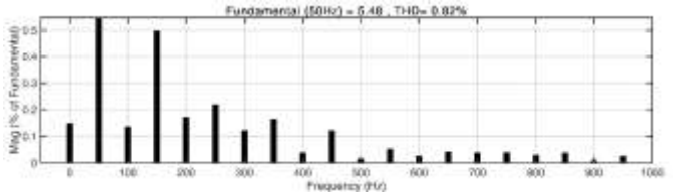


Fig-10: THD of load current of the SDCHI

5. Conclusion

In this paper, a new inverter topology has been proposed which has superior features over conventional topologies in terms of control requirements, cost and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. The new feedback control system for the proposed topology, which is based on SPWM control method has fewer complexities. The simulation results for a thousand-level inverter of the proposed topology are demonstrated in this paper. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a lower output voltage and current THD.

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