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Comparative Study of Carrier-Based Pwm Techniques for Control of Double-Star Modular Multilevel Converter Using Half Bridge Cells

V. M. Silva [1, 2], A. S. A. Luiz [1], M. M. Stopa [1]

[1] *Department of Electrical Engineering, Centro Federal de Educação Tecnológica e Minas Gerais – CEFET MG, 7675 Ave. Amazonas, Nova Gameleira, 30510-000, Belo Horizonte - MG, Brazil.*
[2] *Professor, Department of Control and Automation and Fundamental Techniques, Universidade Federal de Ouro Preto - UFOP, 122 St. Diogo de Vasconcelos, Pilar, 35400-000, Ouro Preto - MG, Brazil.*

Abstract - *The aim of this study is to compare the performance of the Half Bridge Double-Star Multilevel Converter (represented as M2C) for medium-voltage applications using different PWM techniques based on multilevel level and phase shifted carriers and a method of capacitor balancing and circulation voltage control where it is used a single closed-loop control system without the addition of an external circuit. The criterion to be analyzed in this comparison will be the DHT of the output voltage and current as well as the current waveform. It will be assessed which types of modulation techniques benefit the capacitor balancing for the proposed system and the improvements that can be made. In addition to the investigation of which is the most effective, this study will also address the influence of the armature inductances of the converter in terms of the total harmonic distortion (THD) of the output current and line voltage for each proposed technique, as well as the range of freedom of variation of the frequency modulation index (m_f) of the carriers in situations of low commutation, therefore observing until what level it is possible to offer current and voltage for the load with small distortion through simulations in the Matlab/Simulink platform*

Key Words: Multilevel, M2C, Modular, PWM, Control.

NOMENCLATURE

V_d	DC supply voltage.
I_d	DC input current.
N	Number of Submodules for arm.
C	Submodule capacitance.
V	Rated line-to-line rms voltage.
I	Rated RMS current.
I_a	Phase “a” output current.
I_{Ua}	Phase “a” upper arm current.
I_{Da}	Phase “a” lower arm current.
I_{circ}	Circulating current.
I_{circ}^*	loop current command of I_{circ}.
P	Rated active power.
S	Rated apparent power.
E_{nom}	Nominal energy stored for arm (reference value).
E_{SM}	Nominal energy stored in each submodule capacitor (reference value).
P_d	DC input power.
v_{ja}	Output voltage of a-phase chopper-cell numbered by “j”.
v_{ja}^*	Voltage command of v_{ja}.
$v_{C_{ja}}$	Voltage of the j-capacitor of a-phase.
v_a	a-Phase three-phase line-to-neutral voltage.
v_a^*	Voltage command of v_a.
v_{Aa}^*	Voltage command from the averaging control.
$v_{B_{ja}}^*$	Voltage command from the balancing control.
v_{ab}	Three-phase line-to-line voltage.
S	Static switch (IGBT).
k_{max}	Relative upper limit for the capacitor voltage ripple.
L_{bf}	Buffer inductance.
v_C	DC capacitor voltage.
v_C^*	Voltage command of v_C.
$\bar{v}_{Ca}$	a-Phase capacitors average voltage.
L_{Load}	Load inductance.
R_{Load}	Load resistance.
PF	Load power factor ($\cos(\theta)$).
H	Unit capacitance constant.
f	Rated frequency.
f_C	Carrier frequency.
f_{fund}	Fundamental frequency.
f_{eq}	Equivalent frequency.
K_1	Proportional gain of averaging control.
K_2	Integral gain of averaging control.
K_3	Proportional gain of current control.
K_4	Integral gain of current control.
K_5	Proportional gain of balancing control.

1. INTRODUCTION

Multiple voltage level converters (multilevel) have acquired a wide acceptance and a special highlight in the industrial sector due to their large applicability in medium and high voltage, along with an incredible adaptation to the most different functions by accepting multiple serial semiconductor connections, its customizable character, lower maintenance cost and reduction of semiconductor energy loss in a way that, when compared to their precursors, the two-level voltage source inverters (VSI), their intrinsic redundant realization, low filter requirements, balanced distribution of power under the semiconductors and flexibility of multiple or common single DC source makes its popularity grow continually compared to other technologies because, since several low voltage levels are used, there is the generation of low line voltage distortion, making the generated harmonics less harmful [1-3].

The multilevel converter concept was introduced by [4] in 1975 and was initially used for three-level converters because back then there were only two-level CC-CA converters. Over time, several other multilevel converters topologies have emerged, such as the Flying Capacitor Converter (FLC) [5], with stapled diode or NPC (neutral point clamped) [6]. Cascaded H-Bridge Converter [7] and the Generalized Converter [8].

It is possible to see a summary of the multilevel converter types in Fig-1 with a highlight for the M2C Half Bridge Double-Star topology (the focus of this work). It is worth mentioning that, from the displayed topologies, M2C, FLC and generalized topology have floating capacitors, which interferes directly in their control method due to the voltage fluctuations present in their capacitors, while NPC is the only topology that is not multicell.

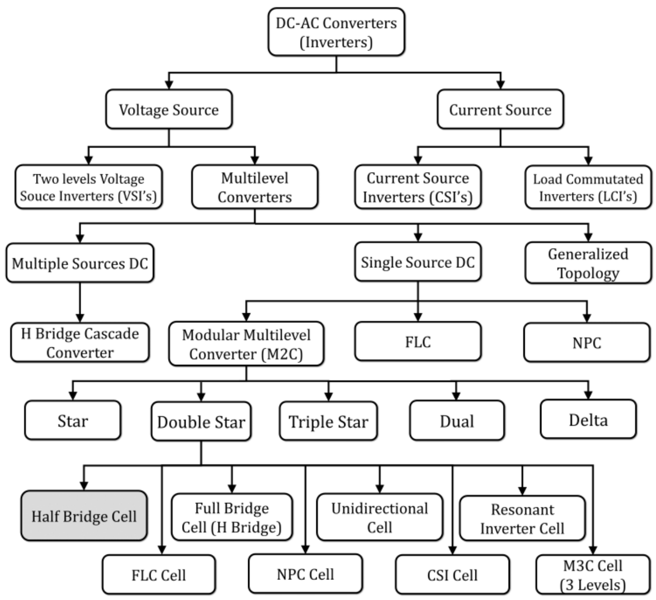


Fig-1: Types of Multilevel Converters.

Among the converter topologies used in industry, the multilevel modular topology (Fig-2) developed by Anton Lesnicar and Rainer Marquardt [3], [9-10] in 2002 has been outstanding due to its modular and configurable structure and high scalability when reaching several levels of voltage and power by the number of cells that are used in each arm, qualities that have caused its imminent popularity and acceptance.

In M2C, as the N number of cells per arm is increased, $N + 1$ voltage levels will be obtained in a way that the larger the number of cells, the greater will be the demand for the system converter's control, however, since each cell has a simple structure, manufacturing costs become small, which makes it interesting for the usage of modulation techniques that take advantage of its multicell feature. Good choices for its control are the PWM modulation techniques based on single fundamental and multiple carriers for the M2C converter, focus of this work.

M2C was initially proposed for high voltage and had half bridge cells as submodules (SM), however, due to its highly reconfigurable feature there are in the literature numerous projects that use, depending on the purpose, other types of cells in their construction. Such cells can be from full bridge SM (also very popular for having an extra protection against DC bus faults, although it costs more due to the large number of keys) to the FLC, NPC and CSI cells as summarized in the diagram of Fig-1.

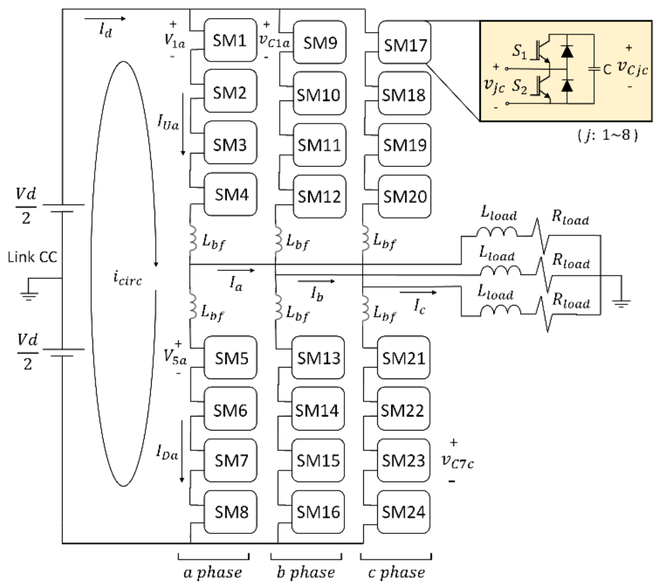


Fig-2: M2C converter with 4half bridge (chopper) cells on each arm.

In this work, it will be used the half-bridge cell in the constitution of M2C due to its greater simplicity, applicability, popularity, reduced cost and small number of semiconductor devices in its construction. The control of M2C in this work will be based on the system proposed in [11] in which it will be investigated which method of modulation presents the better performance and minimization of the total harmonic distortion (THD).

In the [12] paper it was proposed the use of a DC voltage source in place of the capacitor loop of the converter's half-bridge cell, thus featuring an ideal operating and simulation condition leading to a very useful approach to test the concepts regarding the converter balancing under absence of SM and to analyze the effectiveness of carrier-based modulation techniques. There is the disadvantage of obtaining an extremely high circulation current due to the lack of charge and discharge of the SM (since there are no capacitors), although this can be solved by inserting resistors into the converter arms which would, in turn, increase the dissipation power in the system.

Due to M2C's broad potential and immense applicability, big companies such as ABB, SIEMENS, Schneider-Electric, WEG and [13-23] strongly returned their production sectors to this technology, triggering a fierce dispute over the production of this new generation's most robust and efficient converter in order to rule the market with this converter which has become popular in the industry, naval sector [24-25], aeronautic [26], railway sector [27], high voltage direct current (HVDC) [28-34], traction [35], static synchronous compensators (STATCOM's) [36-41], flexible AC transmission systems, FACTS) [42-45], wind turbines [46], high power [47-51] and medium power [52-55], energy conditioning [56-57], maritime power generation [58-60], photovoltaic systems [61-62], electric vehicles [63], micro-networks, among many others, which shows it has a high probability of becoming the most used converter in the world.

2. MODULAR MULTILEVEL CONVERTER (M2C)

2.1 Main Features

The M2C converter can be analyzed in Fig-2, and its main advantages over the other traditional thyristor-based converters are:

- Less stress on the inverter components and the network to be interconnected.
- Scalability at different power and voltage levels.
- Redundancy feature, therefore increasing reliability.
- Small chance of being completely destroyed and easy maintenance
- Lower switching losses and lower THD.
- Extremely high applicability.
- Possibility of network connection with or without transformer.
- It operates in a low switching frequency, although high equivalent frequency ($f_{eq} = f_c * 2N$). [64]
- It has basic components of analog electronics.
- Gradual change in output voltage minimizing electromagnetic interference.
- Simple and modular mechanical constitution.
- It can achieve high output voltage with low voltage levels in its semiconductors.
- Beyond limiting the circulating current, the inductance in the arms is useful for the filtering.
- Reduction or even extinction of the DC bus capacitance due to the fact the energy is stored in the SM of the converter.

Its disadvantages are:

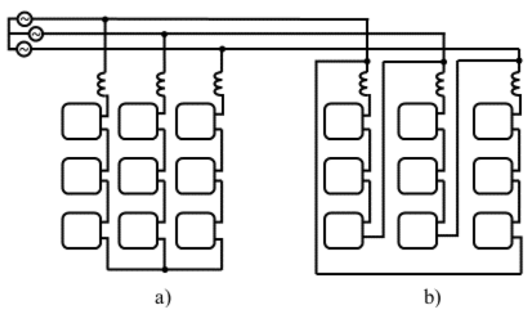
- It requires more components.
- CC bus fault vulnerability.
- Requires monitoring for all capacitors (voltage balancing) and converter armature currents [64].
- It has a more complex sizing than other converters.
- For applications with high currents, the voltage drop of the protection inductors can cause reactive power losses.
- Control complexity directly proportional to the number of cells it has.

2.2 Family of M2C Converter

The multilevel modular converters types are:

1) Single-Star Bridge-Cells (SSBC) (Fig-3 (a)).
2) Single-Delta Bridge-Cells (SDBC) (Fig-3 (b)).
3) Double-Star x-Cells (DSxC), considering "x" anyone of Fig-1 cells.
   a) DSxC with non-coupled buffer inductors (Fig-3 (d)).
   b) DSxC with coupled buffer inductors [11].
4) Dual Double-Star Bridge-Cells (DDSBC) (Fig-3 (c)).
5) Triple Star Bridge-Cells (TSBC) (Fig-3 (e)).

The M2C Double Star topology can support multiple cell, or SM, types while, until now, SSBC and TSBC the topology use only the full bridge or H Bridge cell (in this study mentioned as "bridge") as SM. The most famous cells used in the M2C converter can be seen in Fig-1 along with the innovative three-level cell (known as MMC3), widely used in offshore wind farms [60]. An in-depth approach to the family of multilevel modular converters as well as their respective applications can be seen in more detail in [65].



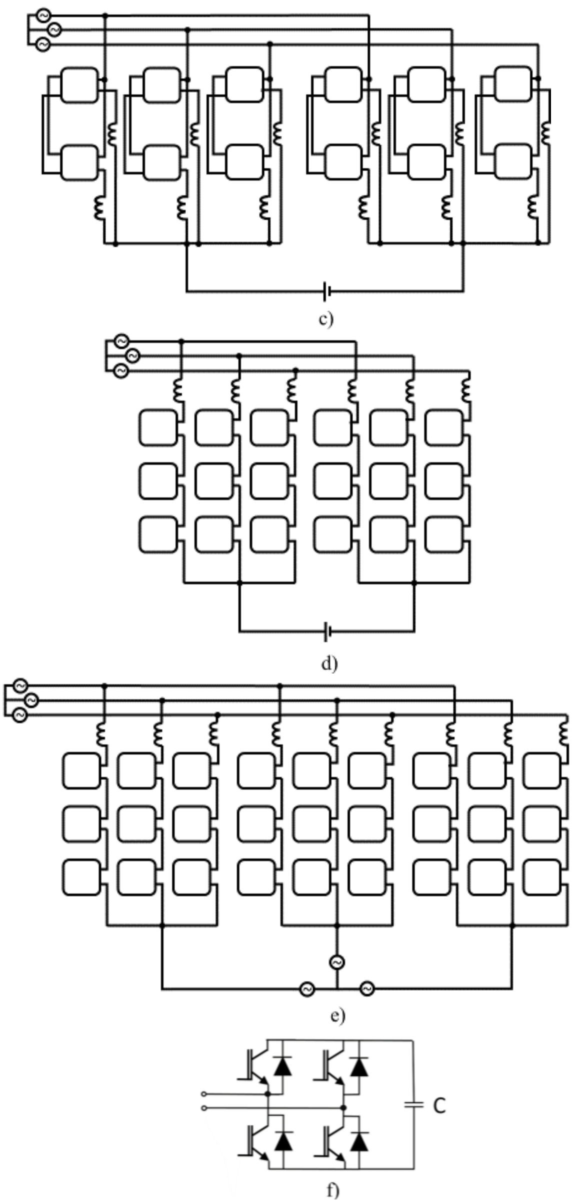


Fig-3: Modular multilevel converter family with their possible three-phase configurations using H bridge cells as SM. (a) SSBC. (b) SDBC. (c) DDSxC. (d) DSxC. (e) TSBC. (f) Bridge cell.

The best multilevel modular converters topology will depend strictly on the application being used. As previously mentioned, this class of inverters is usually used to control motors and grid connections, and such group is divided into star and delta connections [65-66].

The SSBC topology (Fig-3(a)) has the most basic configuration and control, and it can be applied to STATCOMs and battery storage systems. Analyzing the double-star bridge cells (DSBC or M2C) topology, it can be seen that it is made of two SSBC and it can work with projects requiring AC-to-DC or AC-to-AC bidirectional power conversion with the applications displayed in the introduction of this article. However, it is important to notice that both the single-star topology and the delta topology (Fig-3 (b)) do not have a DC link, which makes it impossible to obtain the M2C AC-to-DC or AC-to-AC function, rather, star and delta topologies are not good candidates for industrial motor control [11], [66].

The TSBC topology (Fig-3 (e)), known as the modular matrix converter, can be considered as the combination of three SSBC circuits with application systems oriented to AC-to-AC with bidirectional power conversion flow. It is widely used in regenerative braking and control of high power and medium voltage motors [66].

Unlike SDBC, the SSBC topology cannot release or absorb negative sequence power from the network because it does not have circulating current, reasons for its previously mentioned restricted application [65].

An interesting point is that in [11] it was used, for a certain 1ϕ project, the M2C (or DSCC 1φ, single-phase double-star chopper cell) and the DDSBSC topology also using chopper cells and it obtained the same results so that is was observed that both topologies were similar in control and configuration, with a single difference that the dual double star topology had multiple current loops which required a simple division into the circulating current control algorithm.

Another important factor is the option of using protection inductors in the M2C (coupled or decoupled), because these do not only increase the voltage difference between the various cells of the arms, but also collaborate to control the circulation current. The use of coupled inductors is interesting because they make the circuit lighter and decrease the amount of harmonic components in many applications with motors, besides the fact it is connected directly to the motor terminal, although the use of decoupled inductors is simpler and practical [65].

When dealing with the choice regarding the cell for a certain project, one must be always be attentive to the application that uses the minimum of active and non-linear devices in its structure, such as transistors, thyristors and diodes since they generate harmonic content in the electric network and when it comes to this the half bridge cell stands out because it presents simple constitution and low harmonic content although it does not have security against current surges, faults in the DC bus and in the SM. However, important studies were developed to avoid such damages by inserting redundant SM [67-68], balancing the system in situations of cell failure [69-70] or modifying them to support faults in the DC bus [71-84] or SM [85-94], but such issues will be addressed in another paper.

2.3 M2C Mathematical Model

The M2C can be seen in Fig-2 and its detailed mathematical modeling can be analyzed with precise detail in [11] and [95-96]. An analysis of the loop corresponding to the circulating current i_{circ} through Kirchhoff's current law (KCL) has the following:

$$i_{circ} = i_{Ua} - \frac{i_a}{2} = i_{Da} + \frac{i_a}{2}$$
$$i_{circ} = \frac{1}{2}(i_{Ua} + i_{Da}) \quad (1)$$

Still analyzing the Fig-2, it's noticeable that M2C has two arms (upper and lower arm) which have four cells each in a way that there are multiple other arms belonging to the a, b and c phases. It can be said that the output voltage is the sum of the capacitors relative to each half bridge SM, where, through analyses of the circuit respective to the a-phase by Kirchhoff's voltage law (KVL) and considering $j$as the corresponding number of each upper and lower arms capacitor (1 to 8):

$$V_d = \sum_{j=1}^{8} v_{ja} + L_{bf}\frac{d}{dt}(i_{Ua} + i_{Da}) \quad (2)$$

The capacitors average voltage, which is a very useful control system developed by [11], can be easily obtained by analyzing the circuit of Fig-2 for each phase. Therefore:

$$\bar{v}_{Ca} = \frac{1}{8}\sum_{j=1}^{8} v_{ja} \quad (3)$$

It is known that the nominal energy of the SM capacitors is given by:

$$E_{SM} = \frac{1}{2}Cv_{ja}^2 \quad (4)$$

The nominal voltage of each SM (using as example an a-phase SM) can be obtained by:

$$v_{ja} = \frac{V_d}{N} \quad (5)$$

Considering N cells per arm one can obtain the nominal energy stored by each arm of the converter as [97]:

$$E_{SM} = \frac{N}{2}Cv_{ja}^2 \quad (6)$$

It is known that the mean time of the SM's voltages is close to v_{ja} so that it is possible to control the mean time of the sub-module voltages by controlling the energy stored in the converter. Another important factor is that the voltage of each SM will vary by the time the capacitors charge and discharge due to the current of the arms. From this assertion, was created in [97] a factor that defines the upper limit of voltage of the capacitors so that the instantaneous value of the voltage of these never be higher than k_{max} and also the sizing of the capacitors in SM based in energy storage. This analysis can be seen in more detail in [97] and has the relation below.

$$v_{ja} \leq k_{max}\frac{V_d}{N} \quad (7)$$

$$C = \frac{2NE_{nom}}{V_d^2} \quad (8)$$

The active input power of the M2C converter can be calculated as

$$p_d = V_d.I_d \quad (9)$$

Still in the work [97], it was verified that the insertion of third harmonic in the method of modulation drastically reduces the requirement of storage of energy in the capacitors. However, the method addressed by [98] was used.

Initially used in a static var compensator (SVC), a unified constant was developed in order to aid in the design of capacitors of the SM called unit capacitance Constant (H). This constant is defined as a mean of all the electrostatic energy stored in the capacitors and is defined in seconds [11]. The constant H can be observed below

$$H = \frac{3 \text{ x } 2N \text{ x } \frac{1}{2}Cv_{ja}^2}{P} \quad (10)$$

Note that the multiplication of Eq. 10 by 3 is due to the fact of considering a three-phase M2C.

2.4 Carrier-Based Modulation Techniques for M2C

Due to the huge M2C acceptance and consolidation, several modulation strategies came into being, such as space vector modulation (SVM) [99-102], Nearest Level Control [103] and Selective Harmonic Elimination (SHE) [104] among others. Related to the PWM techniques, it is possible to emphasize the techniques based on the fundamental or carrier, center of study of this article, illustrated in Fig-4.

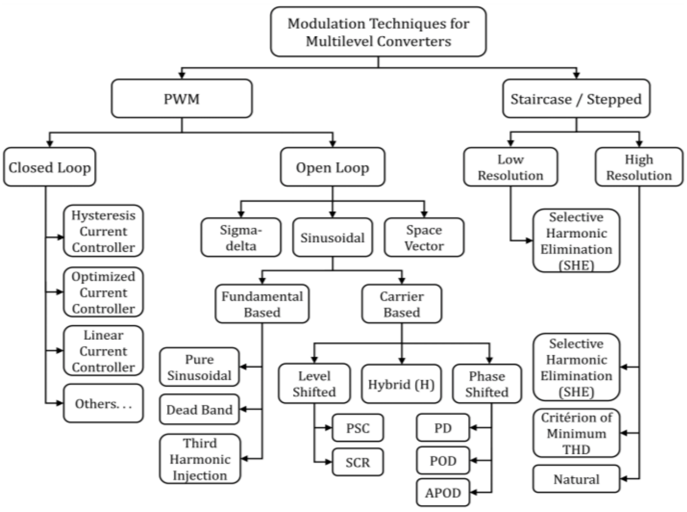


Fig-4: Main techniques of Multiple Converters modulation.

The SVM technique offers a greater degree of freedom when compared to carrier-based techniques. On the other hand, there is the disadvantage due to the fact its high number of switching vectors difficult computational processing during its control, making it into a wide guide technique since the converter needs the phase redundancy during the balancing of the capacitors instead of inserting it in the line-to-line voltage, as it happens with the NPC inverters. The technique of multiple carrier displaced in level or phase shifted carrier PWM (PSCPWM), however, has the advantage of also distributing the energy between the SM, which contributes to the voltage balance of the capacitors and the getting of a satisfactory internal current. On the other hand, it has worse harmonic content in the line-to-line voltages when compared to the phase disposition technique PWM (PDPWM) because it does not synthesize the closest PWM level in these voltages. The carrier-level distribution characteristic of PDPWM modulates a higher harmonic energy concentration in the carrier frequency, but the line-to-line voltage is unharmed [105-107].

Still on the PDPWM technique, it is not the most suggested for the M2C because it promotes unevenly the energy distribution between the SM capacitors, however it has been used in HVDC applications for allowing the M2C control with low modulation frequencies and small indexes of frequency modulation (m_f) and voltage [105]. m_f being defined as:

$$m_f = \frac{f_c}{f_{fund}} \quad (11)$$

Aiming to minimize such disadvantages from the the level shifted (LS) carrier techniques, works were made in which the it was used signal rotation [108], carrier rotation [109], and modified carrier rotation techniques [110] to promote the balanced distribution of voltage across all capacitors of the SM. In general, the carrier based PWM (CB-PWM) techniques have a big adaptation to the multilevel modular converter and greatly help its control, although the the techniques with phase shifted (PS) carriers such as PSCPWM (Fig-5 (d)) and the sawthooth carrier rotation PWM (SCRPWM) (Fig-5 (e)) tend to offer the best results tend to offer better results by contributing to the capacitor balance and evenly distributing the energy between the static switches of the converter because the multiple carriers have the same amplitude and better distribute the voltage ripples on the capacitors.

This article will investigate the M2C performance in face of the carrier based phase and level techniques such the PDPWM (Fig-5(a)), the phase opposition disposition PWM (PODPWM) (Fig-5(b)) and the alternative phase opposition disposition PWM (APODPWM) (Fig-5 (c)) when the converter's system uses a great control technique developed by [11].

In the carrier-based modulations, for N SM per arm of the converter, it is usually used, N triangular or sawtooth carriers that have sine wave reference as the fundamental wave. In the LS modulations, the carriers are distributed continuously and uniformly over the entire vertical extent of V_{dc} thus generating different levels of location for each carrier, i.e. a vertical carrier distribution. For the PDPWM modulation, all the carriers are arranged in the same phase. In PODPWM, the positive and negative carriers have 180° displacement between them. In APODPWM modulation, consecutive pairs of carriers are 180° out of phase. On the other hand, the PS modulations distribute the carriers at the same vertical level, but with a 360/N phase shift between them, thus characterizing a horizontal carrier distribution. Recalling that PS modulation carriers may be sawtooth (SCRPWM) or triangular (PSCPWM) [111].

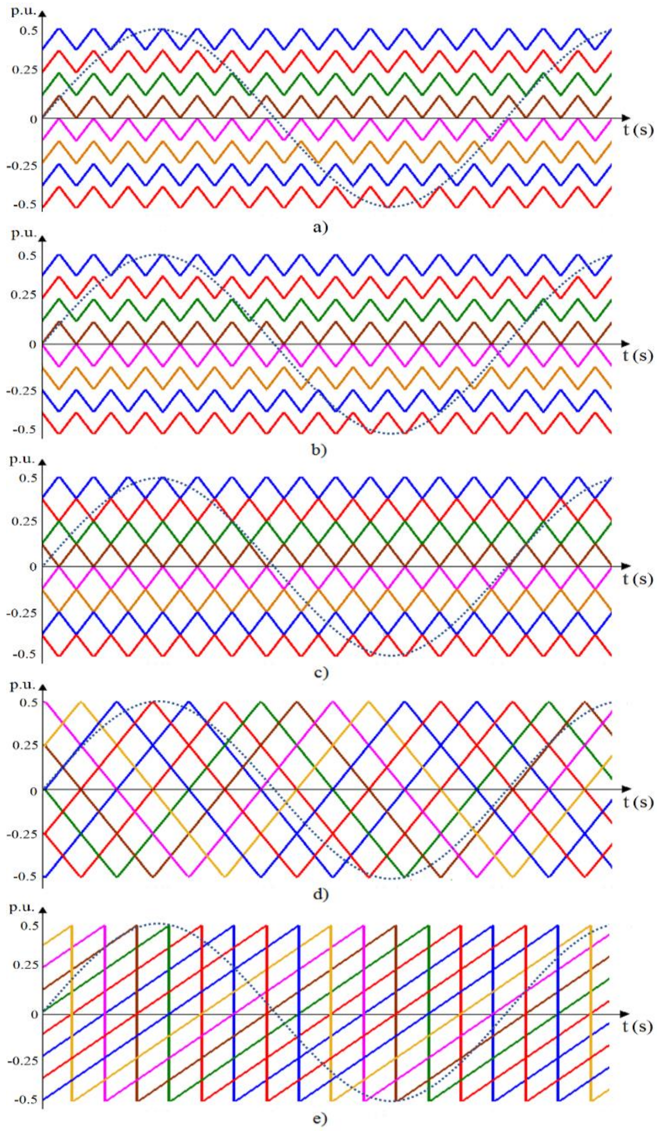


Fig-5: Sketch of PWM modulation techniques based on multiple carriers considering a sine wave as a fundamental wave. (a) PDPWM. (b) PODPWM. (c) APODPWM. (d) PSCPWM. (e) SCRPWM.

The multi-carrier PWM techniques can be seen in Fig-5 and a more in-depth approach to them can be seen in [105], [112-114].

2.5 Voltage Capacitor Balancing and Circulation Current Control Technique for the M2C

One of the intrinsic problems of the M2C topology is the existence of "circulating currents" in the converter arms during its operation. These currents are quite undesirable because they cause failures in the energy transmission between the DC and AC terminals, stress in the semiconductor devices and generate internal losses, which directly damages the efficiency of the converter. The understanding of the emergence of such currents as well as the prediction of their behavior towards the components of the converter is the key point for the elaboration of control methods [71-90] and component sizing [91-95] in many researches. There are important contributions in the literature on studies of control and suppression of circulating currents in [102-106].

Another challenge is to achieve the converter's individual capacitor balancing. Regarding to this, works such as [105-117] propose distributed balancing techniques so that the largest and smallest values corresponding to the capacitor voltages were selected and distributed according to the current direction of the upper and lower arms.

The work [104] proposed a method of open-loop control in which it was used the SHE modulation technique. However, this system displayed a slow dynamics and capacitors of high capacitance were required to minimize the high voltage ripples [112]. In [118] a predictive control model was developed that eliminates circulating currents through the use of minimization of the cost of this topology's function. However, the research [119] obtained, without having to compensate through an external signal, the SM's voltage balance of the capacitors through a directive selective modulation in the virtual loop selective mapping. In the work [120], the SM capacitor balance was obtained through a voltage control of the automatic balancing mechanism as the pulse patterns changed periodically [105].

In [121], it was discussed, analytically, the capacitor's voltage balancing using a control with rotation of switching, and in [122] the switching was reduced and the voltage of the capacitors of each sub-module was balanced through an algorithm which made it possible to avoid damage caused by undesired switching through effective mitigation measures. It was developed in [123] a selective loop polarization mapping method where the PDPWM modulation was modified to promote SM capacitor balancing. In [124] SM capacitors controllers were obtained independently through PSCPWM modulation and adjusting the reference signal of each SM, reinforcing the central idea of this work. In addition, in [125] a stable voltage control method to perform average and balanced controls of floating capacitors. In [126] the M2C was controlled through internal and external balancing of the capacitor voltages of the SM, which was formed by the sum of cell groupings of each arm containing 264 SM's in total [105].

One can find in [11] balancing technique of these capacitors using PI control and without the use of external circuit. This approach was applied in this work due to its great practicality and strength by associating the capacitor's control of the average voltage, which forces the voltage $\bar{v}_{Ca}$ to follow v_a^* next to the balancing control of the capacitors. The diagrams of such technique can be seen, briefly, in Figs. 6 and 7, where an M2C converter of 4 SM per arm was used in this design, as shown in Fig-1.

It should be noted that the diagrams and illustrations in this work, although only demonstrate the a-phase, they are also logically applied in the b and c phases as well.

It is noted that in the diagram of Fig-6 (a) the idealized voltage for each capacitor (v_c^*) is subtracted by the average voltage of the capacitors ($\bar{v}_{Ca}$), given in (3), and then passed by a control PI proportional-integral) in order to make ($\bar{v}_{Ca}$) follow the command signal (v_c^*).

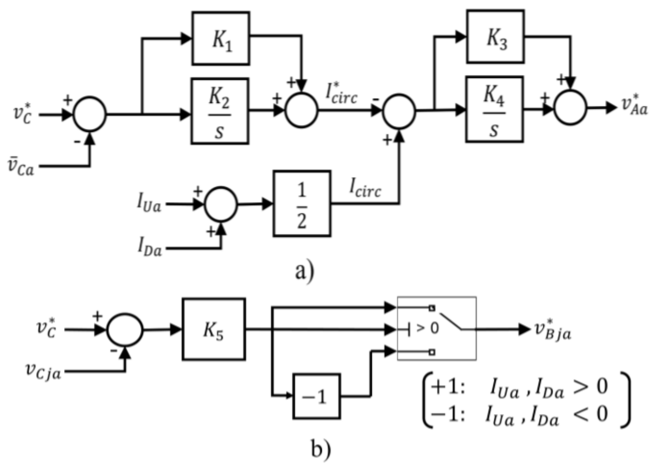


Fig-6: Diagram of M2C control blocks for a-phase: (a) Average control and (b) control of capacitor voltage balancing.

The second loop, displayed in the right portion of Fig-6 (a), forces i_{circ} to follow the control voltage i_{circ}^* and, due to this feedback control, $\bar{v}_{Ca}$ is released to follow the v_c^* command without the intervention of the load current i_u. In a way that i_{circ}^* increases when $v_c^* \geq \bar{v}_{Ca}$ [11]. The mechanism summarized above is described as average control and it is given as:

$$v_{Aa}^* = K_3(i_{circ} - i_{circ}^*) + K_4 \int (i_{circ} - i_{circ}^*)\, dt \quad (12)$$

The command current will be:

$$i^*_{circ} = K_1(v^*_c - \bar{v}_{Ca}) + K_2 \int (v^*_c - \bar{v}_{Ca})\, dt \quad (13)$$

In Fig-6 (b) it is observed the capacitor balancing control so that, for the upper SM (j from 1 to 4) and considering the a-phase as an example, is obtained:

$$V^*_{Bja} = \begin{cases} K_5(v^*_C - v_{Cja}), & i_{Ua} > 0 \\ -K_5(v^*_C - v_{Cja}), & i_{Ua} < 0 \end{cases} \quad (14)$$

For the lower arms (j from 5 to 8):

$$V^*_{Bja} = \begin{cases} K_5(v^*_C - v_{Cja}), & i_{Da} > 0 \\ -K_5(v^*_C - v_{Cja}), & i_{Da} < 0 \end{cases} \quad (15)$$

Based on the Fig-6 (b), (7) and (8) diagram, it is noted that V^*_{Bja} has its signal dictated by the positive or negative result of the subtraction of currents i_{Ua} and i_{Da}. A positive active power will be obtained from the DC source of the four upper SM (for j from 1 to 4) when $v^*_c \geq v_{Cja}$. When $i_{Ua}$is positive, the product of v_{Bja} and i_{Ua} forms the active power and when i_{Ua} is negative, the v_{Bju} polarity must be inverted in order for the active power to become positive [11].

In Fig-7 it is possible to analyze the control diagram of the SM of the M2C converter based on the acquirement of the idealized voltage.

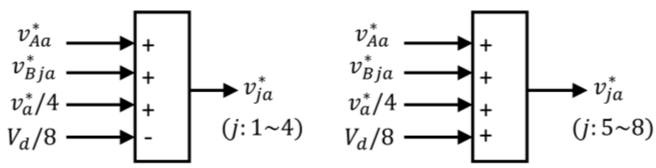


Fig-7: Feedfoward control of Choppers cells belonging to the upper (j: 1 ~ 4) and lower (j: 5 ~ 8) arms of a-phase of the proposed M2C converter.

Based on the Fig-7 diagram, one obtains:

$$v^*_{ja} = v^*_{Aa} + v^*_{Bja} + \frac{v^*_a}{4} - \frac{V_d}{8} \quad (16)$$

$$v^*_{ja} = v^*_{Aa} + v^*_{Bja} + \frac{v^*_a}{4} + \frac{V_d}{8} \quad (17)$$

At a final stage, the control voltage v^*_{ja} is normalized by each DC voltage of the capacitors (v_{Cja}) and then compared by the idealized carrier (triangular or sawtooth) to pass through the desired multicarrier modulation process [11]. As the topology of this work has 4 cells per arm (N = 4), it will be obtained 8 cells per phase considering the upper and lower arm, which for a PS modulation will require a phase difference of $360/2N =$ 45°. Due to the 8 SM per phase the drive will have an equivalent switching frequency of $f_{eq} = 8f_C$.

The reference signal v^*_a is crucial for the control and is given by:

$$v^*_a = V(\sqrt{2})(\sqrt{3})\sin(2\pi f t) \quad (18)$$

or leaving in function of the DC bus, for each phase, is obtained

$$v^*_a = \frac{V_d}{2}\sin(2\pi f t)$$

$$v^*_b = \frac{V_d}{2}\sin\left(2\pi f t + \frac{2\pi}{3}\right)$$

$$v^*_c = \frac{V_d}{2}\sin\left(2\pi f t - \frac{2\pi}{3}\right) \quad (19)$$

where it was considered $f = 60\ Hz$ e $V_d = 9\ kV$.

3. SIMULATIONS AND RESULTS

For the project in question, an M2C was designed to control an induction motor with an active power of 1 MW and a load power factor of 0.9 to 60 Hz. Based on these parameters, the load resistors and inductors were designed. For comparative purposes, the rated line-to-line rms voltage of 5.5 kV and the Rated RMS current of 105A were designed to test the different multi-carrier techniques.

Once the active power and PF of the system are stipulated, the apparent power of 1.11 MVA and inductive power angle of approximately 25.8º are obtained.

Another very important parameter is the unit capacitance constant. Knowing that the number of SM per arm is 4 (N = 4) and replacing the capacitance and active power stipulated for the system in (10), is obtained:

$$H = \frac{(12)(1.9)(10^{-3})(2.25^2)(10^6)}{10^6} = 115\ s \quad (20)$$

As in [11], 2.37pu (1.9mF) was stipulated for the SM's capacitors. Therefore, according to (6), the energy of each SM capacitor will be:

$$E_{SM} = \tfrac{1}{2}(1.9)(10^{-3})(2.25^2)(10^6) = 4.81\ kJ \quad (21)$$

Based on the modeling and graphics described in [97] it is also possible to obtain the SM capacitance based on the energy storage of the arms for different values of k_{max} and modulation index in amplitude equal to 1. Since, knowing that the system has 1.11MVA under 25.8º inductive power angle, the required nominal power required calculated for this power angle could be 30 kJ / MVA by graphical analysis. So, to transfer 1.11MVA it

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would require a total energy of 33.3 kJ, which in turn would correspond to 3.65 kJ per arm.

Calculating the capacitance in (8) yields

$$C = \frac{(2)(4)(5.55)(10^3)}{(9^2)(10^6)} = 0.55mF \quad (22)$$

Was chosen the capacitance and methodology used in [11] (1.9mF) for comparative purposes, and in a future work the project will be done with the proposed methodology in [97] and the capacitance obtained in (22).

For the calculation of the inductors, it is known that, for network applications, the acceptable inductance values can be up to 0.1 pu [97-98]. Thus, an inductance of 9% (8mH) was provided for protection inductors in order to ensure efficient control of circulation currents and fault currents. Another important factor is that the capacitance of the SM is high enough that the maximum voltage under them does not exceed 10% of the voltage nominal value (k_{max} = 1.1) [97].

Since 4 SM per arm is used, the output voltage waveform of each phase is expected to be 9 levels and the line-to-line voltage is 17 levels.

Table-1: Simulation parameters.

Circuit Parameters		Control Parameters	
P	1 MW	K_1	0.5
V	5.5 kV	K_2	150
I	105 A	K_3	1.5
V_d	9 kV	K_4	150
f	60 Hz	K_5	$0.35.10^{-6}$
m_f	11		
fc	$f.m_f = 660$ Hz	Load Parameters	
feq	$8.fc = 5280$ Hz	PF	0.9 at 60 Hz
v_C^*	$V_d/4 = 2.25$ kV	R_{load}	3,9 Ω (12.1%)
L_{Bf}	8 mH (9,97%)	L_{load}	6 mH (6.2%)
C	1.9 mF (2.4%)	θ	25.8°
H	115 ms		

Once the simulation parameters were stipulated, the circuit was assembled on the Matlab/Simulink platform in order to observe the first simulation, in which the waveforms of the inverter's output current by means of different types of phase and level PWM multi-carrier modulation were compared.

The waveforms of the M2C output current I_a, I_b, e I_c can be observed in Fig-8 through PDPWM, PODPWM, APODPWM, PSCPWM and SCRPWM modulation techniques using the parameters of Table-1 and frequency modulation index 11 and 21.

It was observed that, for the proposed control method, the LS modulation techniques presented waveform and deformed current and with high THD, so that the APODPWM technique presented the worst results in both current and voltage in both m_f. On the other hand, it was clearly noted that the PS modulations are very well suited to this control technique because the carriers also cover the fundamental in different phases without the disadvantage of occurring, in certain moments, the absence of crossing between the carrier and the fundamental, which for this control makes unstable the deformation of capacitor balancing as well as the voltages and output currents of the system. Proof of this is in the average error module obtained in the control block of the average and capacitor voltage balancing.

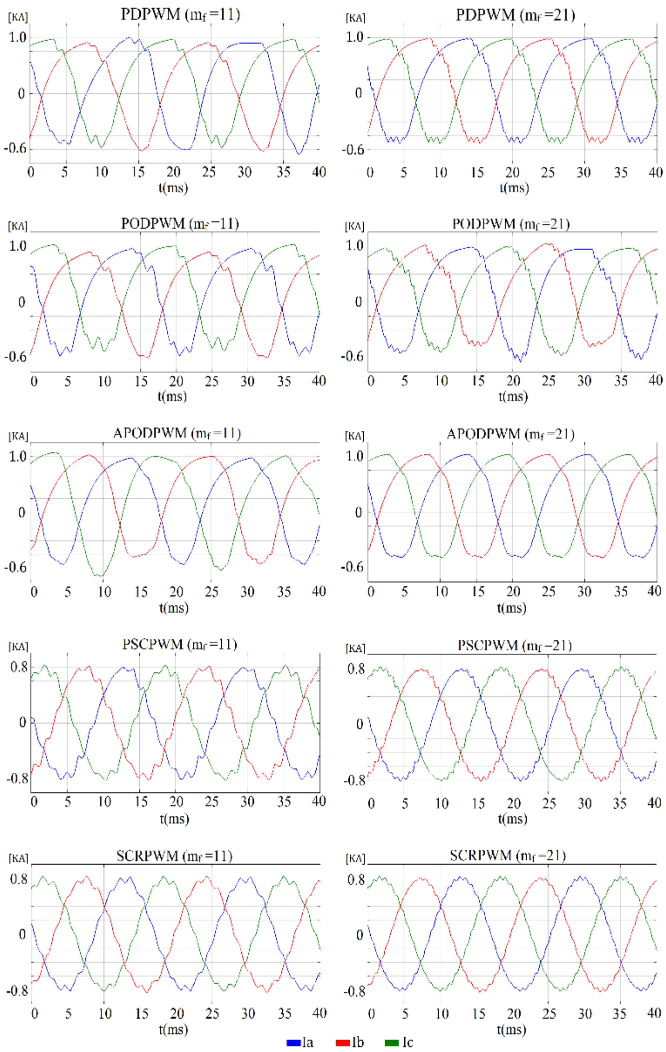

Fig-8: M2C load current for different PS and LS modulation techniques using m_f = 11 and m_f= 21.

With the simulation the Table-2 was made. In it it's possible to see the current's THD, line voltage and the average error of the control method for the first 2 seconds.

Table-2: THD of the line voltage and average error (for the first 2s) of the 5 carrier-based modulation techniques considering m_f = 11 and L = 8mH.

Strategy	THD I_a (%)	THD V_{ab} (%)	Medium Error (V)
PDPWM	28.68	40.42	215.5
PODPWM	28.99	42.85	318.7
APODPWM	24.86	37.08	200.2
PSCPWM	6.96	21.58	23.26
SCRPWM	5.13	13.24	17.94

Both the THD and the average errors of the PS techniques were much lower when compared to the LS techniques. In order to further analyze the behavior of the techniques, the graphs of Figs. 10 and 11 were made where, respectively, the M2C behavior can be seen by increasing the arm protection inductance and the frequency modulation of the index variation influence.

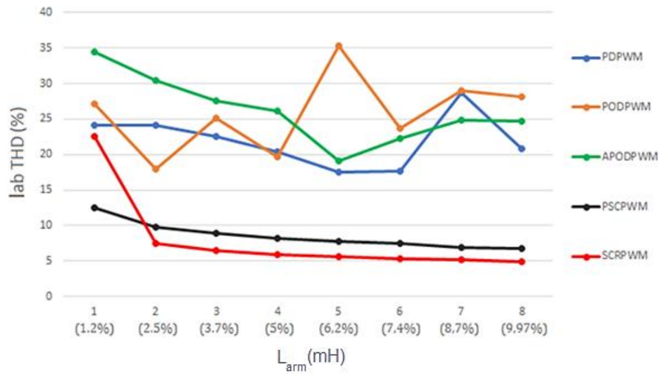

Fig-9: THD of the M2C output current by increasing the armature inductance of the converter arms to m_f = 11 for different carrier-based PWM techniques.

It was noted in Fig-9 that the LS techniques presented high THD regardless of the protection inductance variation, making such increase irrelevant and noting its instability in the proposed control system. Proof of this is in the THD random variation of the PODPWM technique and due to the deformities in the output waves seen in Fig-8. In the PS techniques the opposite is noted, as *the* L_{arm} increases the THD of the line current gradually decreases. An interesting fact is that when L_{arm} was increased from 1.2pu to 2.5pu there was a very large decrease in THD of the current for both PS techniques, but a much more significant reduction of THD was observed for the SCRPWM technique than the PSCPWM technique.

Still analyzing the behavior of the proposed M2C PWM techniques, all techniques were simulated again by stipulating L_{arm}= 8, varying m_f and observing the data obtained in Fig-10.

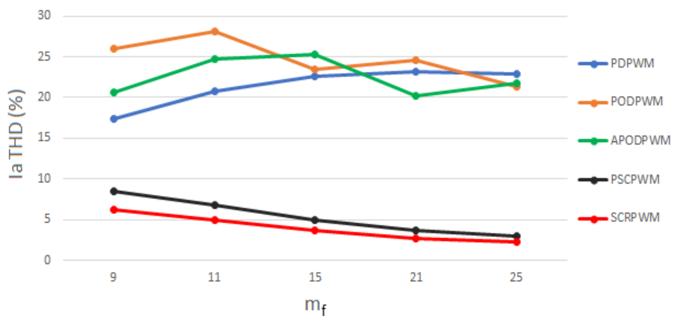

Fig-10: THD of the M2C output current by increasing m_f for different carrier-based PWM techniques, considering L_{arm} = 8 mH.

In analyzing Fig-10 it was confirmed that the LS techniques were not adequate to the balance control technique and average control. The PS techniques again presented excellent results at low modulation frequencies and, as the frequency modulation index increased, the THD gradually decreased while reasonable THD was observed for the PSCPWM and SCRPWM techniques using only m_f = 9 or carrier frequency of 540Hz.

In both simulations the SCRPWM technique obtained lower THD than the PSCPWM technique and this started a new analysis in this more detailed work in order to verify the reasons of these better results.

Table-3 shows that the values obtained from the THD for the SCRPWM technique are smaller than those of the PSCPWM technique.

Table-3: THD of the SCRPWM and PSCPWM techniques in relation to the increase of L_{arm} considering m_f = 11.

L_{arm} (mH)	SCRPWM THD I_a (%)	PSCPWM THD I_a (%)
1	22,62	12,43
2	7,54	9,76
3	6,45	8,89
4	5,93	8,26
5	5,58	7,80
6	5,31	7,44
7	5,13	6,96
8	4,95	6,73

Since it was noted that the LS techniques did not cooperate for the modulation in the proposed control technique, the output voltage waveforms, V_{ab}, were only observed for the PS techniques in order to investigate which one had the best performance. The PSCPWM load voltage waveform and SCRPWM techniques can be analyzed in Fig-11.

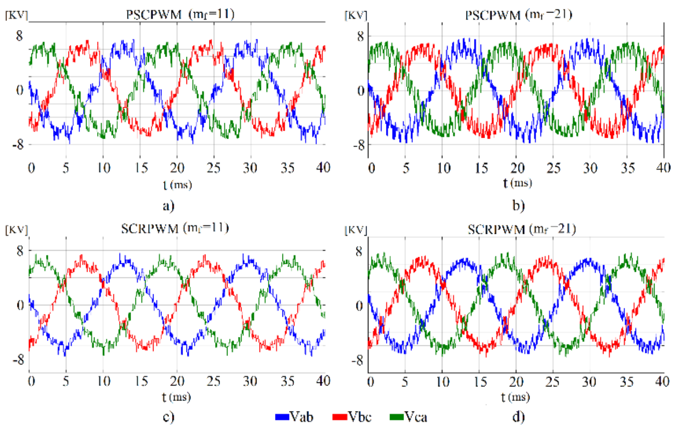

Fig-11: M2C output voltage waveforms for PSCPWM modulations using (a) m_f = 11, (b) m_f = 21 and SCRPWM considering (c) m_f = 11 and (d) m_f = 21.

As expected, a 17-level line-to-line voltage waveform due to the 4 SM per arm is observed in Fig-11. It was also observed that the SCRPWM technique had a cleaner V_{ab} waveform than the PSCPWM, which had already been observed in the form of I_a in the mean error module of the average control. It can be further observed in a comparison of the PI technique performance for Fig-12 (a) PSCPWM and Fig-12 (b) SCRPWM techniques.

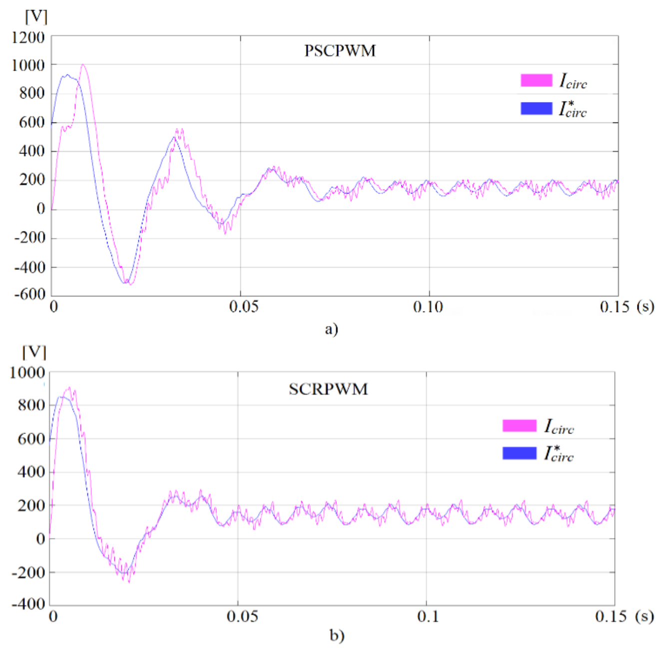

Fig-12: Control of current circulation in charge of the average control system (Fig-6) to (a) PSCPWM and (b) SCRPWM considering m_f = 11 and using the same simulation parameters.

Analyzing Fig-12, a larger overshoot of I_{circ} in the PSCPWM technique was observed in comparison to the SCRPWM and in the first 2s a smaller average error of the voltage command of I_{circ} loop was obtained. Both techniques obtained small signal synchronization time so that the SCRPWM technique stabilized at approximately 0.01s earlier than the PSCPWM technique.

It can be analyzed in Fig-13 output current waveform I_a of the upper and lower arm current in both PS techniques. Both display the standard M2C behavior and do not display significant differences between each other.

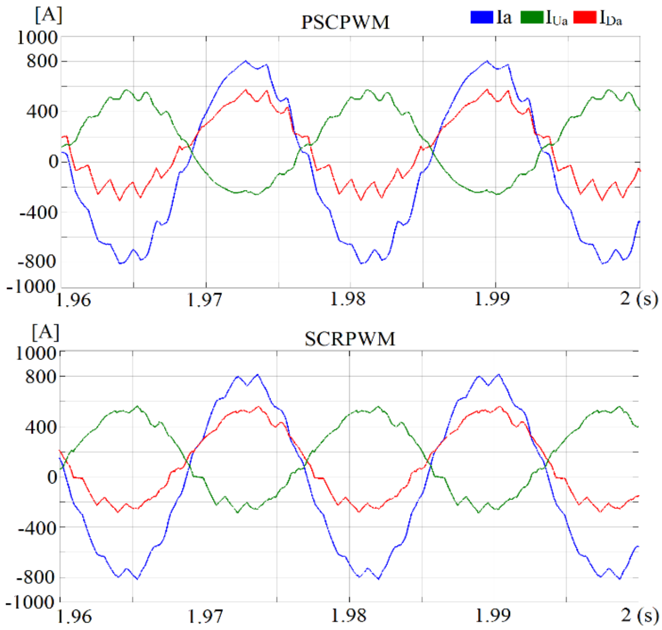

Fig-13: I_a, I_{Ua} and I_{Da} of the PSCPWM and SCRPWM techniques for the parameters described in Table-1.

Another important point to be observed is the requirement of the SM capacitors as the system was executed for both techniques. Fig-14 and Fig-15 display, respectively, the SM capacitors requirement of the PSCPWM and SCRPWM techniques.

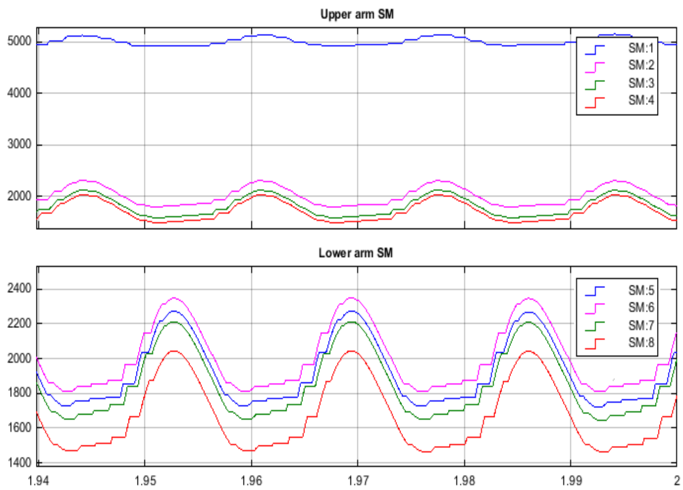

Fig-14: Steady state SM capacitor voltages of the PSCPWM technique for a-phase.

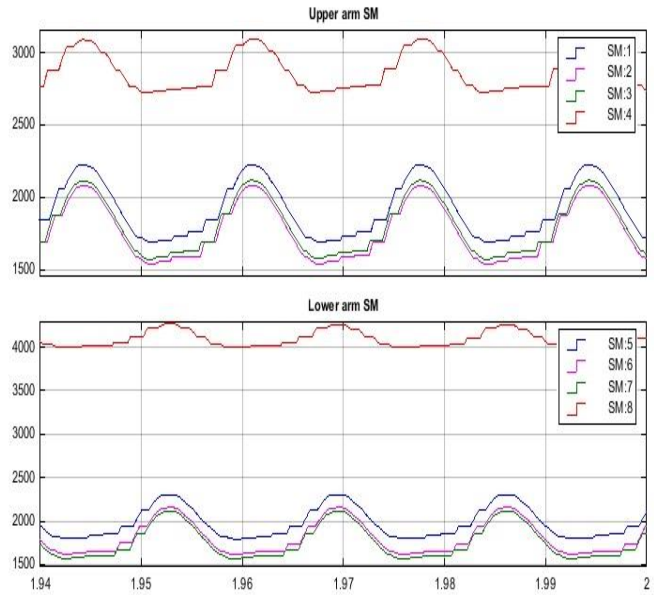

Fig-15: Steady state SM capacitor voltages of the SCRPWM technique for a-phase.

It is noted that the power distribution between SM's capacitors is more evenly balanced in the PSCPWM technique so that the voltage in the first capacitors of the upper arms of each phase stabilize with a high amount of voltage because they are connected directly to the bus DC which characterizes an imperfect energy distribution, possibly this capacitor would be damaged by continuous use earlier than the others. A positive point would be the balance between the other capacitors that have very close values and do not reach high voltage indices.

Fig-15 shows the high amount of voltage that the capacitors of 5th and 8th SM, of each phase, have stabilized to make the system work as expected. On the other hand, the other SM's did not reach high voltage values and obtained peak values very close to each other.

Finally, the spectra of all the multicarrier techniques studied in this work were assembled with the first 100 harmonics (up to 6 kHz) analyzed in this work in Fig-16 so that LS techniques were filled with the red color by the fact of not having good results for the PI control of balancing, control of the average and absence of external control circuit, used in this work, and do not collaborate for the balanced distribution of energy for the capacitors presenting thus high THD and also high harmonics of first and second order.

Analyzing the Fig-16, it's observable that the PSCPWM and SCRPWM techniques presented the best current and line voltage spectra so that the SCRPWM technique presented a THD of 8.34% less V_{ab} than the PSCPWM technique besides obtaining the SM balance faster and lower THD than I_a.

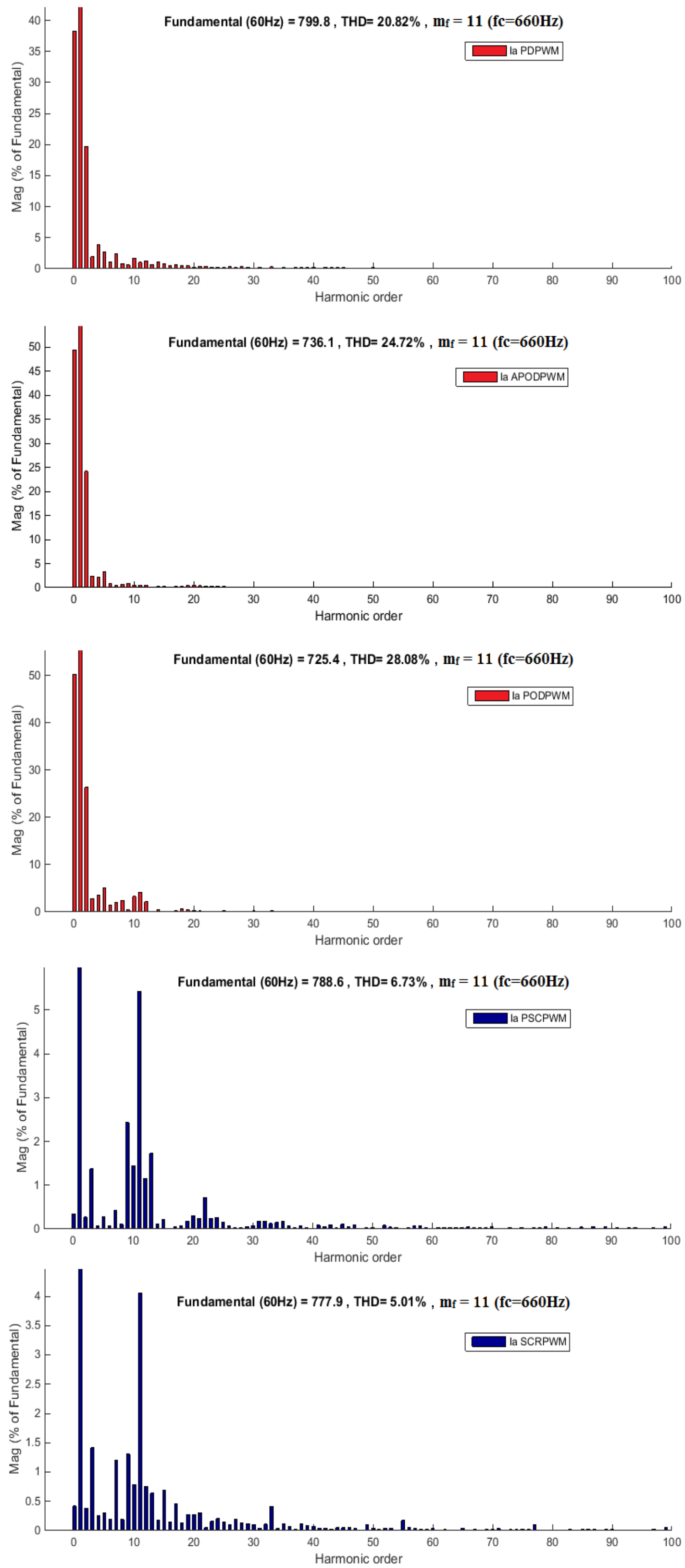

Fig-16: Harmonic spectra of current I_a for all five multi-carrier techniques studied in this work for the Table-1 parameters.

Analyzing the PS techniques for $m_f = 21$ $(f_c = 1260\ Hz)$ is obtained:

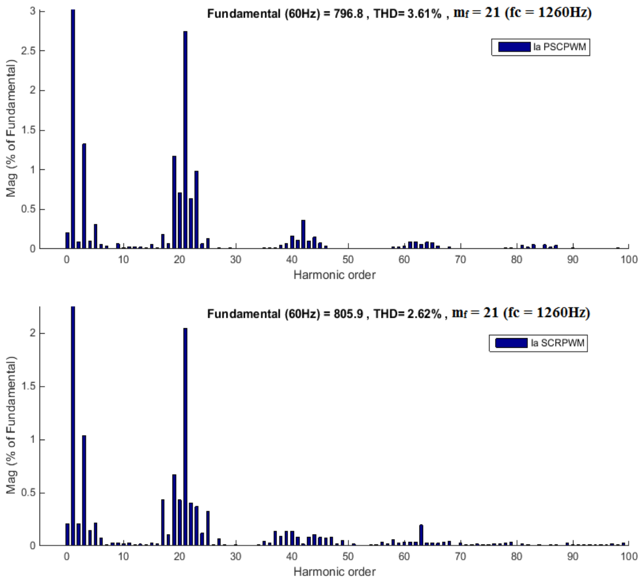

Fig-17: Harmonic spectra of current I_a for PS techniques studied in this considering $m_f = 21$ $(f_c = 1260Hz)$.

The analysis in Fig-17 reinforces the claim that the SCRPWM technique presented lower I_a THD for the proposed control method when compared with other multicarrier techniques. For carrier frequency of 660Hz and 1260Hz, respectively, the SCRPWM technique presented THD 1.7% and 1% lower than the PSCPWM technique.

4. CONCLUSIONS

In this paper, PS and LS techniques were applied comparatively to the Half Bridge Double-Star Multilevel Converter using a PI control to balance the SM capacitors voltage and to control the circulation currents without the aid of an external circuit in order to evaluate the best results for medium voltage application using a load of 1MW. It was concluded that the PSCPWM and SCRPWM techniques presented the best results in line voltage, output current and speed THD in obtaining capacitor balancing. The PI control proved to be effective in both simulations, but when using LS techniques in this control method, many intervals occurred where the carriers did not cross the fundamental one, generating switching losses and increasing the THD abruptly, making the output waveforms of line-to-line voltage and current deformed. On the other hand, the PS techniques fit perfectly into the proposed control by distributing the energy between the SM effectively as well as balancing the IGBT switch requirement.

The PSCPWM technique presented lower peak values for the capacitors although the SCRPWM technique obtained better results regarding THD, showing a better distribution due to the PSCPWM technique but better performance for the SCRPWM technique. Was investigated different methods of obtaining the SM capacitance as well as the optimal use of the arm protection inductance in pu units proving that as L_{arm} increased the THD gradually decreased and the influence of m_f was analyzed and even when one can obtain good current and line-to-line voltage for low values of m_f.

REFERENCES

[1] M. A. Perez, Bernet S., Rodriguez J., Kouro S., Lizana R., “Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters”, IEEE Transactions on Power Electronics, Vol. 30, Nº 1, Jan. 2015.

[2] J. Rodriguez, L. Jih-Sheng, P. Fang Zheng, “Multilevel Inverters, a Survey of Topologies, Controls, and Applications”, IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, Aug 2002.

[3] A. Lesnicar, R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range”, Proc. IEEE Power Tech Conf., 2003, vol. 3, pp. 23–26.

[4] R. Baker, L. Bannister, “Electric Power Converter”, U.S. Patent 3 867 643, Feb. 1975.

[5] T. Meynard, H. Foch, “Multi-Level Conversion, High Voltage Choppers and Voltage Source Inverters”, Power Electronics Specialists Conference, 1992. PESC “92 Record. 23ª Annual IEEE, pp. 397-403 vol. 1, 1992.

[6] R. H. Baker, “High-Voltage Converter Circuit”, U.S. Patent, 04 203 151, May 1980.

[7] W. Mcmurray, “Fast Response Stepped-Wave Switching Power Converter Circuit”, US Patent No. 3,581,212, Filed 31 July 1969, Granted 25 May 1971.

[8] P. Fang Zheng, “A generalized multilevel inverter topology with self voltage balancing”, IEEE Transactions on Industry Applications, vol. 37, no. 2, pp. 611-618, Mar/Apr 2001.

[9] R. Marquardt, A. Lesnicar, J. Hildinger, “Modulares Stromrichterkonzept Für Netzkupplungsanwendungen Bei Hohen Spannungen”, ETG-Conference, 2002.

[10] A. Lesnicar, R. Marquardt, “A New Modular Voltage Source Inverter Topology”, Proc. EPE, vol. 3, pp. 2–4, 2003.

[11] M. Hagiwara, H. Akagi, “Control and Experiment of Pulsewidth Modulated Modular Multilevel Converters”, IEEE Trans. Power Electronics, vol. 24, no. 7, pp. 1737-1746, July 2009.

[12] A. Alesina, M. Venturini, "Solid-State Power Conversion, A Fourier Analysis Approach To Generalized Transformer Synthesis", Circuits and Systems. IEEE Transactions on, Vol. 28, No. 4, pp. 319, 330. Apr. 1981.

[13] "Yaskawa", http,//www.yaskawa.eu.com, accessed 28 March 2017.

[14] "Grupo Jema", http,//www.grupojema.com, accessed 28 March 2017.

[15] "TMEIC-GE", http,//www.tmeic.com, accessed 28 March 2017.

[16] "Eaton", http,//www.eaton.com, accessed 28 March 2017.

[17] "LS Industrial Systems", http,//eng.lsis.biz/, accessed 28 March 2017.

[18] "Converteam", http,//www.converteam.com, accessed 28 March 2017.

[19] "Arrowspeed", http,//www.arrowspeed.com, accessed 29 March 2017.

[20] "Rongxin Power Electronic Co. (RXPE)", http,//www.rxpe.co.uk, accessed 29 March 2017.

[21] "Beijing Leader & Harvest Electric Technologies", http,//www.ld-harvest.com, accessed 29 March 2017.

[22] "Ingeteam", http,//www.ingeteam.com, accessed 29 March 2017.

[23] "Ansaldo Sistemi Industriali", http,//www.prismaservices.com/ansaldo-sistemi-industriali, accessed 29 March 2017.

[24] M. Spichartz, V. Staudt, A. Steimel, "Modular Multilevel Converter for Propulsion System of Electric Ships", 2013 IEEE Electric Ship Technologies Symposium (ESTS), Arlington, VA, 2013, pp. 237-242.

[25] K. Thantirige, A. K. Rathore, S. K. Panda, G. Jayasignhe, A. M. Zagrodnik, A. K. Gupta, "Medium voltage multilevel converters for ship electric propulsion drives", 2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS), Aachen, 2015, pp. 1-7.

[26] J. John, J. Jose, "A three phase step up multilevel inverter for aircraft applications", 2016 International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT), Chennai, 2016, pp. 405-408.

[27] M. Z. Youssef, M. Orabi, M. Tarbouchi, "Design of an efficient multilevel inverter for a 1500V railway propulsion system applications", 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, 2015, pp. 1197-1201.

[28] B. Baroni, "Aplicação Do Conversor Multinível Modular em Transmissão HVSC Com Eliminação Seletiva de Harmônicos", masters dissertation, UFMG, 2012.

[29] N. Flourentzou, G. V. Agelidis, D. G. Demetriades, "VSC-based HVDC power transmission systems, An overview", IEEE Trans. Power Electron., vol. 24, no. 3, pp. 592–602, Mar. 2009.

[30] S. Allebrod, R. Hamerski, R. Marquardt, "New Transformerless, Scalable Modular Multilevel Converters For HVDC-Transmission". Power Electronics Specialists Conference. PESC 2008. IEEE, pp. 174-179, 2008.

[31] M. Saeedifard, R. Iravani, "Dynamic Performance Of A Modular Multilevel Back-To-Back HVDC System, Power Delivery", IEEE Transactions on 25(4), 2903-2912, 2010.

[32] B. Chuco, E. Watanabe, "Back-To-Back HVDC Based On Modular Multilevel Converter", COBEP2011, 2011.

[33] N. Serbia, "Modular Multilevel Converters for HVDC power stations", doctoral thesis, Université de Toulouse, 2014.

[34] B. Paucar, "Sistema HVDC Baseado Em Conversores Multinível Modulares", doctoral thesis, COPPE/UFRJ, 2014.

[35] M. Glinka, R. Marquardt, "A New Ac/Ac Multilevel Converter Family Applied to a Single Phase Converter, Power Electronics And Drive Systems", PEDS 2003, The Fifth International Conference on, Vol. 1, pp. 16 - 23 Vol.1, 2003.

[36] F. Deng, Z. Chen, "A new structure based on cascaded multilevel converter for variable speed wind turbine", IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, Glendale, AZ, 2010, pp. 3167-3172.

[37] Y. Koyama, T. Arai, R. Hasegawa, D. Suzuki, "One-pulse control for modular multilevel converter based STATCOM", 2016 18th European Conference on Power Electronics and Applications (EPE"16 ECCE Europe), Karlsruhe, 2016, pp. 1-10.

[38] A. Ferreira, O. Gomis-Bellmunt, M. Teixidó, "HVDC-based modular multilevel converter in the STATCOM operation mode", 2016 18th European Conference on Power Electronics and Applications (EPE"16 ECCE Europe), Karlsruhe, 2016, pp. 1-10.

[39] W. Zhao, K. Yang, G. Chen, "An improved nearest-level-modulation of modular multilevel converter -

STATCOM", 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, Sydney, NSW, 2015, pp. 219-223.

[40] W. Zhang, Q. Gao, B. Su, M. Jin, D. Xu, J. Liu, "Research on the control strategy of STATCOM based on modular multilevel converter", 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), Hiroshima, 2014, pp. 614-618.

[41] X. Liu, J. Lv, C. Gao, Z. Chen, S. Chen, "A Novel STATCOM Based on Diode-Clamped Modular Multilevel Converters", in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 5964-5977, Aug. 2017.

[42] G. Tsolaridis, E. Kontos, H. Parikh, M. R. Sanchez-Loeches, Teodorescu R., Chaudhary S. K., "Control of a Modular Multilevel Converter STATCOM under internal and external unbalances", IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 6494-6499.

[43] Sanz I., Moranchel M., Bueno E. J., Rodriguez F. J., "Analysis of medium voltage modular multilevel converters for FACTS applications", IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 6459-6464.

[44] Chen Y., Zhao S., Li Z., Wei X., Kang Y., "Modeling and Control of the Isolated DC–DC Modular Multilevel Converter for Electric Ship Medium Voltage Direct Current Power System", in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 5, no. 1, pp. 124-139, March 2017.

[45] Zapico A., Lopez M., Rodriguez A., Briz F., "Fault tolerant cell design for MMC-based multiport power converters", 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

[46] Yin C., Yu J., Atkinson D., "Effective voltage balancing control for Modular Multilevel Converter without current sensors", 10th International Conference on Advances in Power System Control, Operation & Management (APSCOM 2015), Hong Kong, 2015, pp. 1-5.

[47] Lai J. S., Peng F. Z., "Multilevel converters – A new breed of power converters", IEEE Trans. Ind. Applicat., vol. 32, pp. 509–517, May/June 1996.

[48] Peftitsis D., Tolstoy G., Antonopoulos A., Rabkowski J., Lim J. K., Bakowski M., Angquist L., Nee H. P., "High-Power Modular Multilevel Converters With SiC JFET"s". In, IEEE Transactions On Power Electronics, Vol. 27, Nº 1, Jan. 2012.

[49] Korn A., Winkelnkemper M., Steimer P., "Low Output Frequency Operation Of The Modular Multi-Level Converter". Energy Conversion Congress and Exposition (ECCE), 2010 IEEE, pp. 3993-3997, 2010.

[50] Tolbert L., Peng F.-Z., Habetler T., "Multilevel converters for large electric drives", IEEE Trans. Ind. Applicat., vol. 35, pp. 36–44, Jan./Feb. 1999.

[51] Teodorescu R., Beaabjerg F., Pedersen J. K., Cengelci E., Sulistijo S., Woo B., Enjeti P., "Multilevel converters - A survey", in Proc. European Power Electronics Conf. (EPE"99), Lausanne, Switzerland, 1999, CD-ROM.

[52] Akagi H., "Medium-voltage power converters and motor drives", in Conf. Rec. European Center for Power Electronics, Zurich, March 2009, CD-ROM

[53] Hammond W. P., "A new approach to enhance power quality for medium voltage AC drives", IEEE Trans. Ind. Applicat., vol. 33, pp. 202-208, 1997.

[54] T. A. Meynard, H. Foch, P. Thomas, J. Courault, R. Jakob, M. Nahrstaedt, "Multicell converters, Basic concepts and industry applications," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 955–964, Oct. 2002.

[55] M. Hagiwara, K. Nishimura, H. Akagi, "A Modular Multilevel Pwm Inverter For Medium Voltage Motor Drives", Energy Conversion Congress and Exposition. ECCE 2009. IEEE, pp. 2557-2564, 2009.

[56] P. Mohammadi, M. Bina, "A Transformerless Medium-Voltage Statcom Topology Based On Extended Modular Multilevel Converters", Power Electronics, IEEE Transactions on 26(5), 1534 -1545, 2011.

[57] M. Hagiwara, R. Maeda, H. Akagi, Theoretical Analysis and Control of the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC), The 2010 International Power Electronics Conference (IPEC). Jun. 2010.

[58] P. Bresesti, L. W. Kling, L. R. Hendriks, R. Vailati, "HVDC connection of offshore wind farms to the transmission system", IEEE Trans. Energy Convers., vol. 22, no. 1, pp. 37–43, Mar. 2007.

[59] Y. Jin, E. J. Fletcher, J. O"reilly, "Multiterminal dc wind farm collection grid internal fault analysis and protection design", IEEE Trans. Power Del., vol. 25, no. 4, pp. 2308–2318, Oct. 2010.

[60] B. M. H. Nunes, "Nova Topologia De Conversor Multinível Para Parques Eólicos Marinhos", masters dissertation, IST, 2010.

[61] D. Iannuzzi, L. Piegari, P. Tricoli, "A novel PV-modular multilevel converter for building integrated photovoltaics", 2013 Eighth International Conference and Exhibition on Ecological Vehicles and Renewable Energies (EVER), Monte Carlo, 2013, pp. 1-7.

[62] J. Mei, B. Xiao, K. Shen, M. L. Tolbert, Y. J. Zheng, "Modular Multilevel Inverter with New Modulation Method and Its Application to Photovoltaic Grid-Connected Generator", in IEEE Transactions on Power Electronics, vol. 28, no. 11, pp. 5063-5073, Nov. 2013.

[63] R. O. Raghi, J. M. Geisa, "Multilevel Converter Topology With Reduced Switching Elements for Electric Vehicle", 2016 International Conference on Energy Efficient Technologies for Sustainability (ICEETS), Nagercoil, 2016, pp. 647-652.

[64] Pereira B. F. I. F., "Projectar, Simular e Implementar um Inversor Multinível", masters dissertation, FEUP, 2008.

[65] H. Akagi, "Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC)", IEEE Transactions on Power Electronics, vol. 26, no. 11, pp. 3119-3130, Nov. 2011.

[66] W. Kawamura, M. Hagiwara, H. Akagi, "Control and Experiment of a Modular Multilevel Cascade Converter Based on Triple-Star Bridge Cells", IEEE Transactions on Industry Applications, vol. 50, no. 5, pp. 3536-3548, Sept.-Oct. 2014.

[67] N. Ahmed, L. Ängquist, A. Antonopoulos, L. Harnefors, S. Norrga, P. H. Nee, "Performance of the modular multilevel converter with redundant submodules", IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, 2015, pp. 003922-003927.

[68] G. Konstantinou, J. Pou, S. Ceballos, G. V. Agelidis, "Active Redundant Submodule Configuration in Modular Multilevel Converters", in IEEE Transactions on Power Delivery, vol. 28, no. 4, pp. 2333-2341, Oct. 2013.

[69] P. W. Hammond, "Enhancing the reliability of modular medium-voltage drives", IEEE Transactions on Industrial Electronics, vol. 49, no. 5, pp. 948-954, Oct 2002.

[70] M. Rastogi, W. P. Hammond, H. R. Osman, "High performance, high reliability medium voltage drives", 4th IEEE International Conference on Power Electronics and Drive Systems. IEEE PEDS 2001 - Indonesia. Proceedings (Cat. No.01TH8594), 2001, pp. 259-264 vol.1.

[71] S. Haghnazari, M. Shahbazi, R. M. Zolghadri, "A new fault detection method for modular multilevel converter semiconductor power switches", IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, Yokohama, 2015, pp. 000050-000055.

[72] B. Li, Y. Zhang, R. Yang, G. Wang, D. Xu, "An IGBT open-circuit fault detection method for modular multilevel converters", 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 1573-1578.

[73] M. Abdelsalam, I. M. Marei, S. Tennakoon, "An Integrated Control Strategy with Fault Detection and Tolerant Control Capability Based on Capacitor Voltage Estimation for Modular Multi-level", in IEEE Transactions on Industry Applications, vol.PP, no.99, pp.1-1.

[74] Q. Yang, J. Qin, M. Saeedifard, "Analysis, Detection, and Location of Open-Switch Submodule Failures in a Modular Multilevel Converter", IEEE Transactions on Power Delivery, vol. 31, no. 1, pp. 155-164, Feb. 2016.

[75] S. Shao, C. J. Clare, J. A. Watson, W. P. Wheeler, "Detection and isolation of multiple faults in a modular multilevel converter based on a sliding mode observer", 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, 2014, pp. 3491-3495.

[76] S. Haghnazari, M. Khodabandeh, R. M. Zolghadri, "Fast fault detection method for modular multilevel converter semiconductor power switches", in IET Power Electronics, vol. 9, no. 2, pp. 165-174, 2 10 2016.

[77] F. Deng, Z. Chen, R. M. Khan, R. Zhu, "Fault Detection and Localization Method for Modular Multilevel Converters", IEEE Transactions on Power Electronics, vol. 30, no. 5, pp. 2721-2732, May 2015.

[78] S. Shao, W. P. Wheeler, C. J. Clare, J. A. Watson, "Fault Detection for Modular Multilevel Converters Based on Sliding Mode Observer", IEEE Transactions on Power Electronics, vol. 28, no. 11, pp. 4867-4872, Nov. 2013.

[79] H. Xing, Z. Jianzhong, X. Shuai, J. Yongjiang, "Fault diagnosis of modular multilevel converters based on extended state observer", 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Vancouver, BC, 2016, pp. 1-6.

[80] M. Sen, M. Alaraj, D. J. Park, "Open circuit fault detection and localization in modular multilevel converter", 2016 North American Power Symposium (NAPS), Denver, CO, 2016, pp. 1-6.

[81] K. Shen et al. "A modulation reconfiguration based fault-tolerant control scheme for modular multilevel converters", 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2013, pp. 3251-3255.

[82] R. Picas, J. Zaragoza, J. Pou, S. Ceballos, "Reliable Modular Multilevel Converter Fault Detection With

Redundant Voltage Sensor", IEEE Transactions on Power Electronics, vol. 32, no. 1, pp. 39-51, Jan. 2017.

[83] S. Shao, A. J. Watson, C. J. Clare, W. P. Wheeler, "Robustness Analysis and Experimental Validation of a Fault Detection and Isolation Method for the Modular Multilevel Converter", IEEE Transactions on Power Electronics, vol. 31, no. 5, pp. 3794-3805, May 2016.

[84] Q. Yang, J. Qin, M. Saeedifard, "SubModule failure detection methods for the modular multilevel converter", 2015 IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, 2015, pp. 3331-3337.

[85] I. A. Gowaid, "A Low-Loss Hybrid Bypass for DC Fault Protection of Modular Multilevel Converters", IEEE Transactions on Power Delivery, vol. 32, no. 2, pp. 599-608, April 2017.

[86] F. Zhao, G. Xiao, D. Yang, M. Liu, X. Han, B. Liu, "A novel T-type half-bridge cell for modular multilevel converter with DC fault blocking capability", 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-6.

[87] J. Mei et al., "Balancing Control Schemes for Modular Multilevel Converters Using Virtual Loop Mapping With Fault Tolerance Capabilities", in IEEE Transactions on Industrial Electronics, vol. 63, no. 1, pp. 38-48, Jan. 2016.

[88] W. Leterme, J. Beerten, D. Van Hertem, "Equivalent circuit for half-bridge MMC dc fault current contribution", 2016 IEEE International Energy Conference (ENERGYCON), Leuven, 2016, pp. 1-6.

[89] H. Xing, Z. Jianzhong, X. Shuai, H. Jun, "Extended state observer based fault detection and location method for modular multilevel converters", IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 2166-2171.

[90] A. Zapico, M. Lopez, A. Rodriguez, F. Briz, "Fault tolerant cell design for MMC-based multiport power converters", 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-8.

[91] S. Haghnazari, H. Vahedi, R. M. Zolghadri, "Fault tolerant operation strategy design for modular multilevel converters", IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 2172-2176.

[92] R. Lizana, A. Dekka, S. Rivera, B. Wu, "Modular Multilevel Converter based on 5-level submodule with DC fault blocking capability", IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 3482-3487.

[93] X. Yu, Y. Wei, Q. Jiang, "New submodule circuits for modular multilevel current source converters with DC fault ride through capability", 2016 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, 2016, pp. 1468-1474.

[94] X. Yang, et al, "Reverse blocking sub-module based modular multilevel converter with DC fault ride-through capability", 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, 2016, pp. 1-7.

[95] L. Cúnico, Y. Novaes, S. Oliveira, "Modelagem e Controle de Corrente do Conversor Modular Multinível (M2LC)". XIX Congresso Brasileiro de Automática, CBA 2012. ISBN, 978-85-8001-069-5. 2012.

[96] P. Asimakopoulos, "Design and Control of Modular Multilevel Converter in an Active Front End Application", doctoral thesis, Chalmers University Of Technology, 2013.

[97] K. Ilves, S. Norrga, L. Harnefors, P. H. Nee, "On Energy Storage Requirements in Modular Multilevel Converters", IEEE Transactions on Power Electronics, vol. 29, no. 1, pp. 77-88, Jan. 2014.

[98] H. Fujita, S. Tominaga, H. Akagi, "Analysis and design of a DC voltage-controlled static VAr compensator using quad-series voltage-source inverters", IEEE Transactions on Industry Applications, vol. 32, no. 4, pp. 970-978, Jul/Aug 1996.

[99] A. Dekka, B. Wu, R. N. Zargari, L. R. Fuentes, "A Space-Vector PWM-Based Voltage-Balancing Approach With Reduced Current Sensors for Modular Multilevel Converter", IEEE Transactions on Industrial Electronics, vol. 63, pp. 2734–2745, may 2016.

[100] R. Marquardt, "Modular Multilevel Converter, An universal concept for HVDC-Networks and extended DC-Bus-applications", The 2010 International Power Electronics Conference - ECCE ASIA, Sapporo, 2010, pp. 502-507.

[101] Y. Deng, Y. Wang, H. K. Teo, G. R. Harley, "Space vector modulation method for modular multilevel converters", in IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society, pp. 4715–4721, Oct 2014.

[102] B. F. Grigoletto, M. Stefanello, S. G. da Silva, H. Pinheiro, "Space vector pulse width modulation for modular multilevel converters", in IECON 2016 - 42th Annual Conference on IEEE Industrial Electronics Society, pp. 388–393, Oct 2016.

[103] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, W. Li, "Improved nearest-level modulation for a modular multilevel converter with a lower submodule number", IEEE

Transactions on Power Electronics, vol. 31, pp. 5369-5377, Aug 2016.

[104] K. Ilves, A. Antonopoulos, S. Norrga, P. H. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency", IEEE Transactions on Power Electronics, vol. 27, pp. 3482–3494, Aug 2012.

[105] N. Ahmed, A. Massoud, "A Matlab/Simulink model for capacitor voltages balancing in modular multilevel converters", 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, 2016, pp. 1-6.

[106] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, G. V. Agelidis, "Comparison of phase-shifted and level-shifted PWM in the modular multilevel converter", in 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA), pp. 3764–3770, May 2014.

[107] A. Hassanpoor, S. Norrga, P. H. Nee, L. Angquist, "Evaluation of different carrier-based PWM methods for modular multilevel converters for hvdc application", in IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society, pp. 388–393, Oct 2012.

[108] D.-W. Kang, W.-K. Lee, D.-S. Hyun, "CarrierRotation strategy for voltage balancing in flying capacitor multilevel inverter", IEE Proc.Electric Power Appl., vol. 151, no. 2, pp. 239–248, 2004.

[109] G. Konstantinou, V. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques", in Proc. IEEE Conf. Ind. Electron. Appl., 2009, pp. 3399-3404.

[110] B.-S. Jin, W. Kyo Lee, T.-J. Kim, D.-W. Kang, D.-S. Hyun, "A study on the multi-carrier PWM methods for voltage balancing of flying capacitor in the flying capacitormulti-level inverter", in Proc. Conf. IEEE Ind. Electron. Soc., 2005, p. 6.

[111] B. Çiftçi, F. Ertürk, M. A. Hava, "Selection of suitable carrier-based PWM method for Modular Multilevel Converter", 2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - E CCE ASIA), Hiroshima, 2014, pp. 3734-3741.

[112] F. D. Baú, S. G. da Silva, H. Pinheiro, B. F. Grigoletto, "PD modulation strategy for modular multilevel converters", 2016 12th IEEE International Conference on Industry Applications (INDUSCON), Curitiba, 2016, pp. 1-6.

[113] G. Konstantinou, V. Agelidis, "Performance evaluation of half -bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques", in Proc. IEEE Conf. Ind. Electron. Appl., 2009, pp. 3399–3404

[114] A. Hassanpoor, S. Norrga, H. Nee, L. Angquist, "Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application", in Proc. Conf. IEEE Ind. Electron. Soc., 2012, pp. 388–393.

[115] S. Rohner, S. Bernet, M. Hiller, R. Sommer, "Modulation, losses, and semiconductor requirements of modular multilevel converters", IEEE Transactions on Industrial Electronics, vol. 57, pp. 2633–2642, A ug 2010.

[116] Z. Li, P. Wang, H. Zhu, Z. Chu, Y. Li, "An improved pulse width modulation method for chopper-cell-based modular multilevel converters", IEEE Transactions on Power Electronics, vol. 27, pp. 3472–3481, Aug 2012.

[117] K. Wang, Y. Li, Z. Zheng, L. Xu, "Voltage balancing and fluctuationsuppression methods of floating capacitors in a new modular multilevel converter", IEEE Transactions on Industrial Electronics, vol. 60, pp. 1943–1954, May 2013.

[118] Q. Jiangchao, M. Saeedifard, "Predictive Control of a Modular Multilevel Converter for a Back-to-Back HVDC System", Power Delivery, IEEE Transactions on, vol.27, no.3, pp.1538,1547, July 2012.

[119] L. Binbin, Y. Rongfeng, X. Dandan, W. Gaolin, W. Wei, X. Dianguo, "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters", Power Electronics, IEEE Transactions on, vol.30, no.1, pp.297,310, Jan. 2015.

[120] D. Sixing, L. Jinjun, L. Teng, "Modulation and ClosedLoop-Based DC Capacitor Voltage Control for MMC With Fundamental Switching Frequency", Power Electronics, IEEE Transactions on, vol.30, no.1, pp.327,338, Jan. 2015.

[121] S. Ke, Z. Dan, M. Jun, M. L. Tolbert, W. Jianze, B. Mingfei, J. Yanchao, C. Xingguo, "Elimination of Harmonics in a Modular Multilevel Converter Using Particle Swarm Optimization-Based Staircase Modulation Strategy", Industrial Electronics, IEEE Transactions on, vol.61, no.10, pp.5311,5322, Oct. 2014.

[122] T. S. Gum, L. Hee-Jin, S. Nam Tae, C. Yong-Ho, L. Uk-Hwa, B. Seung-Taek, H. Kyeon, P. Jung-Wook, "Design and Control of a Modular Multilevel HVDC Converter With Redundant Power Modules for Noninterruptible Energy Transfer", Power Delivery, IEEE Transactions on, vol.27, no.3, pp.1611,1619, July 2012.

[123] M. Jun, S. Ke, X. Bailu, M. L. Tolbert, Z. Jianyong, "A New Selective Loop Bias Mapping Phase Disposition PWM With Dynamic Voltage Balance Capability for Modular Multilevel Converter", Industrial Electronics, IEEE Transactions on, vol.61, no.2, pp.798,807, Feb. 2014.

[124] L. Binbin, Y. Rongfeng, X. Dandan, W. Gaolin, W. Wei, X. Dianguo, "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters", Power Electronics, IEEE Transactions on, vol.30, no.1, pp.297,310, Jan. 2015.

[125] W. Kui, L. Yongdong, Z. Zedong, X. Lie, "Voltage Balancing and Fluctuation-Suppression Methods of Floating Capacitors in a New Modular Multilevel Converter", Industrial Electronics, IEEE Transactions on, vol.60, no.5, pp.1943,1954, May 2013.

[126] Z. Yuebin, J. Daozhuo, H. Pengfei, G. Jie, L. Yiqiao, L. Zhiyong, "A Prototype of Modular Multilevel Converters", Power Electronics, IEEE Transactions on, vol.29, no.7, pp.3267,3278, July 2014.

BIOGRAPHIES

Vinícius has graduated in Electrical Engineering from the Federal Institute of Bahia (IFBA) and is a master's student in Electrical Engineering at CEFET/MG in partnership with UFSJ, developing researches in the segment of Modular Multilevel Converters in the area of Concentration of Systems Analysis and Modeling. He is currently a professor in the Department of Control and Automation Engineering at the Federal University of Ouro Preto where teaches subjects related to analog electronics, power electronics and general electrotechnology. Has experience in the field of Power Electronics (with emphasis on Choppers and Multilevel Converters), Industrial Automation, Electrical Circuits, Digital and Analog Electronics.

Alex Sander holds a degree in Electrical Engineering with an emphasis in Electronics in 1993, a Master's degree in 1996 and a PhD in 2009 in Electrical Engineering focusing on Industrial Electronics, Systems and Electronic Controls and Power Electronics by the Federal University of Minas Gerais. Currently Associate Professor III of the Department of Electrical Engineering of the Federal Center of Technological Education of Minas Gerais (CEFET/MG) where he works in Industrial Electronics and mainly works on the following topics: controlled rectifiers and frequency inverters, high power static converters, harmonics and multilevel modulation.

Marcelo obtained a degree (1994), a master's degree (1997) and a doctorate (2011) in Electrical Engineering from the Federal University of Minas Gerais. He is currently a professor of higher education at the Federal Center for Technological Education of Minas Gerais (CEFET-MG). Its areas of operation include electrical machines, electric drives, static converters and industrial applications.