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Implementation of Ternary ALU using Verilog

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Abstract - *The ternary logic is an alternative to binary logic as it is simpler and more energy efficient because the gate count, memory requirement will be reduced and the speed increases by using ternary logic. It reduces number of computation steps compared to existing Boolean algebra. So, here we have designed TALU and results are compared with the binary ALU using verilog as logic simulator and circuits functionality is tested with Xilinx 13.2i*

Key Words: Ternary logic, Verilog, computation steps, TALU, Gate count, xilinx 13.2i, logic simulator.

1. INTRODUCTION

Alexander [1964] showed that natural base (e ≈ 2.71828) is the most efficient radix for implementation of switching circuits. It seems that most efficient radix for the implementation of digital system is 3 than 2. Ternary logic system, meaning that it has 3 valued switching.

1.1 Ternary Logic

Ternary (3-Valued) logic is operating at 3 switching levels, and it is one of logic in Multivalued logic. The switching levels of ternary logic are denoted by X may assuming either X^0,X^Z,X^1 where 0,Z,1 signifies logic (voltage) levels per ,'0' as low voltage level corresponding to low level logic (logic-0),'Z' corresponding to medium level logic (logic-Z as high impedance also called meta stable state) and ,'1' corresponding to high/maximum level logic (logic-1).

1.2 Advantages

Ternary algebra is an evident advantage of a ternary representation over than binary is economy of digits. To represent a number in binary system, one needs 62.5% more digits than that of ternary and memory of circuit designing is less than binary.

- The main advantage of ternary logic is that it reduces the number of required computation steps for developing digital design.
- Furthermore memory, control unit, and processor can be carried out faster if the ternary logic is easily employed and memory utilization also less than binary

For Example: To represent a 20-digit decimal number one requires 40 ternary digits instead of 65 binary digits.

2. PROPOSED DESIGN

All combinational circuits required to build ALU are taken from previous design [1].all ternary logic gates are implemented using behavioral modelling in verilog.

Table -1:Utilization of TALU

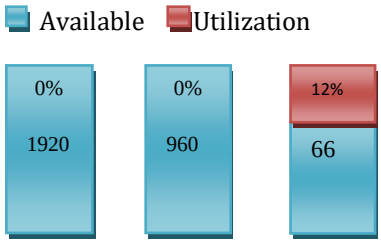
Logic utilization	Used	Available	Utilization
Number of input LUTs	3	1920	0%
Number of occupied Slices	2	960	0%
Number of bonded IOBs	8	66	12%
Delay	6.125ns	8.280ns	
Delay for Logic	5.165ns	6.389ns	84.3%
Delay for Route	0.960ns	1.891ns	15.7%
Total Memory usage	343548KB		

Ternary decoder and ternary 3 x1 multiplexer are basic building blocks for this design. Design process involves the following steps

1. Construct truth table ternary number system for any combinational circuit

2. Simplication with k-map method

3. Implementing simplified expression in terms of 3 x 1 multiplexers.



3 LUTs	2 Slices	8 IOBs	6.389ns Delay	343548KB Total Memory Usage

Graph -1: Utilization of reliable TALU

Ternary ALU inputs are two 1'bit inputs, carry in, borrow in multiple logical cascading inputs and selection lines. Outputs are y, carry, and borrow.

For either sum or difference or multiplication product or logical outputs we have taken single output line 'y'. Based on selection lines different operations are performed

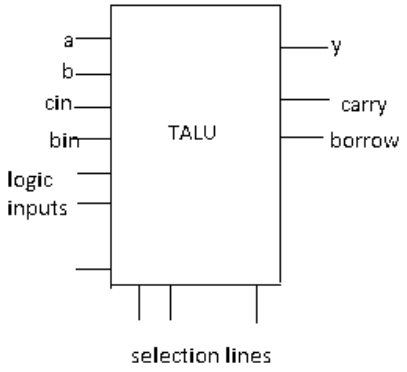


Fig -1: TALU

Here calculating device utilization level in terms of percentage and time taken execution (delay) for the outputs also delay for logic and routing as shown in Table 1. In above table represents details for calculation utilization of reliable TALU and graph1 is shows the representation of utilization of reliable TALU.

The proposal design of Ternary Arithmetic and Logic unit (TALU) is verifying by its functionality using Xilinx ISE 13.2i, ISIM simulator.

3. CONCLUSION

Ternary logic based design are having higher information carrying capacity than binary. Thus, ternary logic gate design technique also provides an excellent speed and power consumption characteristics in data path circuit such as full subtractor and full adder. Ternary logic provides means of increasing data processing capability per unit chip area. The main advantages of ternary logic are that it reduces the number of required computation steps. The number of digits required in a ternary family is $\log_3 2$ times less than that required in binary logic. In this paper, reliable TALU (Ternary Arithmetic Logic Unit) are designed with minimum number of ternary multiplexers.

In these work confirmed to say ternary logic based designs are having less memory, power and delay than binary for addition, subtraction, multiplication and comparisons are should involving number of operations to verifying the functionality. But in binary logic based those operation should perform simply only one operation having more memory and slight greater delay. In this proposed work developed complete ternary algebra basic logic gates, 81X1 multiplexer and also synthesizes delay for logic and routing of TALU, device utilization. Verilog simulator has been used to simulate Ternary logic based Systems which provide enough information to verify functionality and timing specifications.

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