FAULT- TOLERANT FIR FILTER IMPLEMENTATION

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ABSTRACT: This is the matter-of-fact that communication system is never free from noise. Therefore it is a requirement for every communication systems to have suitable means to recognize and correct the errors in the information which is received over communication channels. Digital parallel FIR(Finite Impulse Response) filters are very widely used in DSP application. To get the noise free system, there is a need to implement some techniques to achieve the fault tolerance in parallel filters. In this paper , the idea of implementing FIR Filter with the range of 1 bit to 6-bit Fault tolerance using BCH codes is addressed. This idea is very much effective in fault tolerance as well as comparatively less cost. Both features are evaluated for FPGA implementation.

Keywords: Error Correcting Codes (ECC); Finite Impulse Response (FIR) filter; Very Large Scale Integration (VLSI); HDL; FPGA.

1. INTRODUCTION

The reliability of performance in transmitting the signals is critical as the communication medium or channels are not noise free. The outcome is not so accurate in traditional system . So it create the requirement to design filters to give output accurate in the presence of errors also. Till now many different strategies followed to develop the filters-structures and properties to get a better fault-tolerance.

More complicated or higher level Communication systems incorporate many filters. In those complex type systems, many of them operate like digitally. i.e. by giving the unlike input signal to the same filter. Here, the scheme is used that digital FIR can be fault tolerant by using ECCs. In ECCs, one filter represents a bit. It gives the more competent fault tolerance even when the counting of FIR filters are large in complex communication systems. The whole technique is evaluated through some case studies of digital Finite Impulse Response(FIR)s with unlike inputs(original input with error at different places). Showed outcomes

in these cases are giving effective error-tolerance & low implementing cost.

As moving to complex level of communications systems, the systems comprise more increased counting of elements. In most systems, many elements perform in digital circuits that exhibit the same functioning on the applied different-different signals. Digital filters are most common example of these type elements. The increased counting of blocks in complicated communication systems also exhibits the great reliability challenges. Thus this reliability challenges create the need of error free implementations. Here, in present work, a scheme which uses ECC for error correction has been suggested to protect Digital FIR filters.

Here the scheme of using ECC to protect digital filters is applied. The data (I/O) of filters are numbers instead of bits. Thus this idea provides the fault tolerance as the counting of redundant filters are free from the counting of used digital filters. The concept is first described and then illustrated with case studies. Finally the outcome parameters of the cases are evaluated in terms of error-tolerance & low implemented cost for FPGA implementation.

2. APPROACHES

The figure 1 shows the proposed structure for fault tolerant FIR filter. This figure gives the clear overview of low level overview of proposed fault tolerant FIR filter. FIR filter inputs are mixed with some error bits and fed to the designed fault tolerant FIR filter. Here FIR filter is designed with the help of MATLAB and HDLs. Error detection and correction is done by HDL using BCH coding techniques. The proposed structure gives the error free output and one notification signal which is high when the number of errors are more than the specified criteria.
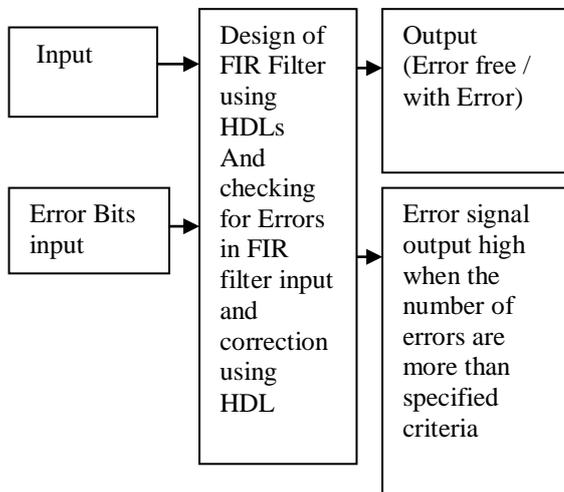
Figure 1. Proposed Structure for Fault tolerant FIR Filter

3. SIMULATION RESULTS

This section shows the various results obtained from the XILINX ISE Tool. The figure 2 shows the RTL view of our designed circuit i.e. Fault tolerant FIR Filter. As shown in the figure there are two inputs named as A , and error . The input A denotes the original message to be filter through the FIR filtration. While error signal are for stimulating the various number of errors.
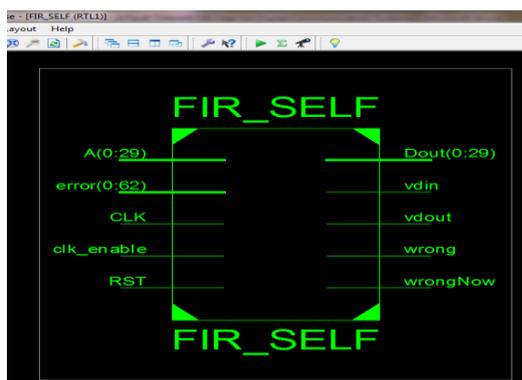

Figure 2: RTL view for Fault Tolerant FIR

The figure 2 shows only the input output ports which can be used as a physical interface for real world implementation.

The figures 3, 4 shows the cumulative result for the fault tolerant fir filter with different input conditions.
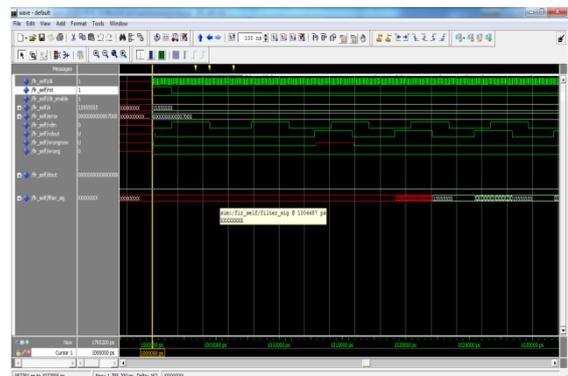
Figure 3: Simulation Result with initial Conditions.

The figure 3 shows the simulation results with initial conditions i.e. RST='1'. For initialization of all the registers, signals into its original states/values.
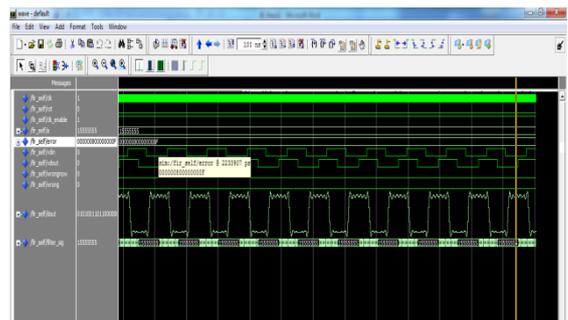
Figure 4: Simulation result for 5 bit error

figure 4 shows the result with stimulation of 5 bit error values through error signal. And we can easily observe that there is not a slight change in the output waveform.

4. CONCLUSION

During present study, some criteria are taken into consideration in BCH decoder designing. The criteria are area of circuit, speed, latency. Present job give emphasis on the decoding algorithm, code design and FPGA-implementation to attain the required parameters like fault tolerance, hardware reconfigurability. Here this undesired hardware area is reduced by using Arithmetic Structure. In this paper efficient coding scheme is used for fault-tolerant FIR Filter. FIR Filters can also be made using different structures i.e. Parallel, Serial but each design has the common feature i.e. the multiplication and shifting process which demands lots of hardware area. So it is a future challenge to reduce the hardware area by using Distributed Arithmetic structure. The

Synthesis has been done by XILINX Synthesis Tool and the simulation has been carried out by Xilinx ISIM and Modelism.

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BIOGRAPHIES

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