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New Approach for PCB Boundary Scan Testing Using Unique TAP

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Abstract - *Traditional test and measurement equipments which rely on connecting external probes are no longer possible given the state of the art of today's shrinking electronics. Since probing is extremely difficult if not impossible, other methods must be used. A novel approach for testing printed circuit boards is presented in this research. The new methodology provides an elegant solution for this problem. The approach is developed based on the IEEE 1149.1 Std for testing and debugging. It defines the architecture for testing modern integrated circuits over printed circuit boards without external probing. PCB compliant with this methodology contains one shared access interface to access testing logic. Chips compliant with this technique contain bypass registers only, whereas the IEEE 1149.1 compliant chips contain four types of registers. The shared access interface which is called test access port (TAP) has a USB port interface. The chips over the PCB are connected with the shared TAP using the star topology. Only one bidirectional data line has been used to connect each IC. The TAP is controlled by an open source software developed using Arduino application. The software is able to access the ICs logic and for automatic test pattern generation. It handled the details of the logic such that users can focus on the actual testing without having to worry about or having a need to know the implementation details at chip level. The logic circuit of this design is simulated and the hardware prototype is built successfully. The new design has the distinct feature of being less complex, less expensive and more reliable than IEEE 1149.1 Std. Also it has the new feature of being totally driven by an open source and user friendly software.*

Key Words: IEEE 1149.1, Test Access Port TAP, System On Chips SOC, JTAG, multi-chip modules MCMs, Scan Test, IC Testing.

1. INTRODUCTION

The incredible shrinking of printed circuit boards and systems on chips (SOCs) has led to miniaturization results in loss of test access. Also, the ever-expanding number chips and the increasing complexity of integration at chip level has complicated the test controllability. Moreover, cost will increase by a factor of ten as fault-finding moves from one level of complexity to the next. This has caused reduced profit margins, delayed product introduction, and dissatisfied customers [1].

The conventional methods of testing, such as functional test methods (such as the edge–connector test) were imposed by hard-wired copper interconnects and, as a result, it encounters many critical limitations and also impedes the advance of future testing device. It is based on board function rather than structure.

Primarily, the test generation was manual, and the test access was limited to primary inputs and outputs only. The in-circuit test (ICT) method, which is based on the board structure, was also limited by superfine chip packages, double-sided boards, conformal coating, multi-chip modules (MCMs), and chip complexity. Also, it requires expensive testers and fixtures. In such tests, chip functions can be ignored for shorts testing and must be considered for continuity tests [2, 3].

The performance of testers depends basically on the device properties. To enhance tester performance, the efforts should be focused on improving testing speed through decreasing the interconnections between the tester and the device under test. The complexity of the interconnections between the DUT and the tester became one of the major showstoppers in evaluating the health of DUT [4].

Embedding memory and microcontroller units inside the testers also causes many disadvantages. It increases cost, size, and complexity of the tester. On the other hand, decreasing memory size leads to a proportional decrease in the number of devices that can be diagnosed by the tester. Versatile and multi-faceted testers can be manufactured, but the cost will be more expensive. The rapid growth in the complexity of circuits requires a parallel and continuous development in tester microcontrollers, creating a difficult challenge [5-7].

To surpass these constraints, we introduce a new test methodology based on JTAG and IEEE 1149.1 Std. The new methodology involves developing one shared test access port (TAP) over the entire PCB and a re-design of the on-chip DFT circuitry. Such improvements will lead to a significant reduction in the complexity of testing nets, resources, and pins connections.

The new methodology uses star test topology for connecting multiple devices; such topology provides a means of arbitrarily observing test results and source test stimulus. The model requires minimal on chip/board resources (pins/nets). Also, it is not limited by the chip function or complexity. Moreover, test access is not limited by the physical factors of the board and the test generation is highly automated.

In the new methodology, only one bidirectional data line is utilized in order to carry data between the TAP and each device under test. Therefore, one test access pin is required for each DUT. The new architecture will help in reducing any resultant yield loss due to the proven contact problems.

Many features and advantages are achieved by using the new methodology. One such feature is the considerable cost reduction due to utilizing only one TAP to interface all on-board devices, and also due to the high simplification in boundary scan circuits. Further advantage is that each DUT is diagnosed separately without any correlation with other DUTs. Moreover, unlike the IEEE 1149.1 Std, there is no need to embed instructions, identifications, or bypass units inside integrated circuits.

The conventional testing methods for printed circuit boards (PCBs) and integrated circuits (ICs) are suffering from so many deficiencies. The incredible shrinking and complexity in the new PCBs and ICs made the traditional testing methods unreliable or even inapplicable.

In 1985, new attempts emerged. Joint Test Action Group (JTAG) developed a creative method for testing finished PCBs after manufacturing. In 1990, the institute of electrical and electronics engineers (IEEE) codified the JTAG method as a standard with the designation IEEE Std. 1149.1-1990 entitled “Standard Test Access Port and Boundary-Scan Architecture”.

Although IEEE1149.1 standard facilitates testing process, it is still suffering from the following disadvantages and deficiencies:

1-It requires adding extra circuitry to the ICs and PCs. Such addition caused an exaggerated complexity and cost.

2-It uses the cascaded (ring) topology to connect ICs on-board, this topology proved its failure because any IC failure will cause halting the whole testing process.

3-The standard requires four test signals to interface each IC, and that will increase traces interference over the PCB.

4-The driving application or software is not open source.

In this paper we present a new testing system based on sharing one test port for all ICs on-board. The system is less complex and more reliable. It utilizes the star topology to connect the ICs on-board, so any IC failure will not halt the testing. Also, the system requires only one test signal to interface the IC, and that will reduce any expected interference between traces. Further advantage, the driving software for the testing process is open source and user defined. After a detailed verification, the new system is more efficient, reliable and applicable than conventional methods.

2. The System Architecture

As previously mentioned, the new methodology uses star test topology (STT) to connect all the peripherals. Each DUT is connected to the central test access port TAP using point-to-point connections. The TAP acts as a hub and the DUTs are considered as clients. The connection does not necessarily have to resemble a star in order to be classified as a star topology, but all of the DUTs access pins must be connected to one shared TAP. All traffic that traverses the testing network has to pass through this TAP. It selects the targeted DUT to be tested. It also forwards the test pattern and returns the corresponding test data output (TDO) pattern. To select a different DUT, the computer transmits a test reset signal (TRST) followed by a new data packet. The star topology is an easier topology to design and implement. The most important advantage of STT is that it responds immediately to any node failure. Only one DUT will be affected if an error occurs, while the entire circuit remains running. Because of this, diagnosing a single device for an error or defect is supposed to be easy.

In STT, the computer broadcasts test-data input (TDI) packets to several DUTs via TAP, and the computer can easily identify any failed DUT. Because of its simplicity in testability, managing the STT using connected DUTs is considered a trivially simple. Moreover, by STT, failures can be located easily by a logical analysis and, as a result, it can be simply diagnosed.

The new system architecture is illustrated in Figure 3 1; it has TAP acting as main hub and the DUTs represent the nodes. Each DUT exploits only one pin to interface the TAP. Therefore, test signals are directly transferred from TAP to the DUT without passing through other devices. To prevent drive conflicts among the DUTs, the TAP controller handles a direct addressing method.

When a data packet is received by the TAP input line, the port reads the address information in the packet header to determine its ultimate destination. Then, using serial to parallel shift registers and demultiplexer circuits, it forwards the test packet to the next DUT on its journey; therefore, TAP performs the "data traffic control" function on the circuit.

Each DUT has its own test hub TH. It is the circuit that interfaces multiple inputs and outputs of the DUT and makes them act as a single network segment. The serial signal that is introduced at the input of the TH appears at the parallel outputs of the TH. It is specialized hardware that forwards data packets between TAP and DUT inputs and vice versa.

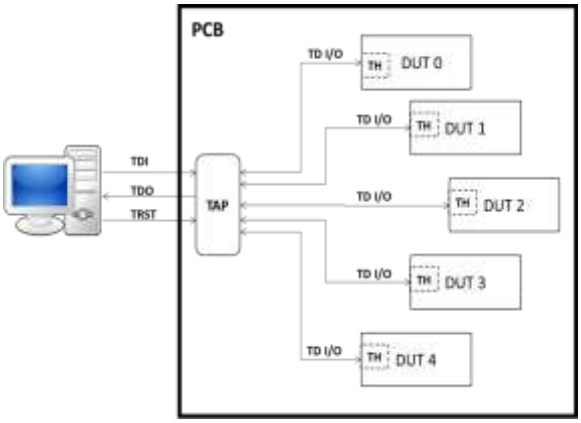

Figure 1: System Architecture

3. Boundary Scan Circuit

The boundary-scan circuit is the IC core-surrounding circuit that is responsible for applying the received test pattern and capturing the response signal. It involves shift registers, buffers, and counters. The circuit exploits only one IN/OUT pin of the IC to receive TDI and broadcast TDO. Also, unlike IEEE 1149.1-compliant ICs, it does not involve any memory cells. Moreover, the circuit extracts the intended testing instructions from the received code; hence, there is no need to embed any instruction registers in the IC. Figure 3 26 depicts an IC core surrounded by a boundary-scan circuit. It is significant that the TDI drive and TDO transmitter have a mutual relation. The TDI driver stimulates the TDO counter to open the capturing port and start transmitting the TDO signal. Two buffers are used to control data traffic via internal connections and to avoid any TDI/TDO interference. The used buffers also represent high-impedance diodes for any unwanted signals.

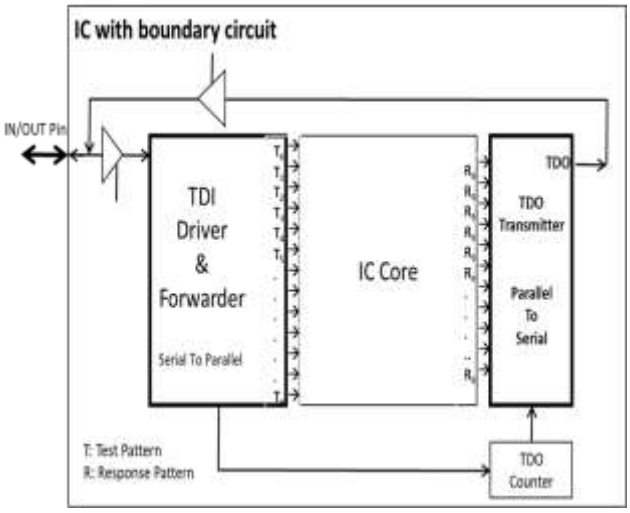

Figure 2 : IC with a boundary scan circuit

3. Computer Interfacing

Interfacing the testing system has been performed using an Arduino Uno board via the universal serial bus (USB) port. A driving program is developed using the Arduino integrated development environment which is based on JAVA. Figure illustrates the combination diagram between the PCB under test and computer using Arduino board.

Computer interfacing is one of the major benefits of our design. It exempts the testing system from using a test pattern generator or even automated test equipment. Moreover, the driving software can be open-source and not a built-in application; engineers can customize their own tests. Furthermore, interfacing via USB gives more impact for the test; it increases patterns transfer speed up to its highest values.

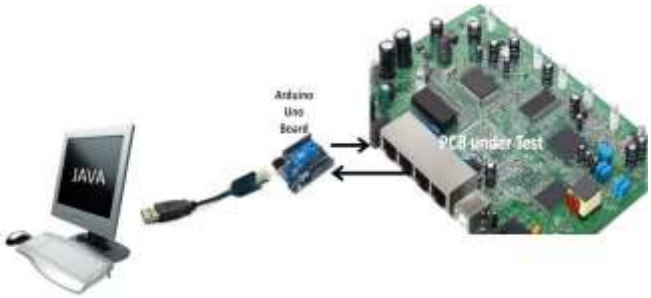

Figure 3: Combination diagram for Arduino interfacing

4. CONCLUSION

The proposed testing circuit was simulated successfully by NI Multisim software. It smoothly transmitted test patterns and received the corresponding response patterns. The circuit succeeded in testing four ICs accurately. Also, the hardware was built and ran successfully. It performed a precise testing for several ICs.

The driving Arduino source code was written, compiled, and loaded successfully. It prompts the user to enter the initial values and accordingly drives the TAP interface. All the system parts successfully integrated together to perform an advanced and sophisticated test.

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BIOGRAPHIE

Salim Jayousi is full time assistant, Completed his Ph.D in University Malaysia Sarawak under the supervision of Prof. Mohammad Saufi who has a lot of contributions in electronic engineering fields all over the world. Salim Jayousi is interested in improving IEEE 1149.1 Testing Methodology.