International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 01 | Jan 2019 www.irjet.net p-ISSN: 2395-0072

A NOVEL SOFT SWITCHING PWM DC-DC CONVERTER

A.E. Anyalebechi

Nnamdi Azikiwe University Awka, Anambra State, Nigeria

Abstract:- *This paper presents the design of a soft-switching boost dc-dc converter. Passive soft-switching is employed due to its advantages over the active soft-switching and its ability to reduce switching losses. A Laplace transform-based analysis of the converter circuit is carried out to obtain design information. Experimental results obtained from the prototype agree closely with the predicted results and demonstrate the feasibility of the system.*

Key words: *Boost Converter, Active, Passive, Laplace transform, Pulse width modulation.*

1. INTRODUCTION

Semiconductor device switching at high frequency is a major contributor to power loss in converters. Switching devices absorb power when they turn on or off if they go through a transition when both voltage and current are non-zero. As the switching frequency increases, these transitions occur more often and the power loss in the device increases. High switching frequencies are otherwise desirable because of the reduced size of filter components and transformers which reduce the size and weight of the converter circuits.

In resonant switching circuits, switching takes place when the switching device voltage and/or current are/is zero, thus avoiding simultaneous transitions of voltage and current and thereby eliminating switching losses. This type of switching is called "soft" switching. Resonant converters include resonant switch-mode converters, load resonant converters, and resonant dc link converters [1].
A successful soft-switching scheme should be able to reduce the switching losses, diode reverse recovery losses, and switching voltage and current stresses on converter components. Any of the two main soft switching approaches which include the zero-current switching and the zero-voltage switching may be employed depending on the semiconductor device technology that will be used. For example, MOSFETs present better performance under zero-voltage switching (ZVS). This is because under zero-current switching the capacitive turn-on losses increase the switching losses and the electromagnetic interference (EMI). On the other hand, insulated gate bipolar transistor (IGBTs) and bipolar junction transistors (BJTs) present better results under zero-current switching (ZCS) which can avoid the turn-off losses caused by the tail current [2].

Furthermore, the last twenty years have witnessed an intensive research with the sole aim of achieving lossless switching of semiconductor devices. Lossless switching increases circuit efficiency and makes high frequency operation possible thereby reducing the size and weight of circuit components. Several dc-dc converter configurations aimed at achieving a percentage degree of this goal have been proposed [3,4,5,6,7,8,9]. Each of these proposed circuit topologies has at least one of the following limitations:

(a) Too many circuit components, thus degrading circuit reliability,
(b) High current/voltage stresses on the circuit components,
(c) Complex control circuitry which may include switching current/voltage level detection circuits,
(d) Parasitic capacitor turn-on loss of some of the circuit switches,
(e) Limitation of the output voltage control range to allow for switching transients.

In this paper, a detailed study of the single stage dc-dc employing a versatile and efficient soft-switching circuit cell is presented. In the presented converter, the turn-off and the turn-on of the main active switch and the corresponding freewheeling diode take place under zero-current and/or zero-voltage switching. Also, the turn-on and the turn-off of the circuit cell semiconductor devices take place under zero-current and/or zero-voltage switching.

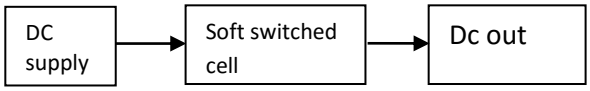


Fig. (1) Block diagram of conventional soft-switched dc-dc converter.

A lossless switching is achieved under the above scheme while the voltage and current stresses are drastically reduced to the barest minimum through clamping techniques. Figure 1 shows a schematic block diagram of a conventional dc-dc converter. In this paper, the performance analysis and design of the soft-switched dc-dc converter is given. Predicted results from the analysis are verified with experimental prototype.

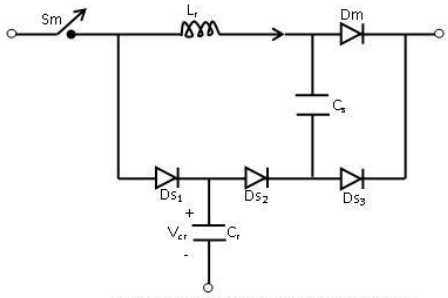
2. ACTIVE/PASSIVE SOFT SWITCHING

Higher switching frequencies allow reduction of the magnetic component sizes with pulse width modulated (PWM) switching converters. Unfortunately, increased switching frequencies cause higher switching losses and greater electro-magnetic interference (EMI). The switching loss mechanisms include the current and voltage overlap loss during the switching interval and the capacitance loss during turn-on. The diode reverse recovery also causes an additional conduction loss and further contributes to the current and voltage overlap loss. Soft switched pulse width modulated converters can either be passively soft switched or actively soft switched. Active or passive soft-switching methods have been used to reduce these switching losses.

Recently, passive soft switching has received renewed inspection as a better alternative to active methods. Passive methods do not require an extra switch or additional control circuitry. They are less expensive, have higher reliability and have been reported to achieve higher performance/price ratios than active methods [10, 11]. For PWM converters, passive soft switching reduces switching losses by lowering the active switch's di/dt and dv/dt to achieve zero-current turn-on and zero-voltage turn off. Furthermore, by controlling the di/dt of the active switch, the reverse recovery currents of the diodes are also controlled. The only loss mechanism not recovered with the passive techniques is the energy in the internal capacitance of the switch. However, this loss is much smaller than the other switching losses and may be smaller than the loss incurred by using an auxiliary switch in an active method [10, 11]. Historically, passive soft switching techniques were used to reduce spikes in the switching circuits and were lossy by dissipating the recovered switching energy in resistors [12]. But more recently, many lossless and partially lossless techniques have been proposed [10, 13].

The two necessary components that must be added to the circuit to achieve passive zero-current turn on and zero-voltage turn off are a small inductor L_r and a capacitor C_r. The inductor provides zero-current turn on of the active switch and limits the recovery current of the diodes while the capacitor provides zero-voltage turn off of the active switch. However, the topological rules that describe where these components must be placed in the circuit have not been proposed in the literature. Typically the inductor and capacitor have been placed in series and parallel respectively with the active switch. But many other locations are possible and can lower the component count and reduce switch stress. Also additional circuitry accompanying the capacitor and inductor is used to recover their energy to either the load or the input. There are many different proposed circuits to accomplish this. Furthermore, circuitry cells can be constructed that simplify the creation of new soft switching circuits.

The description and analysis of the proposed soft-switched converter, implemented with boost converter is hereby presented. A model of the circuit cell of passively soft-switched pulse width modulated converters can be represented as follows:



(2) Fig (3.1) passively soft switching circuit cell

3. BOOST CONVERTER CONFIGURATIONS

There are different possible configurations of the passively soft switching boost converter but the analysis given below is with reference to the configuration shown below:

Definitions: $Z_{os} = W_{os}L_r$; $W^2_{os} = 1$

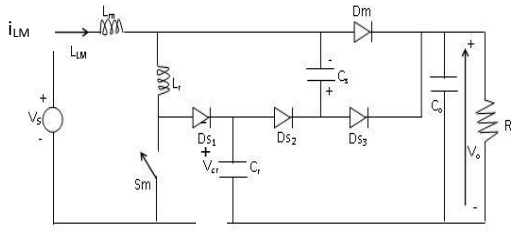


Fig (3.2) Configuration A

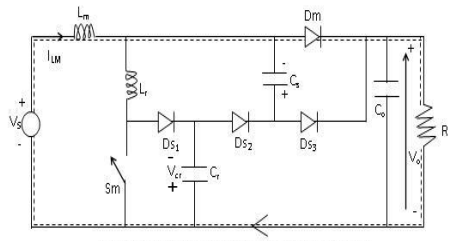
$/L_rC_s$;

$Z_{oT} = W_{oT}L_r$; $W^2_{oT} = 1/L_rC_T$; $W^2_o = 1/L_rC_r$; $C_T = \frac{C_rC_s}{C_r+C_s}$

The main inductor current at time t_0 has a value of I_1 whereas the resonant capacitor voltage (v_{cr}) has an initial value at time t_0 of V_0. Also the resonant inductor current I_{lr} and the snubber capacitor voltage v_{cs} at time t_0 have values of zero each:

$i_{lm}(t_0) = I_1$; $vcr(t_0) = V_0$ ..... (3.1)

$v_{cs}(t_0) = 0$; $ilr(t_0) = 0$ .....(3.2)



(4) Fig (3.3a) Operation at time $t = t_0$ (i.e. before stage 1)

Stage 1: $t_0 \le t \le t_1$

This stage lasts between time t_0 and t_1. Here S_M is turned on at zero current switching, the output voltage V_0 is across the resonant inductor L_r and the resonant inductor current i_{lr} rises to I_1, after D_m recovers from conduction. That is,

$I_{lm}(t_1) = I_1$; $V_{cr}(t_1) = V_0$ ..... (3.3)

$V_{cs}(t_1) = 0$; $i_{lr}(t_1) = I_1$ ..... (3.4)

It is worthy to note that here S_m turns on at zero-current and D_m turns off at zero-voltage because of the resonant inductor connected in series to S_m and snubber capacitor C_s connected across D_m. The circuit operation under this stage is shown below;

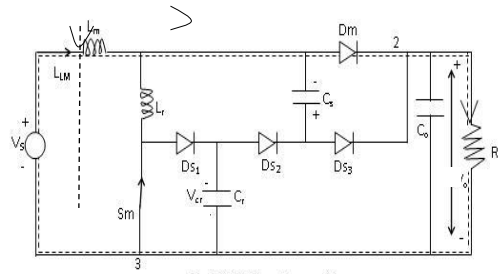


Fig (3.3b) Stage 1 operation

$$-V_{32} = \frac{L_r di_{Lr}}{dt} = V_0$$

$$\therefore i_{Lr} = \frac{1}{L_r}\int_{t_o}^{t} -V_{32}dt = \frac{-V_{32}}{L_r}(t - t_0)$$

At the end of mode 1 when time becomes t_1 the resonant inductor current is I_l. That is,

$$I_1 = -\frac{V_{32}}{L_r}(t_1 - t_o) = \frac{V_o}{L_r}(t_1 - t_o) \quad \ldots\ldots (3.5)$$

Hence, at $t = t_1$, when $i_{Lr} = I_1$ mode 1 stops, therefore, the interval of mode 1 becomes

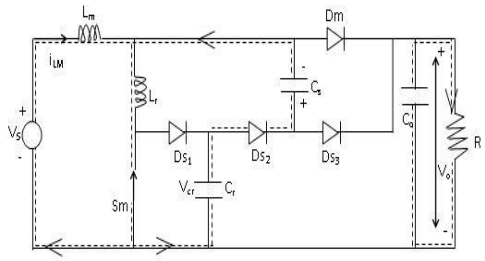
$$t_1 - t_o = -\frac{L_r I_1}{V_{32}} = \frac{L_r I_1}{V_o} \quad \ldots\ldots (3.6)$$

STAGE 2; $t_1 \le t \le t_2$

This stage has a time gap between t_1 and t_2. Due to the resonant capacitor, oscillation will take place in the loop $C_r \rightarrow D_{s2} \rightarrow C_s \rightarrow L_r \rightarrow S_m$ as depicted in the figure below. This oscillation will continue until the resonant capacitor voltage discharges to zero (i.e. $V_{cr} = 0$) and its voltage is clamped to zero by D_{s1} conducting. At the end of stage two we have,

$$V_{cr}(t_2) = 0;\ V_{cs}(t_2) = -V_{cs2} \ldots\ldots (3.7)$$

$$i_{Lr}(t_2) = I_1 + i_{cs2} \ldots\ldots\ldots (3.8)$$



(6) c) Stage 2 operation

From the circuit of second stage of operation, three equations can be derived with regard to resonant capacitor voltage, resonant inductor current and snubber capacitor voltage as follows;

$$Cr\frac{dV_{cr}}{dt} = i_{Lr} - I_1$$

$$\Rightarrow Cr\left[SV_{cr(s)} - V_{32}\right] = I_{Lr(s)} - I_{1/S}$$

$$\therefore V_{cr(s)} = \frac{I_{Lr(s)} - I_{1/S} + V_{32}Cr}{SCr} \ldots\ldots (3.9)$$

Also,

$V_{L_r} = L_r\frac{di_{L_r}}{dt} = -V_{C_s}$

$$\therefore Lr\left[SI_{Lr(s)} - I_1\right] = -V_{Cs(s)}$$

$$\therefore I_{Lr(s)} = \frac{-V_{Cs(s)} + LrI_1}{LrS} \ldots\ldots (3.10)$$

Again,

$$C_s\frac{dV_{C_s}}{dt} = i_{Lr} - I_I$$

$$\therefore C_s\left[SV_{cs(s)} - 0\right] = I_{Lr(s)} - I_{1/S}$$

$$\therefore V_{cs(s)} = \frac{I_{Lr(s)} - I_{1/S}}{SC_S} \ldots\ldots (3.11)$$

Putting (3.9) and (3.11) into (3.10), we have after simplification

$$i_{Lr(t)} = I_1 + \frac{V_o}{Z_{oT}} Sin\, W_{oT}(t - t_1) \ldots (3.12)$$

The resonant capacitor voltage can also be derived.

Substituting (3.11) into (3.9), we have after simplification

$$V_{cr(t)} = -V_o\left[Cos\ W_{oT}(t-t_1) + \frac{W_{oS}^2}{W_{oT}^2} - \frac{W_{oS}^2}{W_{oT}^2}\ Cos\ W_{oT}(t-t_1)\right] \ldots . (3.13)$$

Also, from equation (3.10),

$$V_{cr(s)} = L_r I_1 - V_{cs(s)} - SL_r I_{Lr(s)}.$$

Combining this with equation (3.9), we have

$$\frac{I_{Lr(s)}}{SC_r} - \frac{I_I}{S^2C_r} + \frac{V_{32}C_r}{SC_r} = L_r I_I - V_{cs(s)} - SL_r I_{Lr(s)}$$

$$I_{Lr(s)}\left[SL_r + \frac{1}{SC_r}\right] = \frac{I_1}{S^2C_r} + L_r I_1 - V_{cs(s)} - \frac{V_{32}}{S}$$

But from equation (3.11) we have

$$I_{Lr(s)} = SC_s V_{cs(s)} + {}^{I_1}/_{S}$$

Then substituting equation (3.11) we have after simplification

$$V_{cs(t)} = \frac{V_o W_{oS}^2}{W_{oT}^2} - \frac{V_o W_{oS}^2}{W_{oT}^2}\ Cos\ W_{oT}(t-t_I) \ldots \ldots \ldots . . (3.14)$$

STAGE 3; $t_2 \le t \le t_3$

The circuit operation for this stage is shown below;

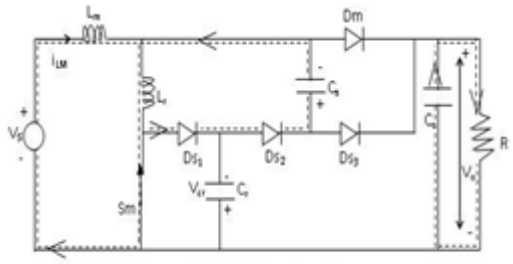


Fig (3.3d) Stage 3 operation

The resonant capacitor voltage is still clamped at zero as a result of D_{s1} and D_{s2} conducting. The resonant inductor current i_{Lr} continues to oscillate about its steady state value in the loop; $L_r \rightarrow D_{sI} \rightarrow D_{s2} \rightarrow C_s \rightarrow L_r$. At the end of stage three, time t , the oscillatory component of the resonant inductor current i_{Lr} dies down [i.e, $i_{Lr}(t_3) = I_2$]. And the operation takes the normal form of S_m conducting and D_m off. Also the snubber capacitor voltage V_{cs} reaches a value of $-V_{cs3}$. That is,

$$V_{cs}(t_3) = -V_{cs3}; V_{cr}(t_3) = 0$$

Initial conditions

$$i_{Lr} = i_{Lr(t_2)}$$

$$V_{cr} = V_{cr(t_2)} = 0$$

$$V_{C_s} = V_{cs(t_2)}$$

Here there are two equations that describe the path of the excess current:

$$\frac{C_s dV_{CS}}{dt} = i_{Lr} - I_1$$

$$\therefore C_s\left[SV_{cs(s)} - V_{cs(t_2)}\right] = i_{Lr(s)} - {}^{I_1}/_{S}$$

$$=> SC_s V_{cs(s)} - C_s V_{cs(t_2)} = I_{Lr(s)} - {}^{I_1}/_{S} \ldots \ldots \ldots (3.15)$$

Also, $L_r \frac{di_{Lr}}{dt} + V_{CS} = 0$

$$=> L_r\left(SI_{Lr(s)} - i_{Lr(t_2)}\right) + V_{cs(s)} = 0$$

$$\therefore V_{cs(s)} = -L_r\left(SI_{Lr(s)} - i_{Lr(t_2)}\right) \ldots (3.16)$$

Substituting (3.16) into (3.15) we have after simplification

$$i_{Lr(t)} = I_1[1 - Cos\ W_{os}(t-t_2)] + i_{Lr(t_2)} Cos\ W_{os}(t-t_2) - \frac{V_{cs(t_2)}}{Z_{os}} Sin\ W_{os}(t-t_2) \ldots \ldots (3.17)$$

Also, from equation (3.15) we have

$$I_{Lr(s)} = SC_s V_{cs(s)} - C_s V_{cs(t_2)} + {}^{I_1}/_{S} \ldots \ldots \ldots (3.18)$$

From equation (3.16) we have

$$I_{Lr(s)} = \frac{L_r i_{Lr}(t_2) - V_{C_s(s)}}{SL_r} \ldots \ldots \ldots (3.19)$$

Combining (3.18) and (3.19) we have after simplification

$$V_{cs(t)} = Z_{os} i_{Lr(t_2)} Sin\ W_{os}(t-t_2) + V_{cs(t_2)} Cos\ W_{os}(t-t_2) - Z_{os} I_1 Sin\ W_{os}(t-t_2) \ldots \ldots . . (3.20)$$

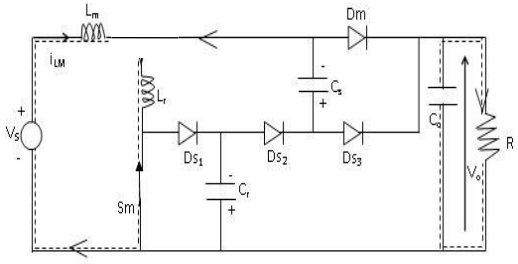
STAGE 4: $t_3 \le t \le t_4$

The resonant inductor current remains constant at a value of I_2 in the loop $V_s \rightarrow L_m \rightarrow L_r \rightarrow S_m \rightarrow V_s$.

That is,

$$i_{LM(t_4)} = I_2; \quad V_{cr(t_4)} = 0; \quad V_{cs(t_4)} = -V_{cs3}$$

The circuit operation for stage four is as shown below;



(8) Fig (3.3e) Stage 4 operation

Initial conditions are,

$$V_{cr} = V_{cr(t_3)} = 0$$

$$i_{Lr} = i_{Lr(t_3)} = I_2$$

$$V_{C_s} = V_{cs(t_3)}$$

Here, only one equation applies,

$$(L_m + L_r)\frac{di_{Lr}}{dt} = V_s$$

$$\therefore i_{Lr} = \frac{1}{(L_m + L_r)}\int_{t_3}^{t} V_s\, dt = \frac{V_s}{(L_m + L_r)}(t - t_3) + I_1$$

This mode ends at t_4 and the resonant inductor current is I_2.

$$\therefore I_2 = \frac{V_s}{(L_m + L_r)}(t_4 - t_3) + I_1$$

This gives the interval of mode 4 as

$$(t_4 - t_3) = \frac{(L_m + L_r)(I_2 - I_1)}{V_s} \quad \ldots (3.21)$$

STAGE 5; $t_4 \le t \le t_5$

At time t_4, the main active switch S_m is opened at zero voltage switching and the resonant capacitor C_r is charged by the current I_2. Stage five ends when D_{s3} is forward biased by taking the loop $V_s \rightarrow L_m \rightarrow C_s \rightarrow D_{s3} \rightarrow V_0 \rightarrow V_s$. Under this condition,

$$V_{cr} - V_{cs} = V_0$$

$$i.e,\ V_{cr} + V_{cs3} = V_0$$

$$V_{cr}(t_5) = V_0 - V_{cs3}$$

$$Since\ V_{cs}(t_5) = -V_{cs3}$$

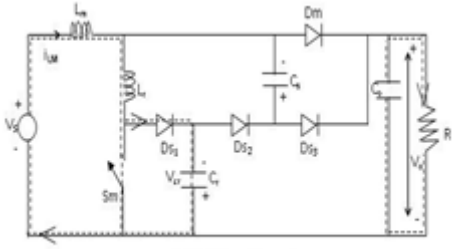


Fig (3.3f) Stage 5 operation

Initial conditions,

$$V_{cr} = V_{cr(t4)} = 0$$

$$V_{C_s} = V_{cs(t4)}$$

$$i_{Lr} = i_{Lr(t4)} = I_2$$

Therefore,

$$Cr\frac{dV_{cr}}{dt} = I_2$$

$$\Rightarrow Cr[SV_{cr(s)} - 0] = I_2/_S$$

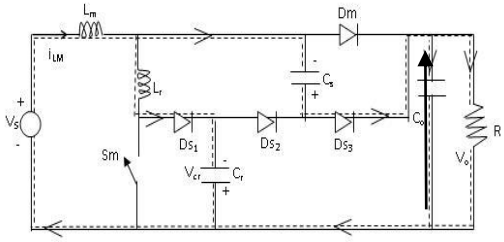
$$\therefore V_{cr(t)} = \frac{-I_2}{C_r}(t - t_4) \quad \ldots\ldots\ldots (3.22)$$

STAGE 6; $t_5 \le t \le t_6$

At t_5 which marks the beginning of this stage the resonant capacitor has charged up to a certain value given by equation (3.22). This causes the resonant inductor current to split into two. One part which tends to discharge C_s flows through $C_s \rightarrow D_{s3} \rightarrow V_0 \rightarrow V_s \rightarrow L_m$, the other part flows through $L_r \rightarrow D_{s1} \rightarrow C_r \rightarrow V_s \rightarrow L_m$ as shown in the circuit below. This continues up to time t_6 when the resonant capacitor voltage becomes V_0 causing D_{s2} to conduct. That is,

$$V_{cr}(t_6) = V_0;\ V_{cs}(t_6) = -V_{cs6}$$

These two voltage values remain V_0 and $-V_{cs6}$ respectively at the end of stage six. it is necessary to note that $-V_{cs6}$ is smaller than $-V_{cs3}$ in magnitude.



(3.33g) Stage 6 operation

At t_5, $V_{cr} + V_{cs} = V_o$ and D_{s3} starts conducting and there are two parallel paths for current.

Initial conditions

$$V_{cr} = V_{cr(t5)}$$

$$V_{C_s} = V_{cs(t5)}$$

$$i_{Lr} = i_{Lr(t5)} = I_2 \ldots\ldots\ldots (3.23)$$

Here, three equations apply,

$$Cr\frac{dV_{cr}}{dt} = i_{Lr}$$

$$i.e, C_r[SV_{Cr(s)} - V_{Cr(ts)}] = I_{Lr(s)}$$

$$\Rightarrow SC_rV_{cr(s)} - C_rV_{cr(t5)} = I_{Lr(s)}$$

$$hhhhhhhhhhhhhhV_{cr(s)} = \frac{I_{Lr(s)} + C_rV_{cr(t5)}}{SC_r} \ldots\ldots\ldots\ldots (3.24)$$

$$Also\ C_s\frac{dV_{cs}}{dt} + i_{Lr} = I_2$$

$$\Rightarrow C_s\frac{dV_{cs}}{dt} = I_2 - i_{Lr}$$

$$C_s[SV_{Cs(s)} - V_{Cs(t5)}] = I_2/_S - I_{Lr(s)}$$

$$SC_sV_{cs(s)} - C_sV_{cs(t5)} = I_2/_S - I_{Lr(s)}$$

$$V_{cs(s)} = \frac{I_2/S - I_{Lr(s)} + C_s V_{cs(t5)}}{SC_s} \ldots\ldots (3.25)$$

Again,

$V_{cr} - V_{cs} = V_o - V_{Lr}$

$$V_{cr(s)} - V_{cs(s)} = \frac{V_o}{S} - L_r \frac{di_{Lr}}{dt} = \frac{V_o}{S} - L_r\left[SI_{Lr(s)} - I_2\right]$$

$$V_{cr(s)} - V_{cs(s)} = \frac{V_o}{S} - L_r SI_{Lr(s)} + L_r I_2 \ldots\ldots (3.26)$$

Combining (3.24), (3.25) and (3.26), we have after simplification

$$\therefore i_{Lr(t)} = I_2 \frac{W_{oS}^2}{W_{oT}^2} + I_2 \, Cos\, W_{oT}(t - t_5) - I_2 \frac{W_{OS}^2}{W_{OT}^2} CosW_{OT}(t - t_5) + \frac{V_T}{W_{oT} L_r} SinW_{oT}(t - t_5) \ldots\ldots (3.27)$$

Also, the resonant capacitor voltage can be derived. Substituting (3.25) into (3.27) we have

$$V_{cr(s)} - \frac{I_2}{S^2 C_s} + \frac{I_{Lr(s)}}{SC_s} - \frac{C_s V_{cs(t5)}}{SC_s} = \frac{V_o}{S} - SL_r I_{Lr(s)} + L_r I_2$$

$$V_{cr(s)} + I_{Lr(s)}\left[\frac{1}{SC_s} + SL_r\right] = \frac{V_o}{S} + L_r I_2 + \frac{I_2}{S^2 C_s} + \frac{V_{cs(t5)}}{S}$$

Substituting equation (3.24) we have after simplification

$$\therefore V_{cr(t)} = \frac{V_o W_o^2}{W_{oT}^2} - \frac{V_o W_o^2}{W_{oT}^2} Cos\, W_{oT}(t - t_5) + \frac{V_{cs(t5)} W_o^2}{W_{oT}^2} - \frac{V_{cs(t5)} W_o^2}{W_{oT}^2} Cos\, W_{oT}(t - t_5) + V_{cr(t5)} Cos\, W_{oT}(t - t_5) + \frac{V_{cr(t5)} W_{os}^2}{W_{oT}^2} - \frac{V_{cr(t5)} W_{os}^2}{W_{oT}^2} Cos\, W_{oT}(t - t_5) + \frac{I_2}{W_{oT} C_r} SinW_{oT}(t - t_5) + \frac{I_2 W_o^2}{C_S W_{oT}^2}(t - t_5) - \frac{I_2 W_o^2}{C_S W_{oT}^3} SinW_{oT}(t - t_5) \ldots\ldots (3.28)$$

Again, the snubber capacitor voltage can be derived as follows:

If we combine equations (3.24), (3.25) and (3.26) we have

$$\frac{I_{Lr(s)}}{SC_r} + \frac{V_{cr(t5)}}{S} - V_{cs(s)} = \frac{V_o}{S} - SL_r I_{Lr(s)} + L_r I_2$$

that is,

$$I_{Lr(s)}\left[\frac{1}{SC_r} + SL_r\right] = \frac{V_o}{S} + L_r I_2 + V_{cs(s)} - \frac{V_{cr(t5)}}{S} \ldots\ldots\ldots (3.29)$$

But from (3.25)

$$I_{Lr(s)} = I_2/S - SC_s V_{cs(s)} + C_s V_{cs(t5)} \ldots\ldots (3.30)$$

Combining equations (3.29) and (3.30) we have after simplification

$$\therefore V_{cs(t)} = V_{cs(t5)} - \frac{V_o W_{os}^2}{W_o^2} + \frac{V_o W_{os}^2}{W_o^2} Cos\, W_o(t - t_5) + \frac{I_2}{C_s}(t - t_5) - \frac{I_2}{C_S W_o^2} SinW_o(t - t_5) \ldots\ldots\ldots (3.31)$$

STAGE 7; $t_6 \le t \le t_7$

This stage starts from time t_6. At this time, D_{s2} is conducting as well as D_{s1} and D_{s3}. This clamps the resonant capacitor voltage at V_0 and also $V_{cs} = -V_{cs6}$ is placed across the resonant inductor.

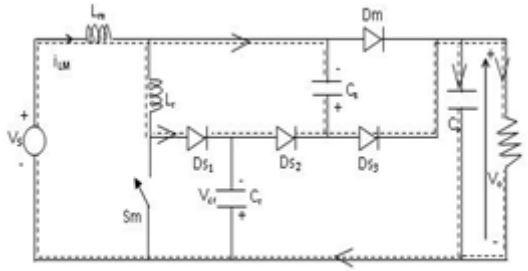


Fig (3.3h) Stage 7 operation

Thus the resonant inductor current is further decreased until it becomes zero at t_7, thus causing the whole of I_2 to flow through C_s. That is,

$$I_{Lr}(t_7) = 0;\ i_{cs}(t_7) = I_2$$

$$V_{cs} = -V_{cs7}$$

Initial conditions are

$V_{cr} = V_{cr(t6)} = V_o$

$V_{C_s} = V_{cs(t6)}$

$i_{Lr} = i_{Lr(t6)}$

Two equations apply in this case:

$$\frac{C_s dV_{cs}}{dt} = I_2 - i_{Lr}$$

$$C_s\left[SV_{Cs(s)} - V_{Cs(t6)}\right] = I_2/S - I_{Lr(s)}$$

$$V_{cs(s)} = \frac{I_2/S - I_{Lr(s)} + C_s V_{cs(t6)}}{SC_s} \ldots\ldots (3.32)$$

Also,

$$L_r \frac{di_{Lr}}{dt} = V_{cs}$$

$$L_r\left[SI_{Lr(s)} - I_{Lr(t6)}\right] = V_{CS(s)}$$

$$\therefore I_{Lr(s)} = \frac{V_{CS(s)} + L_r I_{Lr(t6)}}{SL_r} \ldots\ldots (3.33)$$

Combining equation (3.32) and (3.33) we shall have after simplification

$$I_{Lr(s)} = I_2[1 - Cos\ W_{os}(t - t_6)] + \frac{V_{CS(t6)}}{Z_{oS}}\ SinW_{os}(t - t_6) + I_{Lr(t6)}\ Cos\ W_{os}(t - t_6) \dots\dots\dots\dots (3.34)$$

Also, if we substitute (3.33) into (3.32) we have after simplification

$$V_{CS(t)} = I_2 Z_{oS}\ SinW_{os}(t - t_6) - I_{Lr(t6)} Z_{oS}\ SinW_{os}(t - t_6) + V_{CS(t6)}\ Cos\ W_{os}(t - t_6) \dots\dots\dots\ (3.35)$$

STAGE 8; $t_7 \leq t \leq t_8$

The soft switching capacitor with $i_{cs}(t_7) = I_2$ which is constant till t_8, discharges till the soft switching capacitor voltage V_{cs} becomes zero at t_8. At this point in time the voltage becomes clamped to zero and the charging current I_2 is transferred to D_m for conduction so as to discharge the energy in L_m to the load.

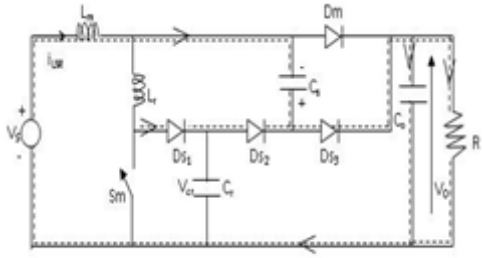


Fig (3.3i) Stage 8 operation

At t_8, mode of conduction becomes as assumed before t_0 and this condition will continue till t_9 when S_m is turned on again to start a new circuit cycle.

Initial conditions are,

$$i_{Lr} = i_{Lr(t7)} = 0$$
$$i_{Cs} = i_{Cs(t7)} = I_2$$
$$V_{cr} = V_{cr(t7)} = V_o$$
$$V_{cs} = V_{cs(t7)}$$

But only the snubber capacitor is involved.

$$\frac{C_s dV_{cs}}{dt} = I_2$$
$$C_s[SV_{Cs(s)} - V_{Cs(t7)}] = {}^{I_2}/_{S}$$
$$hhhhhhhhhhhhh\ V_{Cs(s)} = \frac{{}^{I_2}/_{S} + C_s V_{Cs(t7)}}{SC_s}$$
$$V_{Cs(s)} = \frac{I_2}{S^2 C_s} + \frac{V_{Cs(t7)}}{S}$$
$$\therefore V_{Cs(t)} = \frac{I_2}{C_s}(t - t_7) + V_{Cs(t7)} \dots\dots\dots (3.36)$$

STAGE 9; $t_8 \leq t \leq t_9$

The main diode D_m is now conducting current and $i_{Dm} = i_{Lm}$ which falls from $i_{Lm} = I_2$ at t8 to $i_{Lm} = I_1$ at t_9 when the main active switch S_m is turned on again to restart the switching cycle. Diagram for $t_8 \leq t \leq t_9$ is the same as for the initial stage [see fig (3.3a)]

Initial conditions are

$$i_{Lm} = i_{Lm(t8)} = I_2;$$
$$V_{cr} = V_{cr(t8)} = V_o$$
$$V_{cs} = V_{cs(t8)} = 0$$

One equation applies to this mode:

$$\frac{L_m di_{Lm}}{dt} = V_s - V_o$$
$$L_m[SI_{Lm(s)} - I_2] = \frac{(V_s - V_o)}{S}$$
$$I_{Lm(s)} = \frac{(V_s - V_o)}{S^2 L_m} + {}^{I_2}/_{S}$$
$$\therefore i_{Lm(t)} = \frac{(V_s - V_o)}{L_m}(t - t_8) + I_2 \dots (3.37)$$

4. CONCLUSION

It is necessary to state here that $V_s - V_0$ gives a negative value since in a boost converter the output voltage is always greater than the supply voltage. In fact, from the prototype a supply voltage of 48 volts was used to light a bulb of 230 volts. As time progresses from t_8, the main inductor current which at t_8 is I_2, falls gradually to I_1 which is the value at the beginning of mode 1. The graph below is a measure of the voltage across the load R from the constructed prototype.

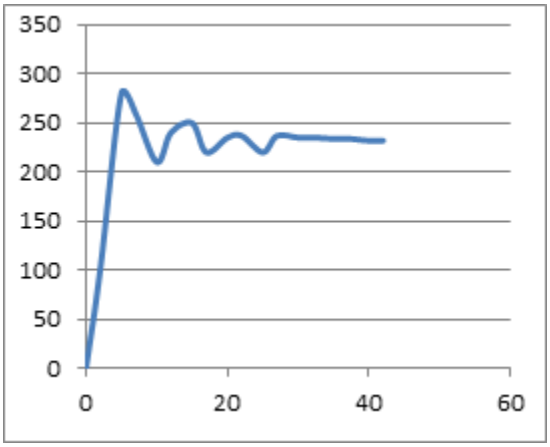


Fig. (13) Voltage across the load R

5. REFERENCES

1. B. T. Lin, K.W. Siu and Y. S. Lee, "Actively clamped zero current switched Quasi Resonant Converters Using IGBT", IEEE Trans. On Industrial Electronics, Vol. 46 No.1 pp.75-81, Feb. 1999.

2. Daniel W. Hart, "Introduction to Power Electronics", Prentice Hall, New Jersey (07458), 1999.

3. R. Rangan et al, "Application of Insulated gate bipolar transistor to zero-current switching converters", IEEE Trans. Power electronics, vol. 4, pp. 2-7, Jan. 1989.

4. C. A. Canesin, C.M.C. Duarte, and I.Barbi, "A new family of pulse-width-modulated zero-current – switching dc/dc converters", in IEEJ IPEC Rec., 1995, pp. 1379- 1384.

5. G. Hua and F.C Lee, "Soft-switching techniques in PWM converters", in Int. Conf. Ind. Electron., Control and Instrumentation, 1993, pp. 637-643.

6. A. Elasser and D. A Torrey, "Soft-switching active snubbers for dc/dc converters", IEEE Trans. Power Electron., vol. 11, pp. 710-722, Sept. 1996.

7. I. Husain and M. Ehsani, "Analysis of high Power soft-switching dc-dc converters using basic three-terminal structures", in Int. Conf. Ind. Electron., Control and Instrumentation, 1995, pp. 252-257.

8. R. L. Steigerwald, "A review of soft-switching techniques in high performance dc power supplies", in IECON, 1995, PP. 1-7.

9. R. L Steigerwald, R. W. De Donker, and M. H Kheraluwala, "A comparison of high-power dc-dc soft-switched converter topologies", IEEE Trans. Ind Applicat., vol. 32 pp. 1139-1145, Sept./Oct.1996.

10. Helio Leaes Hey, Carlos Marcelo de Oliveira Steing, "A true ZCZVT Commutation cell for PWM Converters", IEEE Trans. Power Electron Vol. 15, No. 1, January 2000.

11. Julian Y. Zhu, Daohong Ding, "Zero-voltage- and zero-current-switched PWM DC-DC Converters using Active sunbber", IEEE Trans. On Industr. Applic. Vol. 35. No. 6 Nov/Dec. 1999.

12. T. A Meynard and H. Foch, "Multilevel conversion: High-voltage choppers and voltage-source inverters", in proc PESC' 92 Conf. Rec., 1992, pp. 397-403

13. Eduardo Deschamps & Ivo Barbi, "A Flying-capacitor ZVS PWM 1.5KW DC-DC Converter with half of the input voltage across the switches", IEEE Trans. on Pow. Electron. Vol. 15, No. 5, Sept. 2000.