International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 10 | Oct 2019 www.irjet.net p-ISSN: 2395-0072

PERFORMANCE ANALYSIS OF CLOCK AND DATA RECOVERY CIRCUITS USING MULTILEVEL HALFRATE PHASE DETECTOR

Kanagavalli S A[1]& Padma S I[2] & Mustafa Nawaz S M[3]

[1]PG SCHOLAR, PET ENGINEERING COLLEGE
[2]ASSISTANT PROFESSOR, PET ENGINEERING COLLEGE
[3]ASSISTANT PROFESSOR, PET ENGINEERING COLLEGE

Abstract – This papers represents a recent communication system of electronic industry will focusing on high speed signal processing application, with the assistance of optical to electrical data communications, multiplexing technique of TDMA, CDMA, OFDMA. Here data communication will required a high priority to recover clock and reduced jitter in clock and data with high performance synchronous operations such as the retiming and demodulation. Here this work will present a technique of Half-Rate (HR), Bang-Bang Phase Detector (BBPD) based multiple decision of clock and data recovery about the sign and magnitude of the phase shift between the PD inputs. Here, this proposed architecture will introduced a GDI (Gate Diffusion Input) technique and reduced the number of transistors in this data and clock recovery technique of HR-BBPD and ML-HR-BBPD at 90nm CMOS Technology with using DSCH3 and MICROWIND software and compared all the parameters in terms of Area, Delay and Power.

Key Words: Clock and data recovery (CDR) circuits, Half Rate (HR), Phase Detector(PD), Bang Bang (BB), Multilevel (Ml).

1. INTRODUCTION

Impulse-radio ultra wideband (IR-UWB) communication is a promising solution for high data rate, short-range, and low power communication due to the duty-cycled nature of the output signal as well as the potential for low-complexity and low-power transmitter(TX) architectures. Continuous-time nMOS/pMOS current-matching loop through adaptive with a back-gate-driven amplifier for voltage range compatibility. The total phase noise at the end of the burst in order to ensure correct demodulation of the BPSK-encoded data. At system level, we forced both phases of the LO to be gated at the low logic level to ensure that the frequency divider and the dual ring counters are in data retention without further additions to the TSPC flip-flop architecture[1]. In Serial Data communication systems, clock and data recovery (CDR) circuits play a critical role for achieving required receiver performance. The phase generator should provide more than 1-UI phase range since the initial phase error is unknown. With our technique, the initial phase error is statistically zero due to the CDR operation. The control code from the bit generator selects the counters used for accumulating VD-BBPD output signals. [2]. Clock and data recovery circuit (CDR) is a key building block in all serial communication systems where it performs the crucial function of recovering clock and retiming the received data. The mismatch in the pole-zero cancellation does not change jitter transfer (JTRAN) bandwidth, which is determined by the dominant pole to improve phase interpolation linearity and power efficiency are proposed. The power dissipation in a conventional PRPLL is dominated by the XOR phase detectors and the voltage-to-current (V-I) converter needed to drive the passive loop filter. Current-mode logic (CML) XOR[3]. The performance of Clock and Data Recovery (CDR), a key receiver timing circuit in clock-embedded serial link systems, becomes critical to achieve optimal data sampling over various timing jitter profiles. To achieve the best timing margin over different jitter spectral profiles, it is necessary to find the optimal CDR loop gain. If low frequency jitter is dominant, large loop gain is desirable to enhance jitter tracking capability Adaptive loop gain schemes have been frequently employed in PLLs and CDRs to enable a self-tuning capability for various performance metrics, such as lock time, Jitter Generation (JGEN), Jitter Tolerance (JTOL), loop stabilization and Spread Spectrum Clocking (SSC)[4]. The process variation is an important factor in multi-gigahertz systems. Therefore, it is necessary to determine the timing resolution of BIJM and calibration techniques. The TA structure increases the timing resolution. For 3 GHz systems, the timing difference is small. Using a TA can increase the timing resolution of BIJM. The standard deviation is also the RMS jitter. [5].

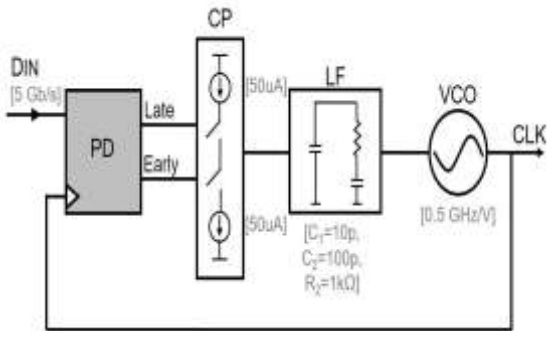

Fig 1: Block diagram of a PLL-based CDR showing the parameters used in our Verilog AMS model.

2. METHODOLOGIES

a)Transmitter SoC in 28-nm FDSOI CMOS

Achieving wireless communications at 5–30 Mb/s in energy-harvesting Internet-of-Things (IoT) applications requires energy efficiencies better than 100 pJ/b. Impulse-radio ultra wideband (UWB) communications offer an efficient way to achieve high data rate at ultralow power for short-range links. We propose a digital UWB transmitter (TX) system-on chip (SoC) designed for ultralow voltage in 28-nm FDSOI CMOS. It features a PLL-free architecture, which exploits the duty cycling nature of impulse radio through aggressive duty cycling within the pulse modulation time slot for high energy efficiency and minimum jitter accumulation.

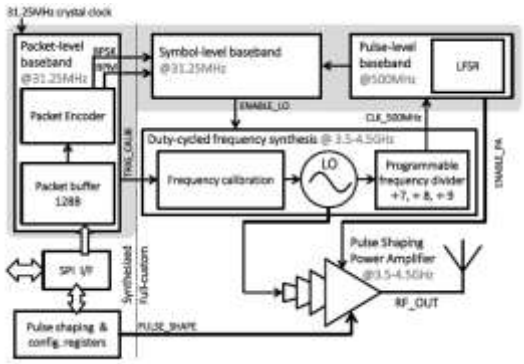

Fig: 2 Architecture of the Transmitter.

The baseband is partitioned between crystal- frequency blocks synthesized from standard cells and aggressively duty-cycled high-frequency full-custom blocks. It is built from a single 31.25-MHz reference crystal clock from which all necessary high-frequency clocks are generated in the duty-cycled frequency synthesis block. It features a 3.5–4.5-GHz LO whose frequency is divided to generate a 500-MHz internal clock with a 2-ns period corresponding to the pulse duration. The calibration of the LO frequency is performed periodically as triggered by the TRIG_CALIB signal. The TX covers seven data rates defined in the 802.15.4a standard.

b) Programmable Multi-Level Phase Detector

The paper proposes a clock and data recovery (CDR) circuit having a new type of a multi-level bang-bang phase detector (ML-BBPD). The gain characteristics of our ML-BBPD can be programmed by scanning the dead-zone width of a variable dead zone BBPD in the time domain. Its linear-like gain characteristics result in less sensitive CDR performance against input jitter and process, voltage, and temperature (PVT) variations. In addition, a built-in on-chip jitter monitor can be easily implemented using our ML-BBPD.

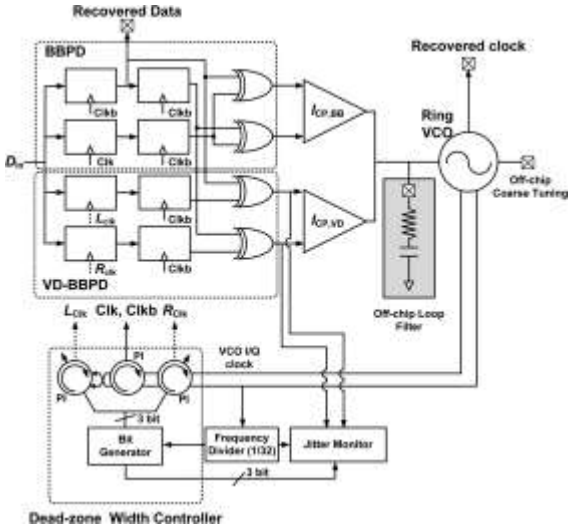

Fig: 3 Clock and Data Recovery aritecture with a jitter monitor.

1.25-Gb/s full-rate CDR circuit with the proposed ML-BBPD and jitter monitor. An off chip resistor and a capacitor are used for the loop filter so that we can easily modify the loop filter dynamics for evaluation purpose. In addition, the complexity of the phase generator can be significantly reduced the phase generator should provide more than 1-UI phase range since the initial phase error is unknown the initial phase error is statistically zero due to the CDR operation. The jitter distribution provided by our jitter monitor is in reference to the retimed clock and it is not able to subtract/exclude CDR jitter due to input jitter.

C) Phase Rotating Phase –Locked Loop

In this paper a reference-less half-rate digital clock and data recovery (CDR) circuit employing a phase-rotating phase-locked loop (PRPLL) as phase interpolator is presented. By implementing the proportional control in phase domain within the PRPLL, the proposed CDR decouples jitter transfer (JTRAN) bandwidth from jitter tolerance (JTOL) corner frequency, eliminates jitter peaking, and removes JTRAN dependence on bang-bang phase detector gain. Fabricated in a 90 nm CMOS process, the prototype CDR achieves error-free operation (BER < 10^{-12}) with PRBS data sequences ranging from PRBS7 to PRBS31..

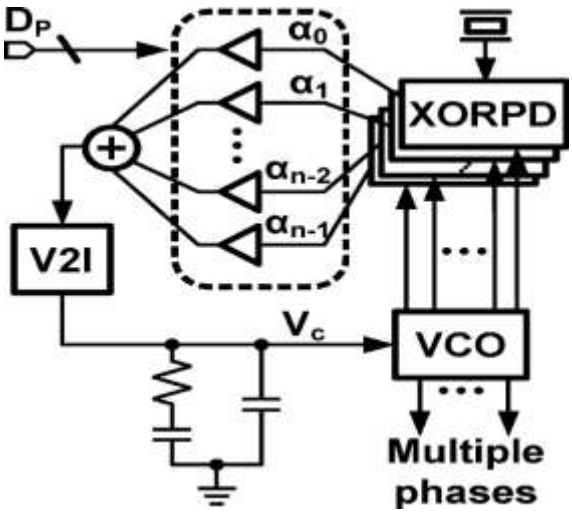

Fig: 4 Phase Rotating Phase Locked Loop block diagram.

PRPLL presents an interesting phase shifting technique without using an explicit phase interpolator, and it overcomes the inherent non-linearity that comes with implementing interpolation in phase domain . Different from a conventional charge-pump PLL, it consists of multiple XOR phase detectors the output currents are weighted, summed, and filtered to generate the control voltage. By weighting the individual XOR outputs differently using control word, the amount of output phase shift can be varied. Compared to a conventional PI, thanks to the current-domain operation, the PRPLL approach exhibits superior digital-to-phase conversion linearity. To improve phase interpolation linearity and power efficiency are proposed. The power dissipation in a conventional PRPLL is dominated by the XOR phase detectors and the voltage-to-current (V-I) converter needed to drive the passive loop filter.

d) Mixed mode Adaptive Loop Gain Strategy

A Bang-Bang Clock and Data Recovery (CDR) with adaptive loop gain strategy is presented. The proposed strategy enhances CDR jitter performance even if jitter spectrum information is limited a priori. By exploiting the inherent hard-nonlinearity of Bang-Bang Phase Detector (BBPD), the CDR loop gain is adaptively adjusted based on a posteriori jitter spectrum estimation. Maximizing advantages of analog and digital implementations, A modified CML D-latch improves CDR input sensitivity and BBPD performance. A folded-cascode- based Charge Pump (CP) is proposed to minimize CP latency. The CDR prototype is fabricated in 0.18 µm CMOS technology to demonstrate the effectiveness of the proposed techniques for applications with high ratio of data-rate. The CDR power consumption is 110.6 mW where only 3.9 mW is used for loop gain adaptation circuitry.

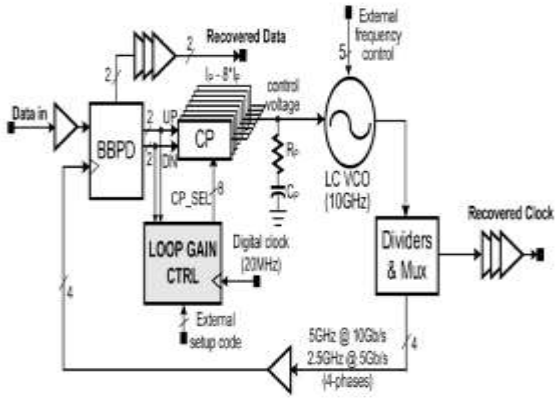

Fig:5 Adaptive loop gain clock and data recovery architecture.

Adaptive loop gain CDR based on the half-rate Bang- Bang PLL architecture, the CDR employs a Loop Gain Controller (LGC) to perform the adaptive loop gain control. Triggered by a low frequency clock, the LGC monitors BBPD outputs, detects the current jitter spectral profile, and adjusts the CP current. The BBPD is implemented employing a modified CML D-latch. The CP is composed of eight segmented CP units. By controlling the number of active units, the CP current is digitally adjustable by factor of eight. A folded-cascode-based CP enhances speed, input and output voltage range. At high frequency, the proposed CDR shows almost same JTOL Performance as the minimum loop gain CDR.

e) Built-in Jitter Measurement Circuit

This paper proposes a 3-GHz built-in jitter measurement (BIJM) circuit to measure clock jitter on high-speed transceivers and system-on-chip (SoC) systems. The proposed BIJM circuit adopts a high timing resolution and self-calibration techniques. The calibration techniques can reduce the timing resolution variation of the vernier ring oscillator and the gain variation of the TA by 66% and 65%, respectively. This reduces the timing resolution variation of BIJM by 60%.

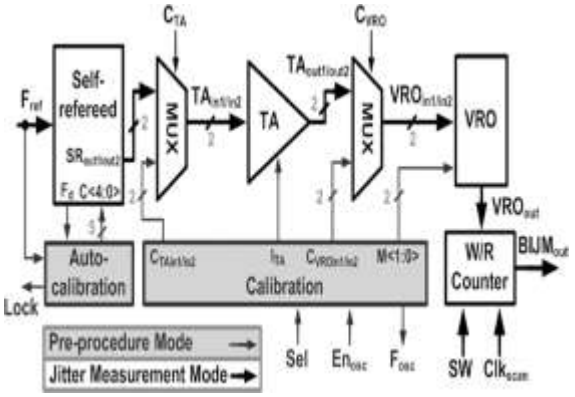

Fig: 6 Built-in –jitter measurement architecture

The BIJM, which consists of two modes: the pre-procedure mode and jitter measurement mode. The pre-procedure mode consists of a self-refereed circuit with the auto-calibration technique, and TA and VRO with the calibration techniques, C_{TA} and C_{VRO} signal control the operation of BIJM into the pre-procedure or the jitter measurement modes.

RESULT AND DISCUSSION

Process	90 nm	90 nm	90 nm	0.18μm	0.13 μm	28nm FDSOI
Data rate [Mb/s]	0.11, 0.85, 0.8	16	12.8	27.21	0.11, 0.85, 1.7, 6.81, 27.24	0.11, 0.85, 1.7, 6.81, 27.24
Active power [μW]	18000	600	4200	NA	3400	TX: 380 SoC: 650
Energy per bit [pJ/bit]	2629.6 @ 6.8Mb/s	600 @ 2Mb/s	280 @15.6Mb/s	746 @27.24Mb/s	299 @27.24Mb/s	TX: 14 SoC: 24 @27.24Mb/s
Die area [mm²]	NA	0.008	0.07	4.5	EF: 7.5 Dig: 301 34.7	TX: 0.085 SoC: 0.95
Supply voltage [V]	2.5	1	1	1.8	1.2	External: 1.2 Core: 0.85* IH: +/-1.8*
Output swing [dV_{pp}]	~600	~150	800-720	NA	Up to 720	Up to 800
LO freq. range [GHz]	3.5-6.5	3-10	2.5-8.7	5-8	3.5-4.5	3.5-4.5
Transmitted output power [dBm]	NA	<-14.5	-10.4	< 4.5	NA	-20

Table: 7 Performance Comparisons for the IEEE 802.15.4

The table compares the performances of recent IEEE 802.15.4a TX or transceivers. The proposed UWB TX is the first designed in 28-nm FDSOI CMOS. The combined use of coarse to fine-grain duty cycling, advanced CMOS process, ULV operation enabled by FBB-induced V_T reduction, and high-speed design explains the obtained ultralow-power consumption.

Data Rate	5 Gb/s	5 Gb/s	1.25 Gb/s	1.25 Gb/s
Technology	180-nm CMOS	90-nm CMOS	180-nm CMOS	180-nm CMOS
Supply Voltage	1.8 V	1.2 V	1 V	1.8 V
Power	80 mW	16.8 mW	68 mW	39.6 mW
Area	N/A	0.3 mm^2	N/A	0.107 mm^2
Jitter of Recovered Clock (UIrms)	2.4 %	0.88 %	1 %	0.54 %
PD type	ML-BBPD	ML-BBPD	ML-BBPD	ML-BBPD
Rate of PD	1/2 rate	1/4 rate	Full rate	Full rate

Table: 8 Performance Comparisons for the ML-BBPD CDRs

The Performance of ML-BBPD CDR Produces the smallest rms jitter for the recovered clock and consumes less power than the other CDR fabricated in same CMOS technology.

Technology	0.18 μm	0.13 μm	0.13 μm	65 nm	0.13 μm	90 nm
Supply (V)	1.8	3.3/1.8	1.2	1.2	0.8/1.2	1.2/1.8
FTRAN [MHz]	0.9	1.2	1.4	N/A	N/A	2.3
Oscillator	LC	LC	Ring	Ring	Ring	Ring
Jitter [p_{rms}/p_{p-p}]	0.5/8.8	0.6/5.1	7.2/47.2	8.7/57.3	5.4/44.0	5.0/44.0
Input sensitivity [mV]	8	10	N/A*	N/A*	N/A*	10
Power [mW]	725.5**	880**	13.2	20.6	6.1	13.1/18.6**
Data rate [Gb/s]	2.5	11.4	2.5	6.65	2.0	5.0
Power efficiency [mW/Gb/s]	290.2**	79.2**	5.28	3.1	3.05	2.62/3.72**
Architecture	Full-rate	Half-rate***	Full-rate***	Full-rate	Half-rate	Half-rate

Table: 9 Clock and Data Recovery Comparison Performance

The CDR compares favorably both in terms of power efficiency and jitter with CDRs implemented using ring oscillators are Compared to LC oscillator-based CDRs in the power efficiency is superior but jitter is higher. Including the on-chip limiting amplifier power consumption in this work, the proposed design still achieves much better power efficiency of 3.72 mW/Gb/s compared to the designs where limiting amplifiers are also implemented on-chip.

4. CONCLUSION

In this survey paper, an ML-HR-BBPD is proposed. It offers a nice trade off between pure linear and pure BB HR-PD, providing multiple levels of quantization to measure the phase difference and tune the VCO in a PLL implementation the ML-HR-PD retains all the advantages of the HR-BBPD at the cost of a slightly higher complexity

while it reduces the jitter of the generated clock by up to 30% thanks to the finer control of the VCO. This jitter reduction which allows to reducing the BER up to 5 times when an input signal at 5 Gb/s is affected by jitter.

REFERENCES

[1] G. de Streel et al.,(2017). "SleepTalker: A ULV 802.15.4a IR-UWB transmitter SoC in 28-nm FDSOI achieving 14 pJ/b at 27 Mb/s with channel selection based on adaptive FBB and digitally programmable pulse shaping," IEEE J. Solid-State Circuits,.

[2] Jour Dae-Hyun Kwon, Young-Seok Park, and Woo-Young Choi,(2015). "A clock and data recovery circuit with programmable multi-level phase detector characteristics and a built-in jitter monitor," IEEE S transactions on circuits and system,.

[3] Shu et al.,(2014). "A reference-less clock and data recovery circuit using phase-rotating phase-locked loop," IEEE J. Solid-State Circuits,.

[4] H. J. Jeon et al.,(2013) "A bang-bang clock and data recovery using mixed mode adaptive loop gain strategy," IEEE J. Solid-State Circuits,.

[5]K. H. Cheng et al.,(2011). "Built-in jitter measurement circuit with calibration techniques for a 3-GHz clock generator,"IEEE Trans. Very Large Scale Integr. (VLSI) Syst.,.

[6] J. Lee, K. Kundert, and B. Razavi,(2004) "Analysis and modeling of bangbang clock and data recovery circuits," IEEE J. Solid-State Circuits,.

[7] M. Sasaki et al.,(2010) "A circuit for on-chip skew adjustment with jitter and setup time measurement," in Proc. IEEE Asian Solid-State Circuit Conf.

[8] J. Poulton et al.,(2007) "A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS," IEEE J. Solid-State Circuits.

[9] C. Sanchez-Azqueta, C. Gimeno, C. Aldea, and S. Celma,(2013) "New multilevel bang-bang phase detector," IEEE Trans. Instrumentation.,