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Design of 16 Bit Low Power Vedic Architecture using CSA & UTS

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Abstract - *Vedic mathematics provides simple mathematical approaches to increased speed and reduced power consumption as in comparison to conventional designs. Multipliers are main building block of ALU, which improves the speed of many functions like Fourier transformation, digital filters and Digital Signal Processor (DSP). Leakage power and low speed has become a general issue in circuit design, for any function we need to reduce the delay in system. In proposed method, we design Vedic Multiplication Algorithm for 16 bit Low Power Vedic Architecture using Urdhava Tiryakbhyam Sutra (UTS) method and Carry Select Adder (CSA) with Vedic mathematics technique. UTM means vertically and cross wise vedic mathematics. It is faster technique used for decimal number multiplications, the computation process is increased and the processing time is reduced due to decrease of combinational path delay compared to the existing multipliers. In our proposed Vedic multiplier architecture the power consumption is less and we get less time delay compared to other algorithms.*

Key Words: **VLSI, Vedic Multiplier, Leakage power, CSA, RCL, Fast Fourier Transform.**

1. INTRODUCTION

The one of the essential and mostly used functions in computer operations is Multiplication. Reducing the time delay and power consumption are very essential requirements for microprocessor operations. The basic blocks in Digital Signal Processing (DSP) operation are Arithmetic logical unit and Accumulate (MAC). [3]They perform multiply operation as basic function to be implemented. The multipliers are the main block in high speed arithmetic logic units, multiplier and accumulate units, digital signal processing units etc. Currently, the execution time of a digital signal processing chip in convolution, filtering, Fast Fourier Transform etc, are still depends on the multiplication time. [5][6]

Digital signal processing applications need of high speed processors. The Vedic multipliers based on Vedic mathematics are presently under focus on one of the fastest and low power multiplier. The "Urdhva Tiryakbhyam" (UTS) has been noticed to be the most efficient one in terms of speed among sixteen sutras in Vedic multiplication. [15]

A large number of high speed Vedic multipliers have been proposed with Urdhva Tiryakbhyam Sutra & CSA technique. This Multiplication is basic function in arithmetic operations such as Multiply and Accumulate(MAC) and inner product. These are frequently used Computation Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing(DSP) applications. The convolution, Fast Fourier Transform(FFT), filtering and arithmetic & logic operations are best example of it [4][9]. There is a need of high speed multiplier because of multiplication dominant in DSP algorithms. Multiplication time is still the dominant factor in instruction cycle time of a DSP chip. The use of high speed processing has been increasing as because expanding computer and signal processing applications. [13]

The development of fast multiplier circuit is done by Vedic multiplication technique in this paper. A 16 bit digital multiplier is proposed which is based on UTS (Vertically & Crosswise) Sutra. Two 16-bit binary numbers are multiplied with this Sutra. The main concept of this paper is that the speed of propagation and decrease in delay of the conventional architecture.

2. RELATED WORK

Low power consumption is important design for advanced processors with High performance digital adder. The speed of operation of such an adder is limited by carry propagation is an optimized adder for advanced processors. The implementation of Carry Select Adder without using multiplexer for final selection and in this approach uses first, the implementation of cin=0 adder and then Excess 1 adder. Excess 1 adder is design form in this way that it becomes a first zero finding logic and replaces the final MUX stage used in conventional approach. Designing of parallel adder configuration is also used to reduce the delay between stages. The Kogge Stone tree approach will give option to generate fast carry for intermediate stages. The adder is implemented on FPGA and is compared with CSA. The adder gives reduced area and better speed compared to other adders.[4][9]

Multiplier design based on ancient Indian Vedic Mathematics Reduces multiplication algorithm. Bit-reduction in multiplication reduces general 4 × 4 bit multiplication to a single 2 × 2 bit.[5]

Low Power and Area- Efficient Carry Select Adder (CSLA) structure is better than the convectional SQRT CSLA in terms of delay, area, power. This CSLA architecture has been developed using Binary to excess one converter its efficient method which replaces a BEC using common Boolean logic. The architecture achieves advantages in terms of area, delay and power.[6] High performance digital adder with reduced area and low power consumption is an important design

constraint for advanced processors. This work based on designing an optimized adder for advanced processors.[4]

The reduction of area and total power are achieved by reducing gates in architecture. The power delay product and also the area-delay product of 16-32-bit sizes which indicates the success of the method. The CSLA architecture is low area & delay, simple and efficient for VLSI hardware implementation.[5][6]

3. PROPOSED METHODOLOGY

In VLSI design, the main focus of research is the reduced size and increase speed path in logic systems. The speed of addition depends on the propagation of carry which is generated sequentially after the addition of previous bit & carry is propagated into the next position. Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Skip Adder and Carry Select Adder are available, which have their own advantages and disadvantages. Design of Carry select adder offers the high speed, low power consumption, regularity of layout less area and compact VLSI design implementation. Vedic multiplier using carry select adder are proposed in this paper, by Vedic multiplication Technique.

The 16 Bit Low Power Vedic Architecture Using CSA & UTS shown in fig. 1. This structure design by using 8- bits blocks. The 16 bit multiplicand A can be decomposed into pair of 8 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The outputs of 8- bit multipliers are added accordingly to obtain the 32 bits final product.

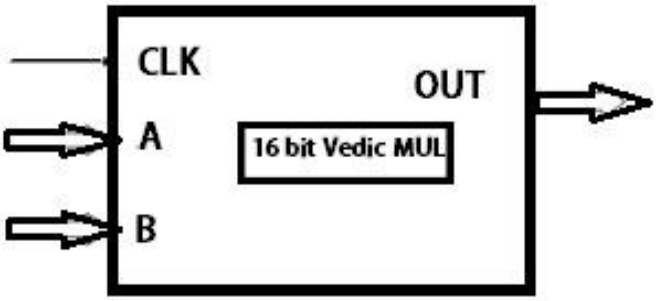

Fig -1: Proposed 16-bit Vedic Multiplier

The proposed system is easier solution for improving the speed of the procedure, we used Modified Vedic multiplier with carry select adder. Vedic multiplier is based on the Urdhva Tiryagbhyam Sutra (UTS). UTS Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. The proposed method is a general multiplication formula applicable to all cases of multiplication. UTS means Vertically and Crosswise, it is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. This algorithm can be generalized for n x n bit number. Since products and sums are calculated in parallel and the multiplier is independent of the clock frequency.

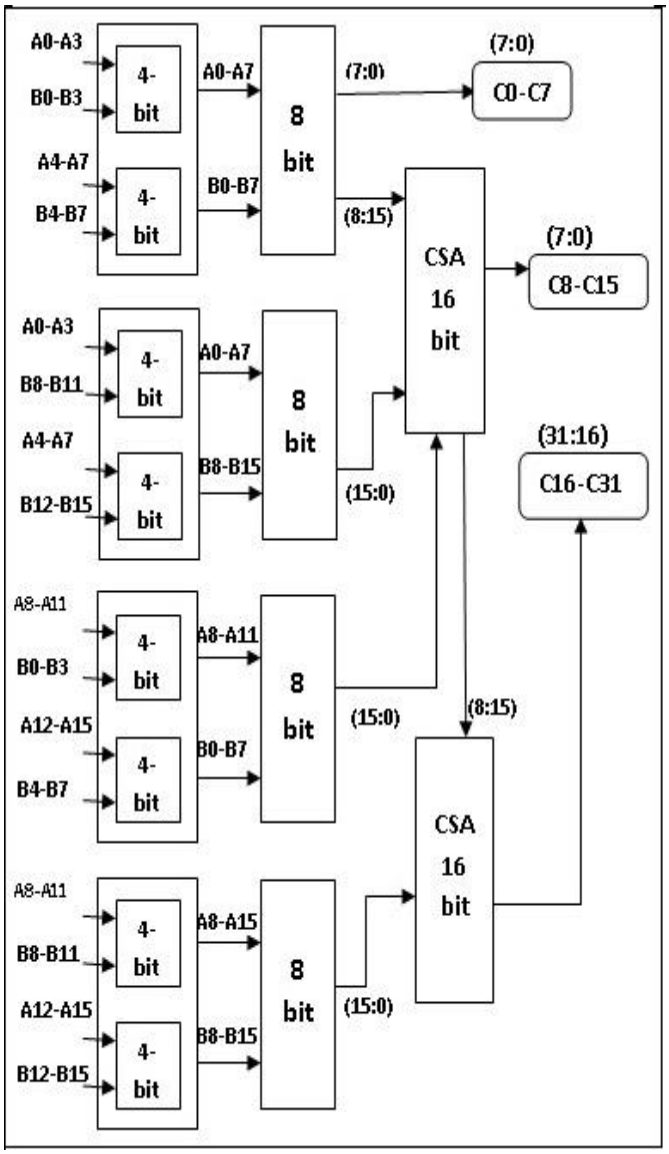

Fig -2: Proposed 16-bit Vedic algorithm

For implementation of Urdhava Tiryakbhyam Sutra(UTM) is the least significant bits of the two numbers are first multiplied vertically, followed by addition of the products got by cross wise multiplication of both the digits and finally the most significant bits of the two numbers are multiplied vertically.

The result of the multiplication of the two numbers is got by adding up all the products received in the three steps, i.e., addition of the partial products obtained by vertical multiplication and cross-wise multiplication.

Let the two 2-bit numbers be X_2X_1 and Y_2Y_1;

Result: $X_1Y_1 + (X_2Y_1 + Y_2X_1) + X_2Y_2$.

This Same pattern is followed in multiplication. The numbers are divided into two equal parts, then vertical & crosswise multiplication and addition is done to gain the partial products and finally the sum of the partial products gives final result [4,8]. For two 4-bit numbers $X_4X_3X_2X_1$ & $Y_4Y_3Y_2Y_1$ UTM is implemented in their multiplication. The UTM method as applied to two 2-bit numbers, Hence for the multiplication of two 4-bit numbers there is a requirement of four 2-bit multipliers following the UTM. Consider two N-bit numbers Xn Xn-$_1$ … X_2X_1 and Yn Yn-$_1$ … Y_2Y_1. They are to be divided into two halves before multiplication. The final result of multiplication of two N-bit numbers thus require four N/2 bit multipliers following UTM , and these N/2 bit multipliers would further require four N/4 bit multipliers employing UTM and so on until the fundamental 2-bit multiplier is reached.

In this paper we propose a 16- Vedic multiplier using CSA & UTS. This will reduce the area and improve speed. Due to its regular structure, it can be easily implement in microprocessors to avoid catastrophic device failures. It can be easily implement in a silicon chip. The Vedic Multiplier based on this UTS that has advantage of low power, bit increases, gate delay and less area as compared to other conventional multipliers.

4. RESULT AND DISCUSSION

The simulation of 16- Bit low power Vedic architecture using CSA & UTS has done in Xilinx 14.2i version. The adders and multipliers is implemented and simulation results were tested. The gate delay count in CSA offers higher speed than the other two. 1, 4, & 8 bit Vedic multipliers have been overviewed by simulation. 16- bit Vedic multipliers designs show lesser delay and use lower power than existing multipliers. This multipliers can be used in DSP and communication applications which require higher speed and lower power consuming systems.

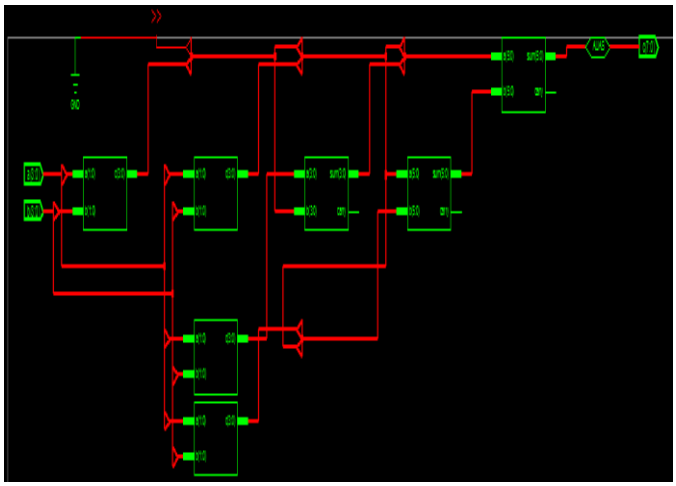

Fig -3: RTL view of 16-bit Vedic multiplier

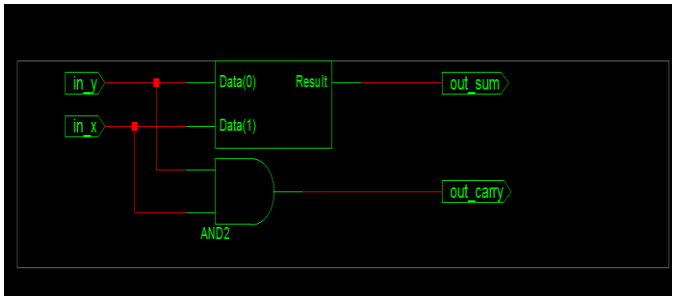

Fig -4: Schematic Diagram of 16-bit Vedic multiplier

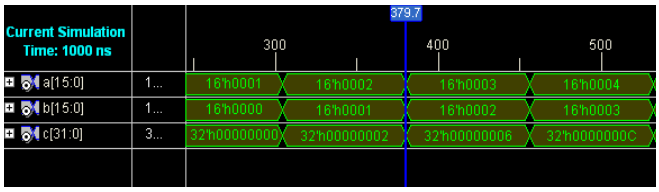

Fig -5: Waveforms of 16-bit Vedic multiplier

Table -1: Comparison of different Multipliers performance in terms of Area and Speed

Type of multiplier	**Conventional Multiplier**	**CSA & UTS based Vedic multiplier**
Speed / delay in ns	108	84
Area in terms of slices(LUT Buffer, register)	884	1220
Area delay product	83154	108050

5. CONCLUSION

An Efficient 16 bit low power Vedic multiplier is designed using CSA & UTS. In this work we used reduces delay as compare to the conventional multiplier and we modified Vedic multiplier with CSA & UTS. All the adders are simulated in Xilinx 14.2 version and the performance is compared and the proposed structure proves to be easier solution for improving, the speed of the procedure. The computation delay for 16-bit multiplier was 108 ns and proposed Vedic multiplier with CSA & UTS has a delay of 84 ns only, it is therefore seen that the proposed Vedic multiplier architecture is much faster than the conventional multipliers.

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