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Comparative Study of Implementation of 8-bit Carry Select Adder using different Technologies

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Abstract - *The addition of two numbers represents the most fundamental arithmetic operation that can be done on two numbers. The addition of two multi-bit numbers involves the propagation of a carry component from one stage to the next. When computations involve large numbers the propagation of this carry component presents a bottleneck to overall system speed as the overall circuit delay is represented by the time taken to produce the sum of the final input bits. This paper analyses an eight-bit carry select adder utilizing four bit carry look ahead adders as the individual stages. Further, the carry look ahead adders have been implemented using three MOS circuit design styles, Static, Dynamic (MODL) and Pass Transistor logic.*

Key Words: **full adder, carry propagation, propagation delay, carry look ahead adder, carry select adder, static, dynamic, pass transistor.**

1. INTRODUCTION

The mathematical operation of addition is the most fundamental calculation that can be done with two numbers. Addition allows us to combine two numbers and see the value of the overall result. The addition of two numbers can produce a carry from the lower digits to the higher digits depending on the inputs applied. Since a digital adder works on binary bits, the additions of two one's produces a carry with the sum being zero.

1.1 Full Adder

Adders form an essential part of any arithmetic circuit. In digital VLSI, the process of addition can be realized using the following Boolean equation insert Boolean equation that can be implemented using the following three basic logic gates, the XOR gate to generate the sum part of addition, AND gates and OR gates to produce the carry from a lower stage to the next higher stage. The circuit shown in figure-1 represents a one bit adder full adder which takes three inputs namely A, B and Cin where A is the first bit, B is the second bit and Cin represents the carry input from the previous stage.

1.2 Ripple Carry Adder

N-bit adder can be created by cascading N full adders, such an adder is called a Ripple Carry Adder. The carry of previous stage is needed to calculate the sum of the next stage. RCA has the easiest architecture and has the least area required, the complexity and delay increase of a Ripple Carry Adder is linear to the increase in the number of bits.

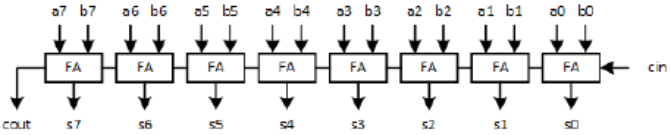

Fig -1: Ripple Carry Adder[3]

1.3 Carry Look Ahead

The Carry Look Ahead adder is a fast adder in which the generation of successive carry bits is not dependent on generation of carry from previous bit additions. The extra segments of this adder are the carry propagate and carry generate, where the carry propagate will be propagated to the next stages and the carry generate is responsible for the advanced generation of carry irrespective of input carry given to the first stage.[2]

Carry bits are generated simultaneously significantly mitigating the problem of propagation delay faced in RCA but at the cost of increased circuitry. A major drawback of CLA adders is that the increase in circuit complexity is exponential compared to the increase in input bits hence is usually limited to 4 bit adders.

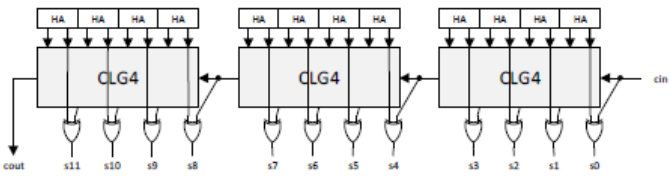

Fig -2: Carry Look Ahead[3]

$Pi=Ai \oplus Bi$

$Gi=Ai.Bi$

$Si=Ci \oplus Ai \oplus Bi$

Where Ai and Bi are the i^{th} input bit, Pi is the propagation term of i^{th} addition, Gi is the generator term of i^{th} addition, Si is the i^{th} Sum, and Ci is the i^{th} carry.

1.4 Carry Select Adder

In this configuration, a multiplexor is used along with small multi-bit adders to create a larger adder. This adder utilizes two adders for the high order bits (one with carry input as '1' and the other with carry input '0') which are connected to MUX inputs. The final carry of the lower adder is used as the control input for the MUX. Depending on the select input, one of the inputs is routed to the output. The advantage of this circuit is that the computation of all the bits takes place simultaneously with the disadvantage being that of the extra circuitry requirement.

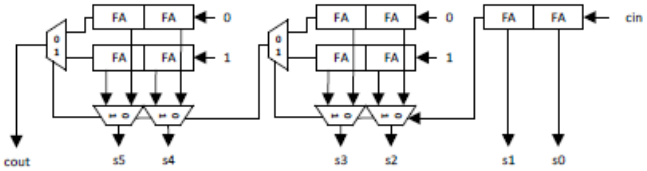

Fig -3: Carry Select Adder[3]

1.5 Pass Transistor

In the pass transistor design, the MOSFET is acting as a voltage controlled switch which passes the logic connected to the drain terminal to its source terminal as shown in figure 4. If the gate voltage Vg is high and input Vd at the gate is high, then the output at the source is obtained as Vs= Vg-Vth where Vs is the output voltage at the source and Vth is the threshold voltage of the MOSFET. If the Vg is low the circuit is off, and the output node is floating. The advantage of pass transistor logic is that the design of circuits is independent of the W/L ratio of transistor and also utilized the least number of MOSFETs of all the design styles. One major disadvantage of pass transistor circuits is that is provides a weak logic '1' as the output voltage drops by one threshold level in each MOSFET making the cascading of transistors a problem. Further pass transistor circuits increase power consumption as there is static power dissipation in the circuits.

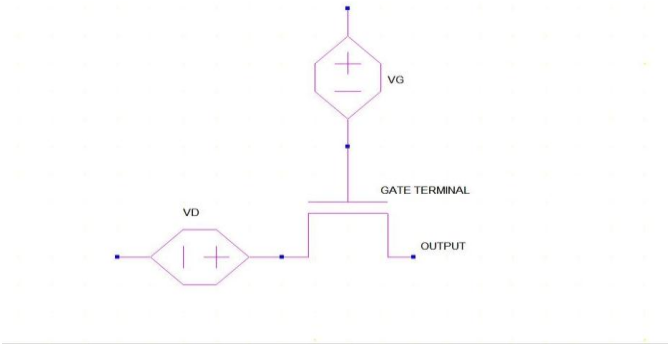

Fig -4: Pass Transistor

1.6 Static CMOS

The Static CMOS Logic is constructed using a PUN and a PDN. The purpose of the PUN is to provide a connection between the output node and the supply voltage when the output of the logic circuit is expected to be high. The PDN connects the output to the ground when the output is expected to be low. The PUN and PDN networks are constructed in a mutually exclusive manner such that either PDN or PUN is conducting in steady state[5]. One of the major advantages of Static CMOS logic is that has zero quiescent power dissipation, where for any applied input state either the PUN or the PDN remains off [5]. The disadvantage of Static CMOS logic is that the creation of two complementary networks results in an increased number of transistors and consequently the area required is higher. Also the capacitance of the circuits is comparatively higher than other design styles which reduces the maximum speed of operation of the circuit.

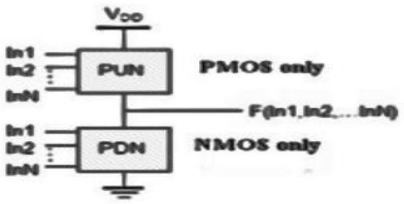

Fig -5: Static CMOS[5]

1.7 Dynamic CMOS

The dynamic logic circuits are constructed using either a PDN consisting of all NMOSs or a PUN consisting of all PMOSs. The transistor Mp called the pre-charge transistor is used to charge the node capacitances to their full value every clock cycle when the clock signal is low. When the clock signal becomes high, the evaluation phase begins during which the input combinations are evaluated to generate the logic gate output. The advantage of dynamic logic circuits is that it requires only transistor network which reduces the area required and improves circuit speed. However, the dynamic logic circuits suffer from the problem of charge sharing and race-around which makes the cascading of two stages complex requiring the use of charge keeper transistors and domino logic or zipper logic to fix these issues.

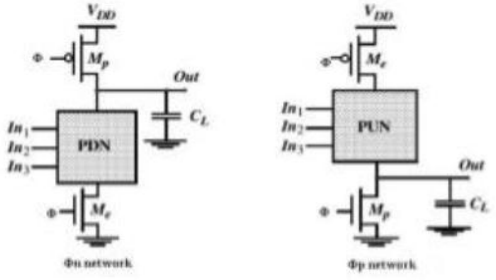

Fig -6: Dynamic CMOS[5]

2. 8 BIT CARRY SELECT ADDER USING 4 BIT CARRY LOOK AHEAD TOPOLOGY

In a standard Carry Select Adder, the lower nibble is added using a 4-bit RCA and the upper nibble is added using 2 parallel 4-bit RCA. This is a kind of fast adder, but still the propagation delay from the first stage remains a problem.

The speed of the adder can be further increased by using another fast adder in place of RCA. The limitation of CLA adder remains that it is only feasible for 4-bit addition. Hence we can use two 4-bit CLA adders in an 8-bit Carry Select Adder, decreasing the delay time of the adder considerably.

CLA generates parallel carry terms for all bit additions hence the delay is minimal. The auxiliary carry bit is given to the control line of a 2:1 MUX to select a circuit that calculated further terms using the corresponding carry in.

The two circuits to simultaneously calculate the higher nibble are exact same circuits with the only difference of the carry in fed to each of them. One of the circuit assumes 0 as carry in and the other as 1. Both the circuits calculate sum and further carry terms on the assumption of initial carry. Either one of these circuits are selected corresponding to the actual carry generated at the first stage via a MUX.

This circuit can be realized using different MOS technologies, such as Pass Transistor, Static CMOS, and Dynamic CMOS. In each of different design style number of transistors used would be different, and the number of stages required to realize the same Boolean equation might vary too.

The following topology of adders was simulated in microwind dsch software.

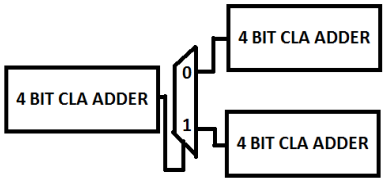

Fig -7: Implemented circuit block diagram

3. SIMULATIONS AND RESULTS

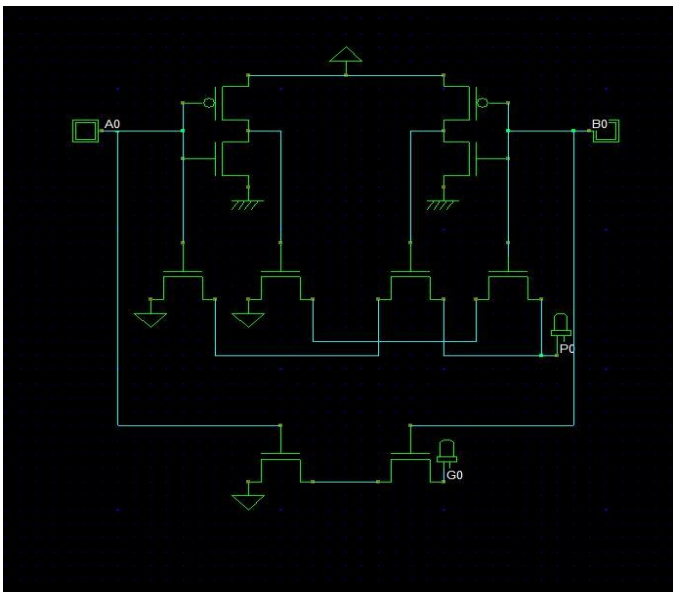

Fig -8: Propagation term and generator term using pass transistor.

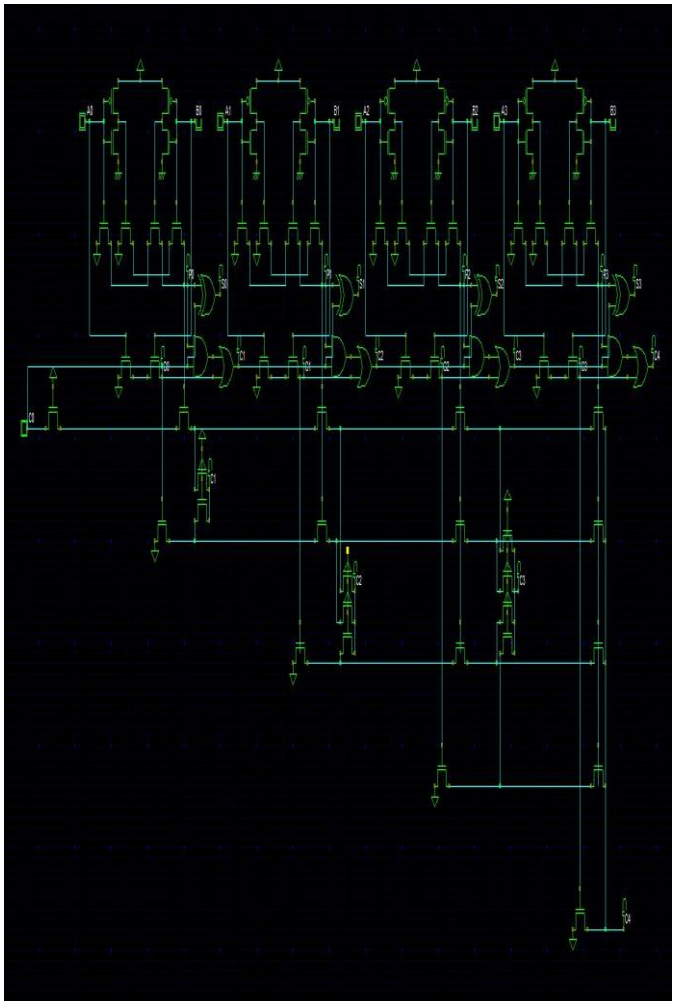

Fig -9: 4-bit CLA Adder using pass transistor

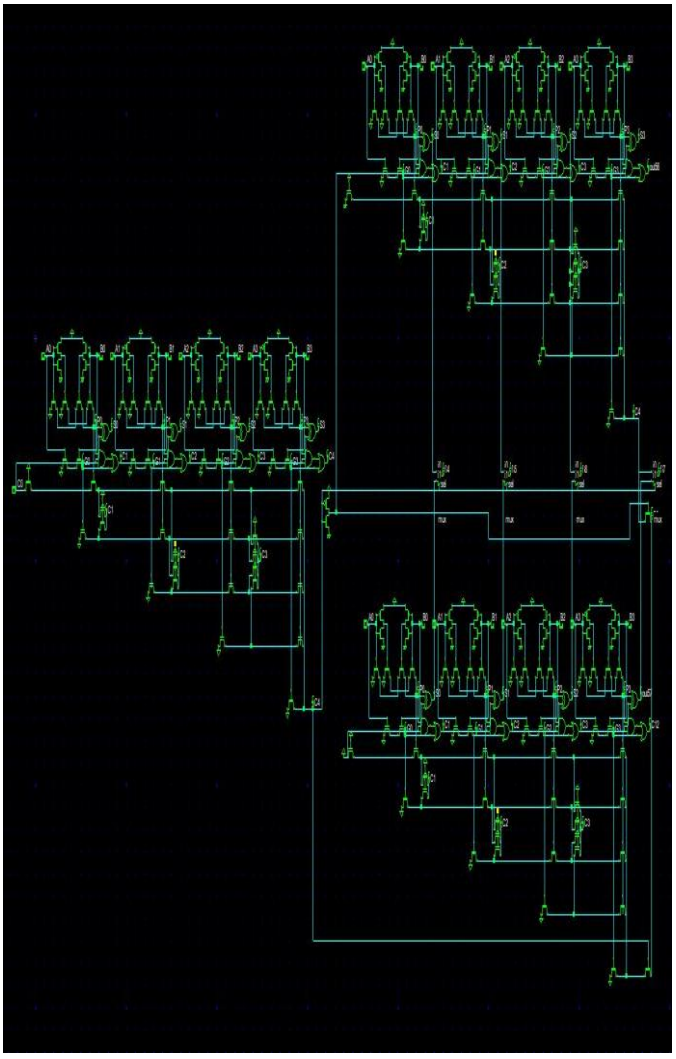

Fig -10: 8-bit Carry Select Adder with 4-bit CLA adder using pass transistor

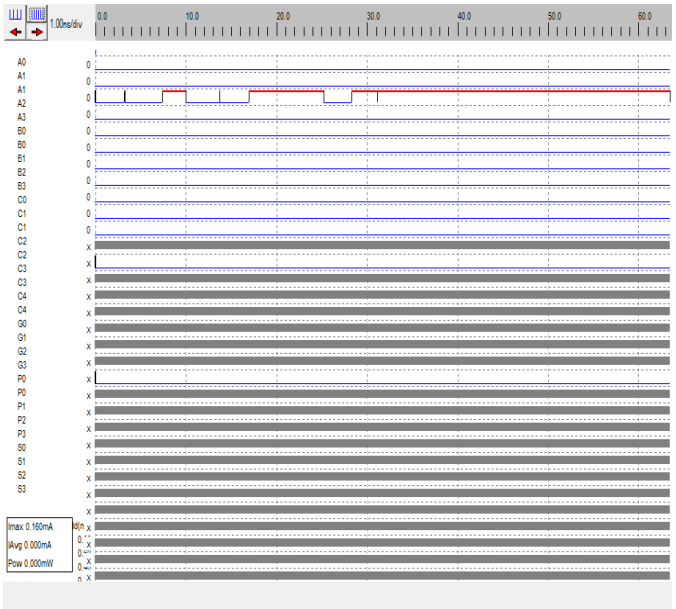

Fig -11:8-bit adder using pass transistor simulation

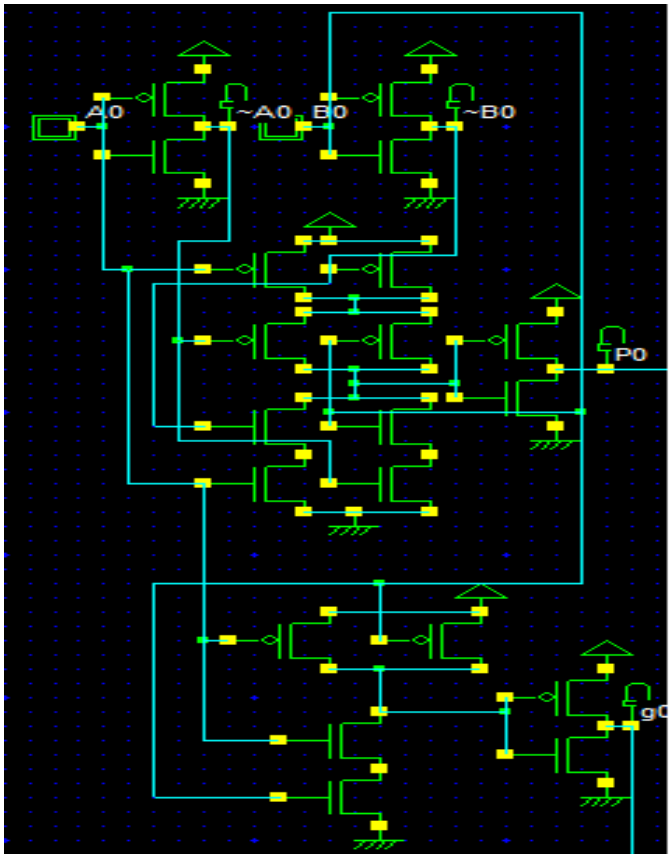

Fig -12: Propagation term and generator term using static CMOS

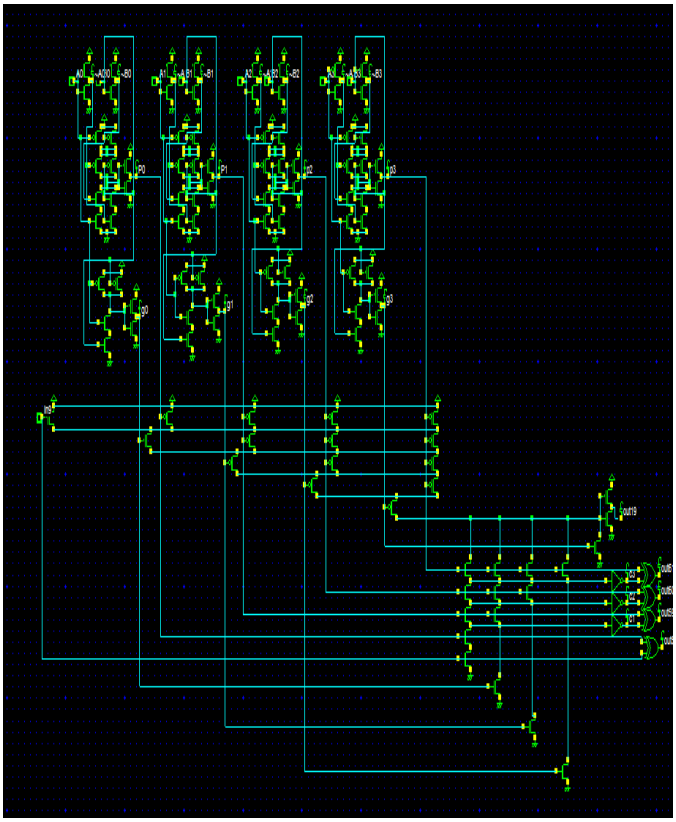

Fig -13: 4-bit CLA Adder using static CMOS

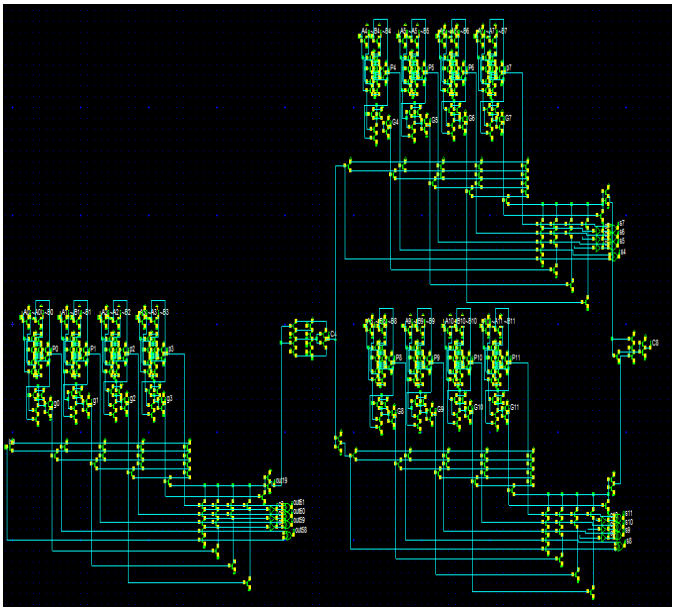

Fig -14: 8-bit Carry Select Adder with 4-bit CLA adder using static CMOS

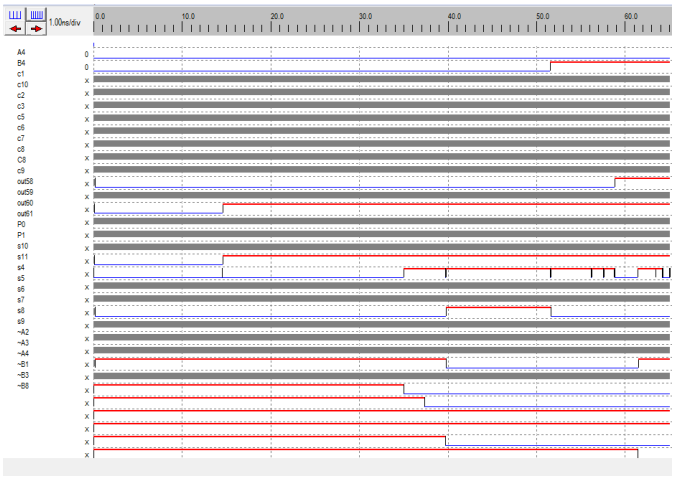

Fig -15: 8-bit adder using static CMOS simulation

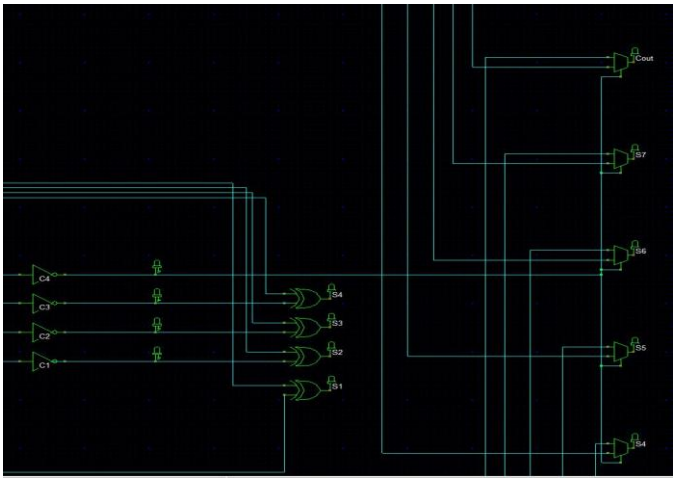

Fig -16: Propagation term and generator term using dynamic CMOS

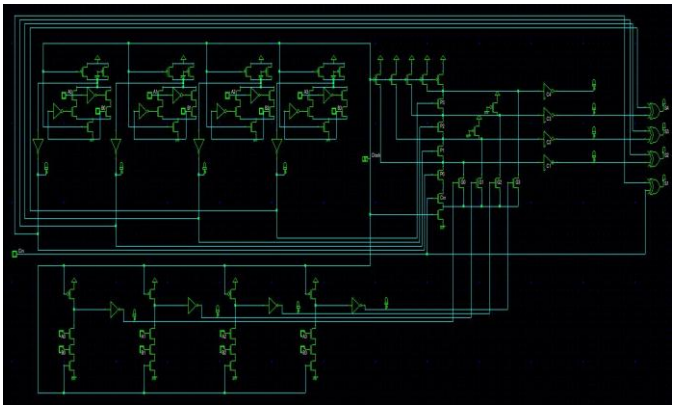

Fig -17: 4-bit CLA Adder using dynamic CMOS

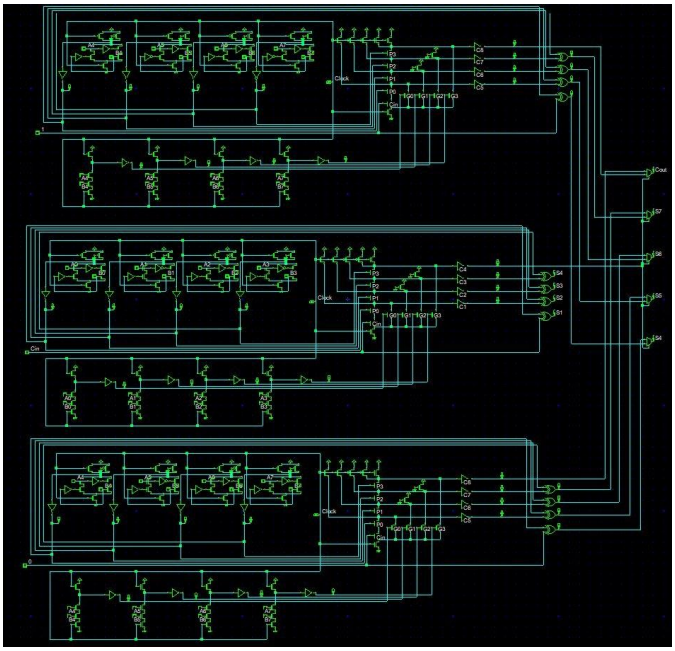

Fig -18: 8-bit Carry Select Adder with 4-bit CLA adder using dynamic CMOS

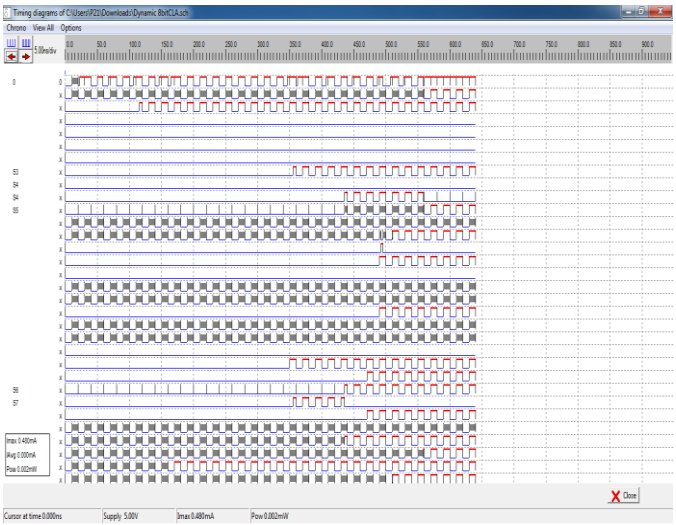

Fig -19: 8-bit adder using dynamic CMOS simulation

3. CONCLUSIONS

Using CLA adder instead of RCA makes the circuit considerably fast. Though due to CLA's limitation of it being feasible only for 4-bit addition, the sub part of Carry Select Adder cannot exceed 4-bits. If one wishes to increase the number of bits the complexity of circuitry would drastically increase.

Pass transistor uses a lot less number of transistors but as the circuit turns to become more and more complex, the voltage passing from the drain becomes weaker in order to overcome the threshold voltage of the MOS transistor.

Using CMOS technology provides ease in fabrication. The static circuit experiences race error which the dynamic circuit overcomes by the use of pre charge circuit.

Design Technology used	NMOS	PMOS	TOTAL
Pass Transistor	171	25	196
Static CMOS	177	177	354
Dynamic CMOS	179	108	287

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