International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 06 Issue: 03 | Mar 2019 www.irjet.net p-ISSN: 2395-0072

AN EFFICIENT VLSI ARCHITECTURE FOR 3D-DWT USING LIFTING SCHEME

P. Kannan[1], I. Asma[2], A. Benasir[3], R. Deepikha[4], R. Divya[5]

[1]Professor, Dept. of ECE, Panimalar Engineering College, Poonamalle, TamilNadu, India.
[2,3,4,5]UG students, Dept. of ECE, Panimalar Engineering College, Poonamalle, TamilNadu, India.

Abstract - Image compression is one of the known techniques in image processing. The modern real time applications related to image processing demands high performance discrete wavelet transform (DWT). Existing techniques like DCT require more complex operations and also needs increased hardware resources. Compared to DCT, DWT has better compression results due to lossless compression .In DWT there are two techniques ,they are convolution and lifting scheme .The lifting scheme represents the fastest implementation of the DWT than the convolution based DWT. Hence lifting scheme is considered. The proposed 3D-DWT achieves reduction in total area and net power as compared with existing convolution DWT and DCT. The major objective of this work is to improve the performance of the DWT for DSP applications.

1. INTRODUCTION

Nowadays, from satellite images to medical diagnosis images are stored on our computers. To get these images on the computer they must be transmitted over phone lines or other cables. When the images are larger it takes longer compression time and higher storage space. A common characteristic of most images is that the neighboring pixels are correlated and therefore contain redundant information. Hence in order to remove that redundant information we have to detect less correlated pixels representation of the image. The two main components involved in compression are redundancy and irrelevancy reduction. In order to decrease the redundant information we can eliminate duplication from an image or a video. The reduction in irrelevancy eliminates the part of the image or video that will not be noticed by the signal receiver, namely the Human Visual System (HVS).

1.1 Redundant Techniques

Thus compression is obtained after removing one or more of three basic data redundancies: (1) Coding redundancy, that are present only when code words used are less than optimal; (2) Interpixel redundancy, that occurs as a result of correlations between the pixels of an image; (3) psychovisual redundancy which is due to the data that is ignored by the human visual system. For many years, artificial neural networks (ANNs) have been studied and used to model information processing systems based on or inspired by biological neural structures. The artificial neural network results with solutions whose performance is better than that of traditional problem-solving methods, and also provides a clear understanding of human cognitive abilities.

Kohonen's self-organizing map (SOM) is one of the most popular neural network models. This is mainly introduced for an associative memory model which is one of the unsupervised learning algorithms with a simple structure and computational form. Self-organization is a fundamental pattern recognition process. In self-organization, intrinsic inter- and intra-pattern relationships among the stimuli and responses are learned without the presence of a potentially biased or subjective external influence. The SOM is mainly used to provide topologically preserved mapping of input and output spaces [1, 2]. The SOM is optimal for vector quantization. The property of SOM, that provides the topographical order mapping with enhanced fault- and noise-tolerant abilities.

1.2 Proposed algorithm

In turn SOM is also applicable to various other applications, like reducing dimensionality, data visualization, clustering and classification. Many other extensions of the SOM are also devised to extend the mapping as an effective solution for a wide range of applications. Wavelet transform is the only method that provides both spatial and frequency domain information. The properties of wavelet transform gently helps in identification and selection of significant and non-significant coefficients among the wavelet coefficients. Image compression based on wavelet transform results in an improved compression ratio as well as image quality and thus both the significant coefficients and their positions within an image are encoded and transmitted. In this paper, a wavelet based image compression is applied to the result of the SOM based vector quantization.

With the rapid progress of VLSI design technologies, many processors based on audio and image signal processing have been developed recently. The discrete wavelet transform plays a major role in the JPEG-2000 image compression standard. The Discrete Wavelet Transform (DWT) has become a very versatile signal processing tool. The advantage of DWT over other traditional transformations is that it performs multi resolution analysis of signals with localization both in time and frequency. In addition to audio and image compression, the DWT has important applications in many areas, such as computer graphics, numerical analysis, radar target

distinguishing and so forth. Discrete wavelet transform (DWT) has been widely used in many multimedia applications including video coding and various signal processing applications.

2. LITERATURE SURVEY

2.1 "Efficient Architectures for Two-Dimensional Discrete Wavelet Transform Using Lifting Scheme" by "Chengyi Xiong, Jinwen Tian, and Jian Liu"

Novel architectures for 1-D and 2-D discrete wavelet transform (DWT) using lifting schemes are presented in this paper. An embedded decimation technique is exploited to optimize the architecture for 1-D DWT, which is designed to receive an input and generate an output with the low- and high-frequency components of original data being available alternately. Based on this 1-D DWT architecture, an efficient line-based architecture for 2-D DWT is further proposed by employing parallel and pipeline techniques with 100 percentage hardware utilization. Moreover, another efficient generic line-based 2-D architecture is proposed by exploiting the parallelism among four sub band transforms in lifting-based 2-D DWT, hence it is called high-speed architecture. The throughput rate of the latter is increased by two times when comparing with the former 2-D architecture, but only less additional hardware cost is added. Compared with the works reported in previous literature, the proposed architectures for 2-D DWT are efficient alternatives in tradeoff among hardware cost, throughput rate, output latency and control complexity, etc.

2.2 "An Efficient Hardware-Based Higher Radix Floating Point MAC Design" by "MOHAMED ASAN BASIRI M and NOOR MAHAMMAD SK"

This article proposes an effective way of implementing a multiply accumulate circuit (MAC) for high-speed floating point arithmetic operations. The real-world applications related to digital signal processing and the like demand high-performance computation with greater accuracy. Thus, the separate accumulation circuit can be avoided by keeping the circuit depth still within the bounds of the **Wallace tree multiplier** or **Braun multiplier**. In this article, three kinds of floating point MACs are proposed. The experimental results show improvement in worst path delay achieved by the proposed floating point MAC using a **radix-2 Wallace structure** compared with a conventional floating point MAC without a pipeline. The performance results show comparisons between the proposed floating point MAC with various floating point MAC designs for radix-2,-4,-8, and -16. The proposed design has lesser depth than a conventional floating point MAC as well as a lower area requirement than other ways of floating point MAC implementation, both with or without a pipeline.

2.3 "Area-Efficient and Power-Efficient Architecture for High-Throughput Implementation of Lifting 2-D DWT" by " Basant K. Mohanty, Senior Member, IEEE, Anurag Mahajan, and Pramod K. Meher, Senior Member, IEEE"(2012)

We have suggested a new data-access scheme for the computation of lifting two-dimensional (2-D) discrete wavelet transform (DWT) without using data transposition. We have derived a linear systolic array directly from the dependence graph (DG) and a 2-D systolic array from a suitably segmented DG for parallel and pipeline implementation of 1-D DWT. These two systolic arrays are used as building blocks to derive the proposed transposition-free structure for lifting 2-D DWT. The proposed structure requires only a small on-chip memory of words and processes a block of P samples in every cycle, where N is the image width. Moreover, it has small output latency of nine cycles and does not require control signals which are commonly used in most of the existing DWT structures.

2.4 "Image Compression Based upon Wavelet Transform and a Statistical Threshold by "Ahmed A. Nashat, N" and "M. Hussain Hassan" (2016)

Discrete Wavelet Transform, (DWT), is known to be one of the best compression techniques. It provides a mathematical way of encoding information in such a way that it is layered according to level of detail. In this paper, we used **Haar wavelets** as the basis of transformation functions. Haar wavelet transformation is composed of a sequence of low pass and high pass filters, known as filter bank. The redundancy of the DWT detail coefficients is reduced through thresholding and further through Huffman encoding. The proposed threshold algorithm is based upon the statistics of the DWT coefficients. The quality of the compressed images has been evaluated using some factors like Compression Ratio (CR) and Peak Signal to Noise Ratio (PSNR). Experimental results demonstrate that the proposed technique provides sufficient higher compression ratio compared to other compression thresholding techniques.

2.5 "Review of image compression techniques "by "Abhipriya Singh K.G. Kirar" (2017)

Demand of multimedia growth, contributes to insufficient bandwidth of network and memory storage device. Therefore data compression is more required for reducing data redundancy to save more hardware space and transmission bandwidth. Image compression is one of the main researches in the field of image processing. Many techniques are given for image compression. Some of which are discussed in this paper. This paper discusses **'k'** means clustering, 2D-DWT and fuzzy logic based image compression.

3. LIFTING SCHEME

This paper proposes the 3D- DWT using lifting scheme. The lifting scheme entirely relies on the spatial domain, has many advantages compared to filter bank structure, such as lower area, power consumption and computational complexity. The lifting scheme can be easily implemented by hardware due to its significantly reduced computations. Lifting has other advantages, such as "in-place" computation of the DWT, integer-to-integer wavelet transforms which are useful for lossless coding.

3.1 LIFTING ALGORITHM

In image processing, DWT can be used in image compression, image reconstruction, image coding, and Image fusion. In general, VLSI architecture for DWT is classified into two categories, they are

- Convolution based and
- Lifting based.

Wim Sweldens developed a lifting scheme for the construction of bi-orthogonal wavelets. The main feature of the lifting scheme is that all constructions are derived in the spatial domain. Lifting scheme is a simple and an efficient algorithm to calculate wavelet transforms as a sequence of lifting steps. Constructing wavelets using lifting scheme comprises three steps:

Step 1:

- Split Samples: The original signal, input image X (n), is split into odd and even samples.

Step 2:

- Lifting: This step is executed as N sub steps depending on the type of the filter, where the odd and even samples are filtered by the prediction and update filters, p (z) and u (z).

Step 3:

- Normalization or Scaling : After N lifting steps, scaling coefficients K and 1/K are applied respectively to the odd and even samples in order to obtain the low pass sub band i.e. significance coefficient YL (i) and the high-pass sub band i.e. detailed coefficient YH (i).

The proposed work is specialized for the DWT 5/3 wavelet in lifting scheme implementation. 'X' be the input image, which has predefined pixels.

Let, X = [X (1), X (2) ... X (2n)] be an array of length 2n.

In this work we begin with the **"poly-phase decomposition"** splitting *X into two sub-bands, each of length N. The* original signal i.e. input image pixels are split into even and odd pixels in split step of the design.

Xo = [X (1), X (3), X (5)... X (2n-1)]

Xe = [X (2), X (4), X (6) ... X (2n)]

There are four stages in the lifting scheme architecture which is summarized by the equations as follows:

$P1(n) = Xo(n) + a\,(Xe(n) + Xe(n+1))$

$U1(n) = Xe(n) + b\,(P1(n) + Xe(n+1))$

$d_c(n) = k * P1(n)$

$S_c(n) = 1/k * U1(n)$

P1 (n) and U1 (n) are scaled by the constant K and K-1 respectively, for normalizing their magnitude. Filter coefficients are described in table 1. The inverse transform is done by performing the lifting steps in the reverse order and with a, b and k negated.

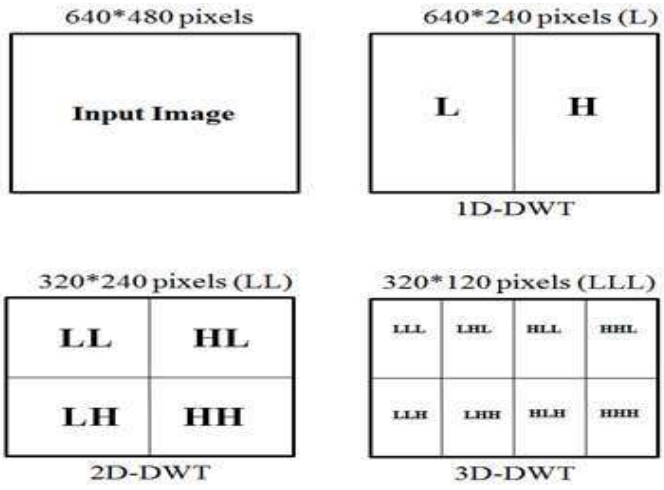


Fig-3.1.1: Block diagram of Lifting Scheme

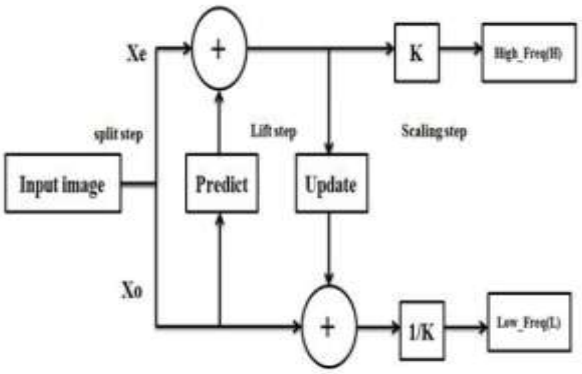


Fig-3.1.2: Forward Lifting Scheme

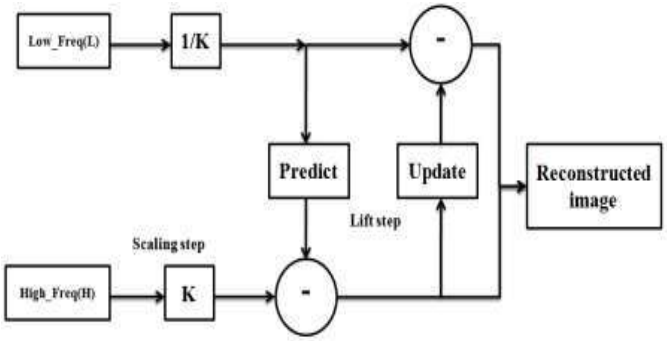


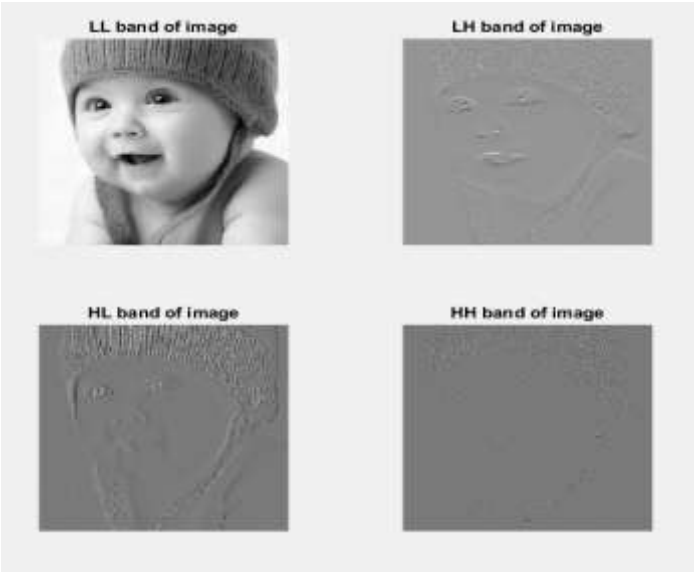
Fig-3.1.3: Backward Lifting Scheme

4. STAGES OF COMPRESSION

4.1 INPUT IMAGE

4.2 1D-DWT

4.3 2D AND 3D-DWT



5. RESULTS

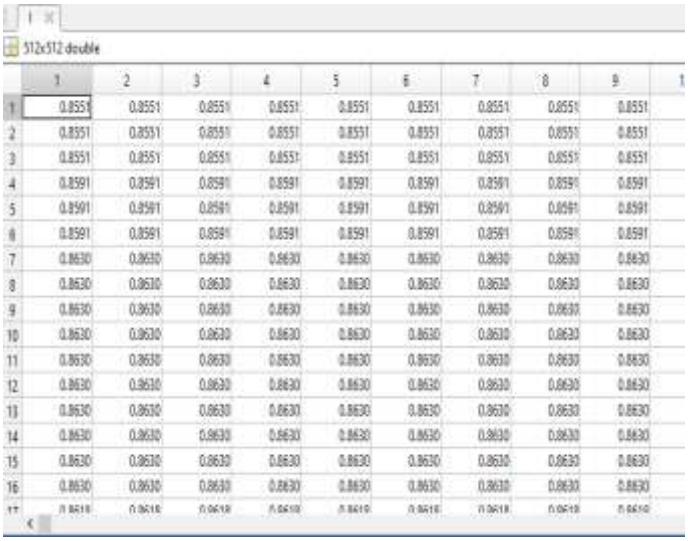
5.1 AREA-ANALYSIS

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	1408	5720	24%
Number of fully used LUT-FF pairs	0	1408	0%
Number of bonded IOBs	880	102	862%

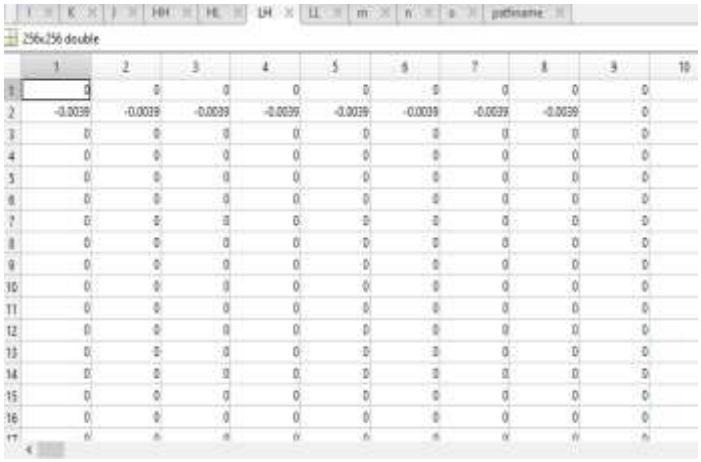
5.2 DWT LIFTING TIMING REPORT (DELAY)

```
Timing Summary:
---------------
Speed Grade: -3

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 10.069ns

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 154176070 / 480
-------------------------------------------------------------------------
Delay:              10.069ns (Levels of Logic = 32)
  Source:           x0<0> (PAD)
  Destination:      e22<31> (PAD)
```

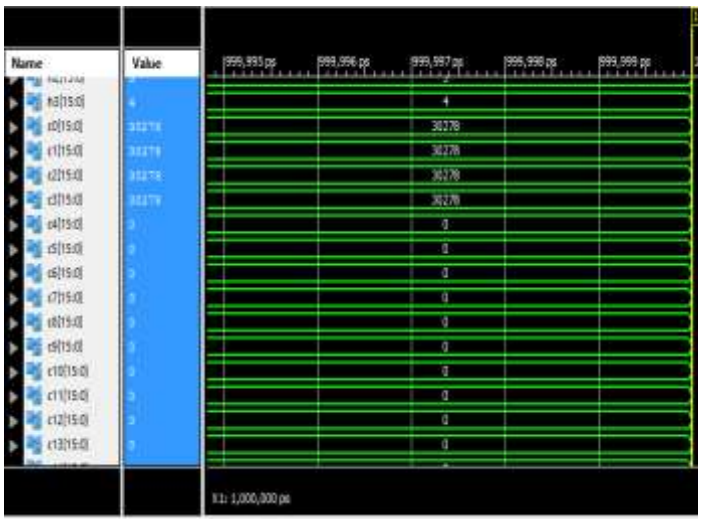
5.3 MATRI X OF PIXELS BEFORE IMAGE COMPRESSION



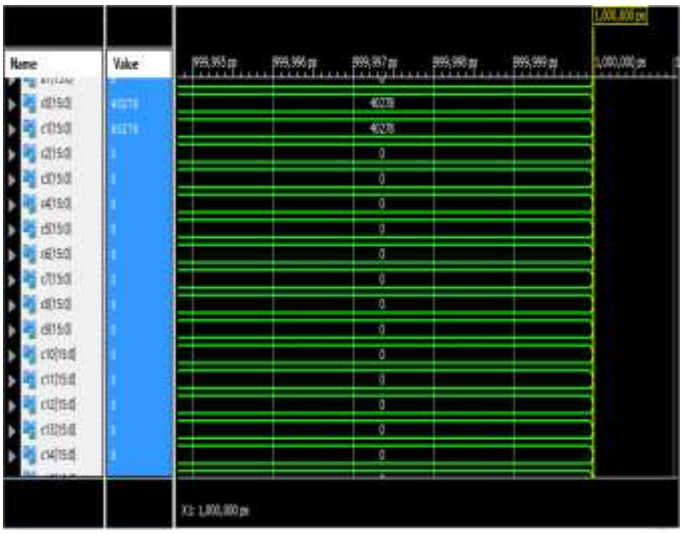
5.4 MATRIX OF PIXELS AFTER IMAGE COMPRESSION



5.5 DWT-CONVOLUTIONAL OUTPUT



5.6 DWT-LIFTING OUTPUT



5.7 FPGA OUTPUT

6. ADVANTAGES

- Integer-to-integer wavelet transforms which are useful for lossless coding.
- Better Compression Performance.
- Computation Performance is good.
- Less area and delay.
- In image processing, DWT can be used in Image compression , Image coding, Image fusion and Image reconstruction.

7. CONCLUSION

In this Project, Efficient VLSI architecture for convolution based folded 1D/2D-DWTs are proposed. This project proposes the floating point MAC based 1D/2D-DWT,

where the low/high pass FIR filter outputs are found using a MAC and high performance VLSI architecture for discrete wavelet transform (DWT) is proposed that are used in real time high efficiency video coding (HEVC) applications. The proposed 1D architecture is used to design 2D folded and parallel designs. The performance results show that the proposed architecture gives good improvement as compared with existing architecture.

8. REFERENCES

[1] Po-Cheng Wu and Liang-Gee Chen, "AN EFFICIENT ARCHITECTURE FOR TWO-DIMENSIONAL DISCRETE WAVELET TRANSFORM", IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11 (4), 536-545.

[2] Chu Yu and Sao-Jie Chen, "VLSI Implementation of 2-D Discrete Wavelet Transform for Real-time Video Signal Processing", IEEE Transactions on Consumer Electronics, 1997, 43 (4), pp. 1270-1279.

[3] Frances comaria Marino, "Efficient High-Speed/Low-Power Pipelined Architecture for the Direct 2-D Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing, 2000, 47 (12), pp. 1476-1491.

[4] Tinku Acharya and Chaitali Chakrabarti, "A Survey on Lifting-based Discrete Wavelet Transform Architectures", Journal of VLSI Signal Processing, 2005, 42, pp. 321-339.

[5] Liu Hong-jin, Shao Yang, He Xing, Zhang Tie-jun, Wang Dong-hui and Hou Chao-huan, "A Novel VLSI Architecture for 2-D Discrete Wavelet Transform", IEEE International Conference on ASIC, Oct. 2007, pp.40-43.

[6] Guangming Shi, Weifeng Liu, Li Zhang, and Fu Lii, "An Efficient Folded Architecture for Lifting-Based Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems-II: Express Briefs, 200956 (4), pp. 290-294.

[7] Chengyi Xiong, Jinwen Tian, and Jian Liu, "Efficient Architectures for Two-Dimensional Discrete Wavelet Transform Using Lifting Scheme" ,IEEE Transactions on Image Processing, 2007, 16 (3), pp. 607-614.

[8] Chih-Hsien Hsia, Jen-Shiun Chiang, Member, and Jing-Ming Guo "Memory-Efficient Hardware Architecture of 2-D Dual-Mode Lifting-Based Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems for Video Technology, 2013, 23 (4), pp. 671-683.