A NOVEL DESIGN OF FLIP FLOP AND ITS APPLICATION IN UP COUNTER

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Abstract - *As CMOS technology has a scaling limitation in deep nanometre technologies, the best alternative for CMOS technology is a Quantum – Dot Cellular Automata (QCA) technology. The QCA technology has many advantages than transistor based technology such as small size, high speed and low power consumption. In conventional CMOS technology, transistors are used to create a logic gate. But in QCA technology, QCA cells are used to create logic gates and wire. The basic logic elements are an inverter and the majority gate. By using these elements many of the combinational and sequential circuits are created. In this brief, we design the binary up counter using JK, SR, D and T flip flop. 4 bit up Counters are implemented using the above mentioned QCA technology. Thus we propose a dual edge triggered Flip-flops based 4-bit up counter. The layout was designed and the functionality of the counter circuit was verified using QCADesigner tool.*

***Key Words*: Quantum – Dot cellular Automata, CMOS, flip-flops, counter.**

1. INTRODUCTION

QUANTUM dot cellular automata (QCA) is one of the emerging technologies that shows features to overcome the limitations like high computation throughput and power consumption faced in CMOS technologies. A lot of research has been done in designing universal logic gates, combinational circuits, sequential circuits and ALU using QCA and has shown its efficiency due to its small size and high computational speed. Apart from these advantages of QCA, it also has a great potential for low power consumption.

Among several other alternatives, Quantum Dot Cellular Automata (QCA) is a revolutionary promising transistor less quantum paradigm that performs computation and routing information at Nano domain. The unique feature of QCA is that logic states are represented by a cell. A cell is a Nano scale device capable of transferring data by two state electron configurations.

Alternatives to conventional CMOS technology is QCA which provides higher density, lower dissipation of power, higher clock frequency and better output results are needed. Quantum Dot Cellular Automata (QCA) technology is explored and introduced. When a new technology is introduced, new design principles are also necessary to consider. The design nature of QCA is not very complicated, instead it is simple than the conventional technologies.

1.1 EXISTING SYSTEM

The term CMOS stands for "Complementary Metal Oxide Semiconductor". CMOS technology is one of the most popular technology in the computer chip design industry and broadly used today to form integrated circuits in numerous and varied applications. Today's computer memories, CPUs and cell phones make use of this technology due to several key advantages. This technology makes use of both P channel and N channel semiconductor devices. One of the most popular MOSFET technologies available today is the Complementary MOS or CMOS technology. This is the dominant semiconductor technology for microprocessors, microcontroller chips, memories like RAM, ROM, EEPROM and application specific integrated circuits (ASICs).

2. CMOS WORKING PRINCIPLE

In CMOS technology, both N-type and P-type transistors are used to design logic functions. The same signal which turns ON a transistor of one type is used to turn OFF a transistor of the other type. This characteristic allows the design of logic devices using only simple switches, without the need for a pull-up resistor.

In CMOS logic gates a collection of n-type MOSFETs is arranged in a pull-down network between the output and the low voltage power supply rail (Vss or quite often ground). Instead of the load resistor of NMOS logic gates, CMOS logic gates have a collection of p-type MOSFETs in a pull-up network between the output and the higher-voltage rail (often named Vdd).

Thus, if both a p-type and n-type transistor have their gates connected to the same input, the p-type MOSFET will be ON when the n-type MOSFET is OFF, and vice-versa. The networks are arranged such that one is ON and the other OFF for any input pattern. CMOS offers relatively high speed, low power dissipation, high noise margins in both states, and will operate over a wide range of source and input voltages.

3. PROPOSED SYSTEM

QCA is a novel emerging technology in which logic states are not stored as voltage levels, but rather the position of individual electrons. Conceptually, QCA represents binary information by utilizing a bi-stable charge configuration rather than a current switch. Unlike conventional logic circuits in which information is transferred by electrical current, QCA operates by the Columbic interaction that connects the state of one cell to the state of its neighbors. Hence the information transfer (interconnection) is the same

as information transformation (logic manipulation) in the QCA technology.

The QCA cell in contrast to electronics based on transistors, QCA does not operate by the transport of electrons, but by the adjustment of electrons in a small limited area of only a few square nanometers. QCA is implemented by quadratic cells, the so-called QCA cells. In these squares, exactly four potential wells are located, one in each corner of the QCA cell. In the QCA cells, exactly two electrons are locked in. They can only reside in the potential wells. The potential wells are connected with electron tunnel junctions.

There are two diagonals in a square, which means the electrons can reside in exactly two possible adjustments in the QCA cell. Regarding these two arrangements, they are interpreted as a binary '0' and binary '1', i.e. each cell can be in two states. The state '0' and the state '1', as shown in figure 3. A binary system is something familiar, as Boolean logic is used already in today's computers. There, a high voltage is often interpreted as binary '1' and a low voltage as binary '0'.
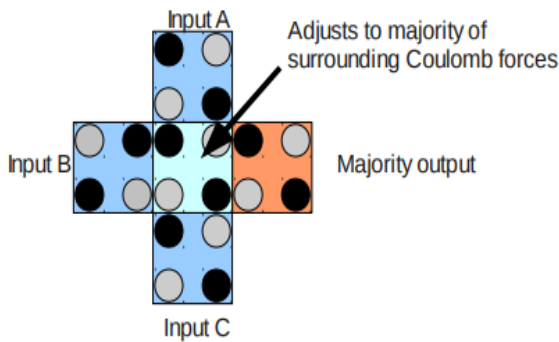
3.1 QCA MAJORITY GATE

Fig-1: QCA majority gate

From physics, it is know that the Coulomb forces of several electrons sum up. The majority voter takes advantage of this effect. The cells on top, at the left and at the bottom work as input cells. As the Coulomb forces of the electrons of all input cells sum up, the middle cell adjusts to the majority of adjustments of the input connection cells. Finally the output cell adjusts to the middle cell and the resulting state of the majority vote can be obtained from the output cell.

3.2. QCA CLOCK ZONES

To avoid the input and output lagging problem, we generally use clock signal to add delay. The clock guides the flow of input to the cell and execution. In contrast to transistor-based circuits, one clock cycle consists of four clock signals, which are delayed by ¼ of the whole clock cycle among each other, as depicted in figure 2.
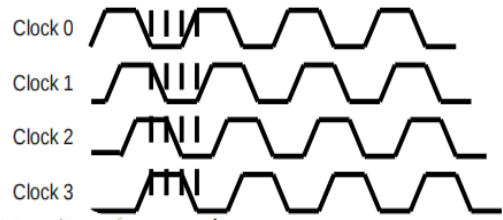

Fig-2: The four shifted clock signals

The figures in this chapter will always show clock zones like clock 0, clock 1 and so on. This is for convenience of course you can also read it as clock n, clock n+1, clock n+2. Important is, that particular groups of QCA cells are in different clock zones. When the clock signal is high, it opens the electron tunnel junctions in QCA cells. Opened tunnel junctions allow the two electrons in a QCA cell to travel between potential wells

4. QCA DESIGN

Depending on the surrounding Coulomb forces around the QCA cell, the electrons will travel to respective potential wells. In this implementation a careful consideration is taken into account, to increase the device stability. This implementation also reduces the number of cells. It has been reduced by suitable arrangement of cells without overlapping of neighbouring cells and by using 2 cells inverter. Hence this implementation further reduces the area and complexity.

4.1 SR FLIP-FLOP

The S-R flip-flop has two inputs namely, SET(S) and RESET(R), and two outputs Q and Q-bar which are complement to each other. The clock pulse input acts as an enable input to the other two inputs S and R.
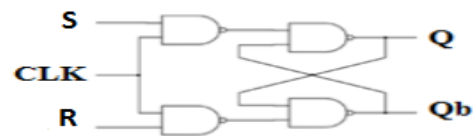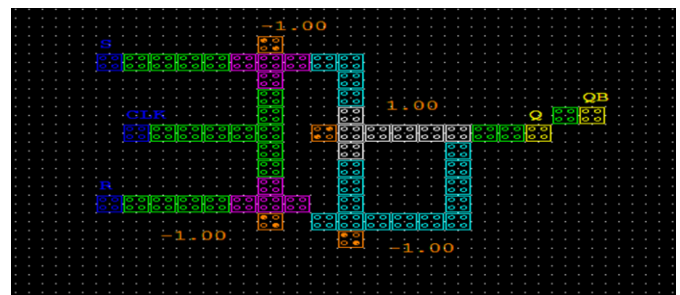

Fig-3: SR flip-flop using NAND gate

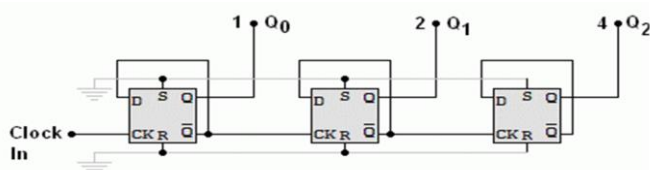**Fig-4:** Design of SR flip-flop in QCA

5. CONCLUSION

By the above design process we have designed the flip flops in QCA Designer tool and obtained the power dissipation of the flip flop designs. Using this power and the power obtained from the CMOS design is compared. From this, we could obtain a great power difference of flip flop over the CMOS technology. By this complexity also reduced. And so the time taken for the process gets reduced. Many other logical and combinational circuits can be designed using this as a base. The flip flops and counters are designed and the results are verified has been shown in this paper.

Table -1: Comparison of power between CMOS and QCA

DESCRIPTION	CMOS LOGIC	QCA LOGIC
SR flip-flop	6.46 e^0.002 watts	2.46 e^0.002 watts
JK flip-flop	7.85 e^0.002 watts	2.18 e^0.002 watts
D flip-flop	4.32 e^0.002 watts	4.10 e^0.002 watts
T flip-flop	5.22 e^0.002 watts	4.87 e^0.002 watts

6. APPLICATION

SR flip flop up counter is designed by using three flip flops connected in series. So by using the flip flop design of SR the counters is made by giving a wire connection from one flip flop to another based on basic circuit of counter.

Fig-5: SR flip-flop counter
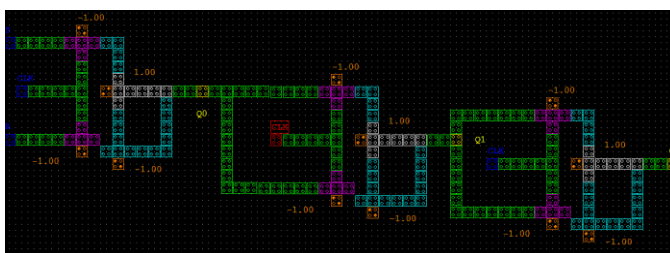
Fig-6: Design of SR flip-flop counter in QCA

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