Literature Survey on Hardware Addition and Subtraction

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Abstract:- *The integration of number of processor cores into one chip is increasing due to increase in the demand of enhancing the ability of processor to handle the more complex and challenging processor. All microprocessors consists of arithmetic operations and logical operations. To develop the more powerful and smaller computer. Arithmetic logical unit is made smaller and more complex. IC fabrication technology designer cost and productivity slow down and more complex IC chip due to some limiting factors. Parameters like low power dissipation, small area and low cost are concerned in past. But now speed considerations are now gaining attention with VLSI design.*

Key words:

LSB, Control unit, Reversible gates, CMOS, adder, logical unit.

Introduction:

In digital system design arithmetic logical unit is very important design. In computer processor an arithmetic logic unit is an integral part. Various bit widths are used frequently in very large scale integrated circuits for arithmetic logical units.

To develop more powerful and smaller computer arithmetic logical unit is getting smaller and more complex. Expanding computer and signal processing applications result in increasing the demand for low power and high speed processing. To achieve desired performance in many real time signal higher throughput operations are required. The key arithmetic operations are addition, subtraction, division and multiplication. To reduce power dissipation reversible logic are used and it is required in low power digital design.

A reversible logic gate is one to one mapping device with n-input and n-output. The outputs from inputs and inputs from outputs can be determined easily. To make number of inputs equal to number of outputs extra inputs and outputs are added. Using minimum number of reversible gates, reversible circuits can be designed. The reversible logic units are constructed under two main constraints. They are i) fan out is not permitted ii)loops or feedback are not permitted.

Reversible circuits are particularly for CMOS VLSI design.

Literature survey:

Computation automatically. Speed while dissipation. Intermediate results by retracing. Three tape turning machine. Physical example of reverse computation. Logically reversible. Simplicity and general computations. Irreversible. Single valued inverse .Only the preferred data will get output not other[1]. Carry-look-ahead for more than two decades. Includes the neighbouring pairs. Decreases component count. Fewer logic level. Astonishingly uniform loading. Bit pair truth table is used. Not in critical path. Only for two bit pairs.8 terms as compared. Contains 15 terms [2]. Binary adders. Carry look ahead adder. Carry propagation. High speed addition. Faster. Less expensive. Composite term. Only for 2 bit adder. Recurrence relation. Proximity[3]. Semi automatic chip floor plan algorithm. Initial block placement by attractive and repulsive force. Gradually moving and reshaping blocks. Manual optimization process. Decreases design effort. Color. Design automation. Un defined design language.10k-gate CPU is used[4]. Add and sub of 30 bit number.20 fraction bits in logarithmic system.275 less memory. Linear approximation Non-linear in some regions. Variable size regions are used for approximation. Difficulty in performance. Restricted to 8 to 12 bits. Require 70 mb of ROM[5].

Add/sub. Parallel operations. Algebraically verified. Normalization Rounding and rounding stages. Renormalization is not required. Performance improvement. Cost effective. High speed adder for increment. Increasing execution time. Occupies large amount of chip area [6]. Two thermometer coded words having most significant. Reconstruction. Shift right process in proper

thermometer code. Borrowing condition exists. LSB subtraction is translated. Decreases prior signal processing. Circuitry for determining the LSB. Only gives output for 2 input. Most technical [7]. Perform main prime field arithmetic operations. Considerable improvement. Requires fewer clock cycles. Can perform 256 bit prime. Fastest. Can perform many different operations.Critical path delay. Uses particular comprises. Requires high no. of clock cycles[8]. Novel add/sub AU. Unsigned, sign-magnitude. Reconfigurable technology in from of run-time. 40% of hardware resources are shaped. Classical adder organizations. Throughput of 82.6 mops. Equivalent area-time. Not capable of expressing exactly. Delays due to software. Typically 100 to 1000 times slower [9]. Reduced power dissipation. Low power digital design. Wide applications. Optimized reversible BCD adder. Shows in terms of gates. Quantum cost. Built for Lost information cannot be recovered. Irreversible hardware results in energy dissipation[10].

Reversible programming logic array. Effective cost. Boolean functions also be reversible. Improvement in the quantum cost. Low power re configurable computing hardware. Approach to design low power digital system.Garbage output. Perform only RLPA for 3 inputs. Used a mux and Feynman gate to develop. Dissipation of heat takes place [11]. Reduce power dissipation. Information bits are not destroyed. High power optimization. Parallel adder. Low garbage output. Results in terms of no. of gates.No. of constant inputs. Quantum cost. Gate count is lesser. Low power applications. Fully reversible architecture. Reversible memory[12]. Application specific integrated circuits. Using 90 nm CMOS technology. Created using verilog code. Simulated using micro wind 3.1 to analyze. Consumed 0.60 mw power. Decimal addition takes place. Easy. Causes approximation errors. Uses only 4 bits. Require 00 bits for representation [13].4*4 reversible logic gates are used. Minimal delay. Configured to produce a variety of logical calculations. Fixed outputs based on inputs. Quantitatively analyzed. Quantum cost. Reduced delay and power. Reversible operation is application. Power dissipation occurs. Complexity of circuit [14]. Integration of no. of processor into one chip. Process is not less in system. Performs ALU. To get powerful and smaller computer. Design of 4-bit ALU chip. Computations are done in parallel. Simply select required output. CMOS technology is about 120 mw. Power reduction is 34.34%.High power consumption[15].

Decrease quantum cost.Depth of circuits.Control unit is efficient.Optimized realization of ALU.1-bit ALU.DKFG reversible gate.Full adder.Can design fully reversible.Reversible ALU will be central unit[16].Comprises combinational logic. Implements logical operations. A pad frame is designed. Subsequent rules checks. Design using spice code. Fabrication or extended to make a newer system. Will not have physical example.[17].Parallel prefix address.DSP applications. Better latency performance. Less-power features. Competitive latency. Fully parallel. Carrier free. Delay of parallel prefix. Delay of 16-bit reversible. Only for high speed applications [18].Power dissipation. Reversible logic. Quantum computing. Minimal heat generation. Microprocessor used in ALU. Irreversible arithmetic and logic unit. Consumes less area. Effective quantum computing. Applicability of moore's law. Unavoidable energy penality.Less constant input.[19].fast and efficient processing parts. Low power.n-bit arithmetic circuit. Circuit application. Digital computing. Major processing applications.　High performance. Reversible logic approach. Optimizes parameters. Only low loss digital design applications[20].

Addition and subtraction using generic algorithm. ALU module divided into sub modules. Top down approach used for two inputs. More precise quantity value. Operation of single precision. Achieve higher accuracy. Lesser area[21].Low power. Area effective design. Using GDI technique. Optimize ALU using conventional CMOS .Increases no. of transfers. Optimize the area of ALU. Increase working speed. Uses more no. of transistor. High input load. Larger silicon area[22]. Effectiveness of digital circuits. quantum cost.no. of constant inputs. power utilization. Reversible computing one to one mapping. Input vectors from output vectors. Heat dissipation. Fan out not allowed in reversible circuits[23].Financial and commercial applications use. Hardware support for decimal arithmetic. A reduced delay binary coded decimal adder. Increases parallelism. Area and delay compressed. Synthesized using 0.81 micro TSMC.64-bit addition also takes place. Typically at-least 100 times slower than hardware. Not tolerable. More decimal data. Delay of two 4-bit binary adders[24].

Conclusion:

Thus the logic gates are designed, so that information bits are not destroyed and power consumption can be reduced dramatically. In case of reversible computation information bits are not lost, this leads to the development of reversible gates. These gates are mainly used in digital circuits to enhance the effectiveness.

References:

1) c.h.bennett, Thomas, j.watson," Logical reversibility of computation", 1973, November, IBM journal of research and development.

2) Huey ling," High speed binary adder", 1981, Journal of research and development

3) R.W.doran," Variants of an improved carry look ahead adder", 1988, IEEE international journal of research and development

4) David, Malzahn,"Operations on right and left shifts of an subtraction", 1985, National institute of technical training and research

5) David m.lewis, Lawrence k.yu," Algorithm design for a 30 bit integrated logarithm processor", 1991,IEEE transactions and circuits:

6) Woo-chan, Shi-wha, Oh-young kwon,"Floating point adder/subtracts performing IEEE rounding and addition /subtraction in parallel", 1996april, IEICE TRANS.INF AND SYST.,.

7)Anvash G. keskar,Vishal R.satmata, "Design of eight bit novel reversible arithmetic and logic unit", 2001,November, ICETET,Trends in engineering and technology.

8) Ciaran j.melvor, miare mc loone" Hardware elliptic curve cryptographic processor over GF", 2006

9) Humbertocalderon,Georgigaydadjiev, Stamatisvassiliadis,"Reconfigurable universal adder", 2007, april, IEEE journal of computer applications:

10) H.R. bhagyalakshmi, M.K. venkatesha," Optimized reversible BCD adder using new reversible logic gates", 2010 February, Journal of computing.

11) Pradeepsingle,Naveen kr. Malik," A cost effective design of reversible programmable logic array", 2012,march, International journal of computer applications:

12) Akanksha dixit, vinodkapse," Arithmetic and logic unit design using reversible control unit", 2012,June, International journal of engineering and innovative technology.

13) Meenaaggarwal,aasthaagarwal,mr.rajeshmehra," 4-input decimal adder using 90 nm CMOS technology", 2013, National institute of technical training and research:

14) Khushbooahirwar,Sachinbandewar, Anandkumarsingh,"FPGA implementation ALU based on reversible logic", 2014,January, International journal of engineering research and technology:

15)Priyankayadav, Gauravkumar, Sumitagupta," Design and implementation of 4-bit arithmetic and logic unit chip with the constraint of power consumption", 2014,may, IOSR journal of electronics and communication engineering.

16) Shefalimamataj,Biswajit das," An optimized realization of ALU for 12-operations by using a control unit of reversible gates", International journal of advanced research in computer science and software engineering

17) Priyalgrover, Hemaniverma." Design layout and simulation of 8-bit arithmetic and logic unit using C5 process technology", 2015, December, International journal of electrical and electronics engineering

18) M.V.K. karthik,Dr. k.s. sagarreddy,"Implementation of reverse converter design by using reversible logic gates in hybrid parallel prefix adders, 2016,June, International journal of innovations in engineering and technology:

19) Sanjay kumar,Dr. harijindersingh," An extensive literature review on reversible arithmetic and logical unit" 2017,july, International research journal of engineering and technology.

20) Vandanashukla, o.p. singh ,g.r. mishra," Reversible realization of n-bit arithmetic circuit for low power loss ALU application", 2017,December, International conference on smart computing and communication.

21) Shanthala,Nayana,Chandrashekar,Sivayellampalli," Basic operation performed on arithmetic logic unit for 32-bit floating point numbers", 2017,november International journal of electronics engineering research.

22) d. vigneshwari ,"Design and implementation of ALU using GDI technique", 2017,july, International journal electronics and computer science.

23) Shweta thakur, sumanrani, amandeepsingh bhandari," Literature survey on reversible gates", 2018,June, International journal of engineering development and research;

24) Alp arslanbayrakei,Ahmetakkas," Reduced delay BCD adder,2017, International journal of electronics and computer science.