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A Novel Design of Hybrid 2 Bit Magnitude Comparator

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Abstract - *With the increasing demand of IoT and portable devices which are battery operated, low power designs are very essential. Comparator is the most fundamental component that performs comparison operation in circuits. In this project an efficient 2-bit magnitude comparator circuit design is proposed. This technique reduces power consumption, propagation delay, and area of digital circuits while maintaining low complexity of logic design when comparing with the traditional circuit. The performance analysis of proposed 2 bit magnitude comparator is compared with the existing technologies. The simulations are carried out in Tanner EDA tool.*

Key Words: CMOS, Gate Diffusion Input, Hybrid Designs, Low power VLSI, Magnitude Comparator, Pass transistor logic, Self Controllable Voltage Level

1. INTRODUCTION

Nowadays the semiconductor industry has been exhibiting a rapid pace of performance improvements in its products by shrinking the device geometries. The electronic devices of such products need to dissipate low power in order to conserve battery life and meet packaging reliability constraints. Consequently power consumption is a dramatic problem for all integrated circuits designed today. In the last decade, IoT devices, portable electronics such as smart phones, tablets and sensors has increased dramatically. Most of these devices are battery operated and thus power consumption has become a critical design constraint. Therefore, researchers set out to discover new methods for designing low-power electronics. Comparator is an integral part of many of the electronic circuits. When some emerging technologies are combined in the circuit, the performance and efficiency can be enhanced.

A 2 bit magnitude comparator is a hardware electronic device that takes two numbers as input in binary form and determines whether one number is greater than, less than or equal to the other number by utilizing various logic gates.

Fig 1 depicts a 2 bit magnitude comparator with inputs A1, A0, B1, B0 and outputs A<B, A=B and A>B.

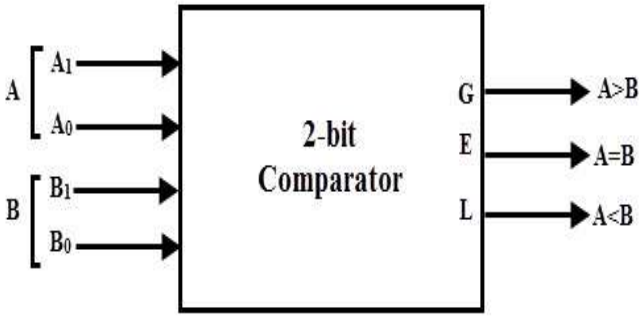

Fig -1: 2 bit magnitude comparator

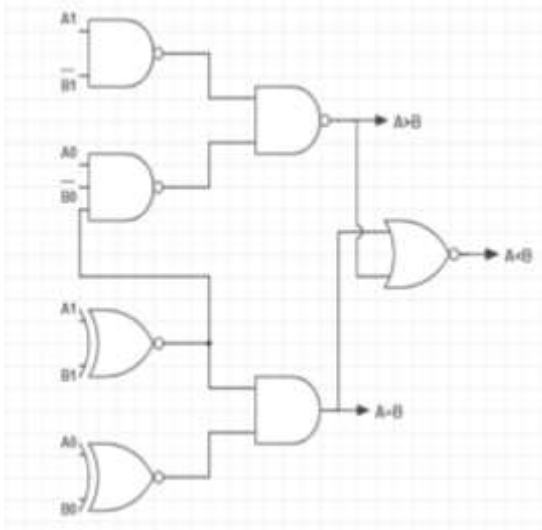

Fig -2: Gate implementation of 2 bit magnitude comparator

The gate implementation of 2 bit magnitude comparator using three NAND gates, 2 EX-NOR gates, one AND gate and one NOR gate is shown in fig 2.

The outcome of 2-Bit magnitude comparator is shown in Table 1 for different combinations of input vectors. According to different condition of inputs, appropriate outputs are generated.

Table -1: Truth table of 2 bit magnitude comparator

Inputs				Outputs		
A_1	A_0	B_1	B_0	$A<B$	$A=B$	$A>B$
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

2. CONVENTIONAL DESIGN

Most of the digital circuits are generally designed using various logic styles. Nowadays, hybrid designing is a new methodology followed by circuit designers for efficient performance of the circuit. It is a new approach of designing in which two or more trending low power techniques are combined to form an effective circuit exhibiting low power, area and delay.

2.1 PTL-CMOS HYBRID DESIGN

Since hybrid designing is a trending method in low power designing, PTL-CMOS hybrid 2 bit magnitude comparator is one of the existing design. The 2-bit Magnitude Comparator has a binate composition of input variables. When it is implemented by using a synthesis of Pass Transistor Logic and CMOS logic styles, very low trends in power consumption, delay, power delay product and area in terms of transistor count were obtained. Fig 3 depicts the 2 bit magnitude comparator circuit using PTL-CMOS hybrid technology. The circuit is comprised of two PTL XOR gates, six CMOS NAND gates and a CMOS AND gate. This design of magnitude comparator has achieved 50-90% reduction in power consumption. Even though the existing design is hybrid, an upswing in power consumption, delay and PDP is observed and curtailment of the design parameters can be prevailed using other hybrid designs.

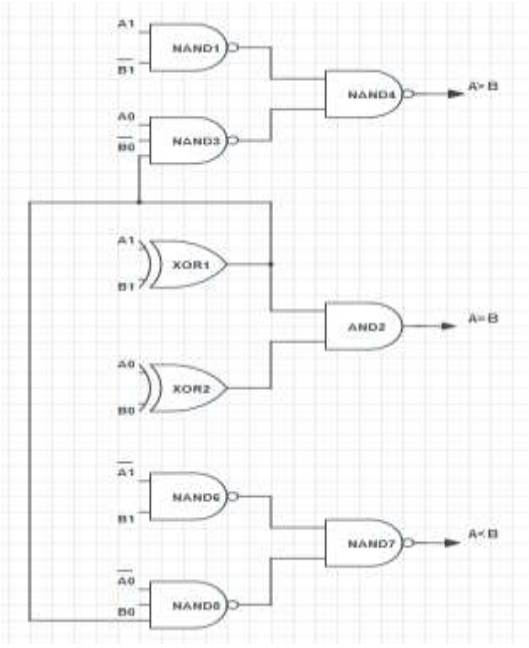

Fig -3 PTL-CMOS hybrid circuit

3. SELF CONTROLLABLE VOLTAGE LEVEL

Self- Controllable Voltage Level (SVL) circuit is a low power technique which can significantly decrease power consumption while maintaining high-speed performance of the circuit. It comprises of an upper SVL circuit and a lower SVL circuit. The SVL circuit is portrayed in fig 4.

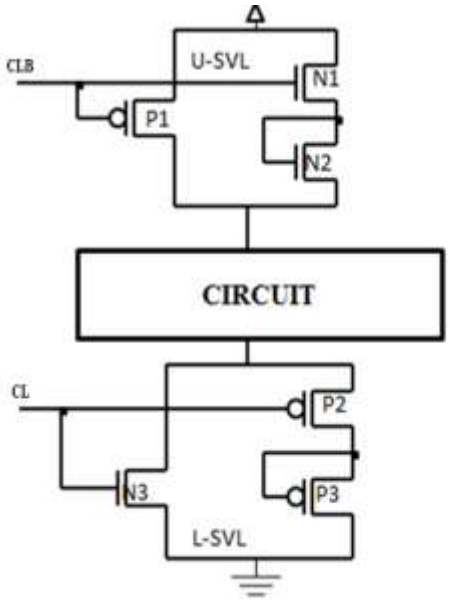

Fig -4 Self Controllable Voltage Level (SVL) circuit

The U-SVL technique is a combination of a PMOS and two NMOS transistors that are linked in parallel. Here an input clock pulse is fed to drive PMOS of U-SVL circuit and the remaining all NMOS are connected to drain terminal.

For small Power consumption applications, U-SVL technique is most accountable. The L-SVL system is an incarnation of an NMOS and two PMOS that are linked in parallel. Consequently an input clock pulse is applied to the NMOS of L-SVL circuit and the remaining all PMOS are connected to the ground. The ground terminal is allied to the L-SVL circuit.

When clock is low in U-SVL, PMOS would turn ON and maximum amount of V_{DD} is passed to load circuit. This is referred to as the active mode. In standby mode, clock is made high so that PMOS is turned OFF and NMOS is turned ON. Thus V_{DD} to the load is reduced and threshold voltage of NMOS in the load circuit is magnified. This in turn minimize subthreshold conduction and leakage current. By the utilization of this technique, sufficient amount of leakage current, PDP and average power can be considerably diminished.

4. PROPOSED DESIGNS

4.1 GDI-CMOS HYBRID DESIGN

The 2 bit magnitude comparator designed using hybrid combination of GDI and CMOS logic style is shown in Fig 5. The design comprises of different logic gates designed with GDI and CMOS. The proposed design shows good performance and power reduction with the incorporation of low power technique called SVL in the design.

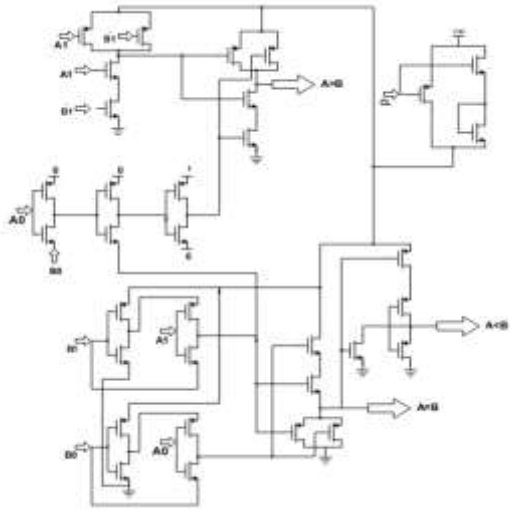

Fig -5 GDI-CMOS circuit

4.2 PTL-GDI 1 HYBRID DESIGN

The 2 bit magnitude comparator designed with a combination of PTL and GDI logic styles to form a hybrid design is shown in Fig 6. The designed circuit comprises of logic gates using PTL and GDI styles. The low power technique known as SVL is added along with the circuit to reduce the power consumption and delay to provide better performance.

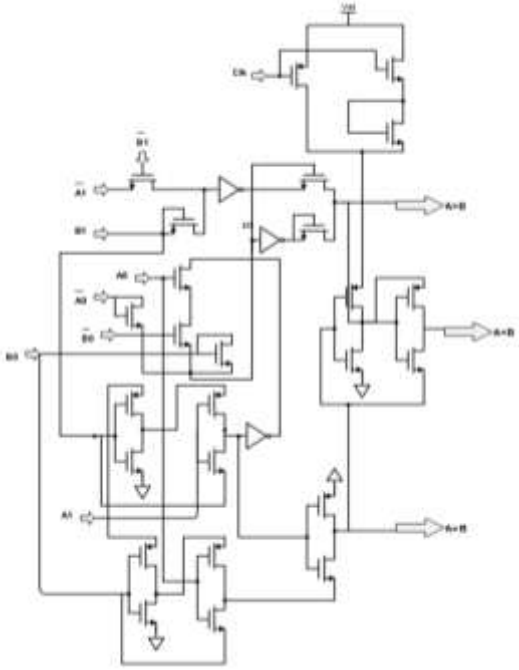

Fig -6 PTL-GDI 1 circuit

4.3 PTL-GDI 2 HYBRID DESIGN

Hybrid 2 bit magnitude comparator designed using PTL and GDI logic style is shown in Fig 7. The design along with low power technique, SVL provides better performance by reducing power and delay.

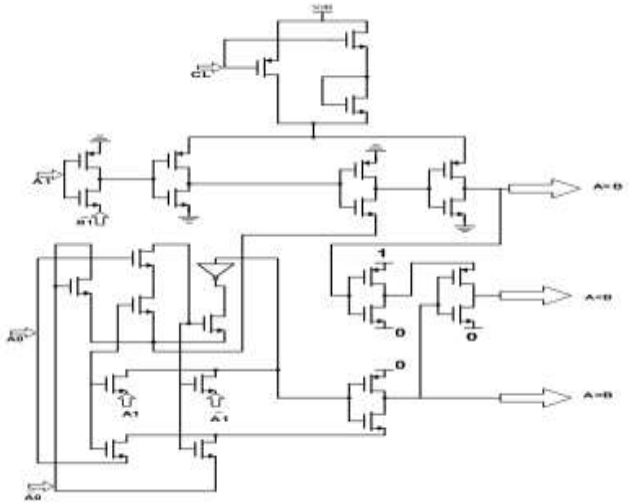

Fig -7 PTL-GDI 2 circuit

4.4 PTL-GDI 3 HYBRID DESIGN

Circuit design styles in VLSI, PTL and GDI are combined to give a hybrid 2 bit magnitude comparator which enables better power reduction and less delay with SVL in the design. This in turn shows good performance. The circuit is depicted in Fig 8.

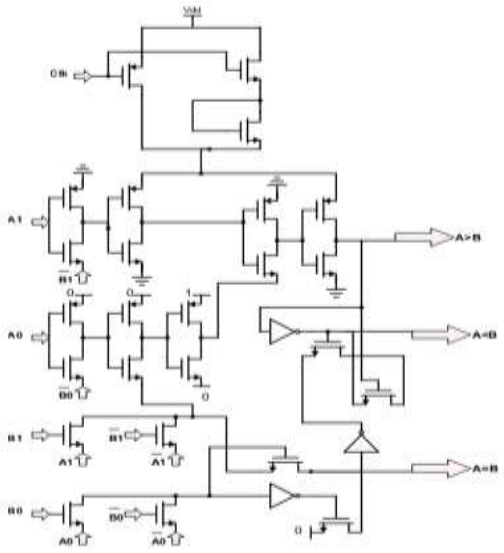

Fig -8 PTL-GDI 3 circuit

4.5 PTL-GDI 4 HYBRID DESIGN

PTL and GDI combination gives another hybrid 2 bit magnitude comparator which is shown in Fig 9. SVL technique is incorporated in the circuit design so as to reduce the power and delay to provide good performance.

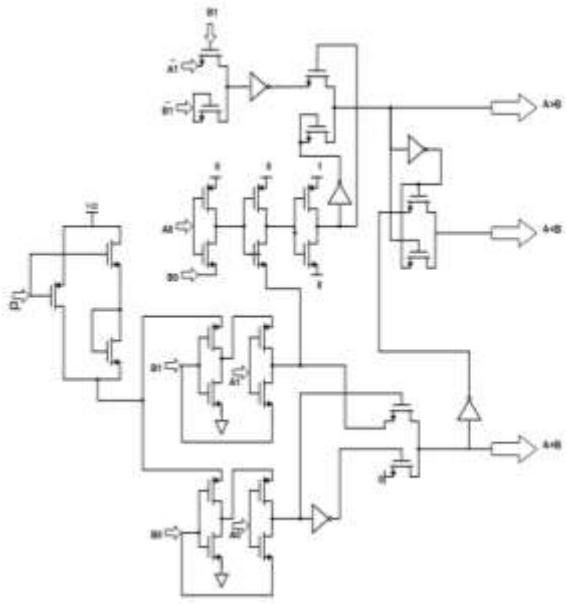

Fig -9 PTL-GDI 4 circuit

5. RESULTS AND ANALYSIS

5.1 WAVEFORM

Figure 10 depicts the obtained waveform of 2 bit magnitude comparator.

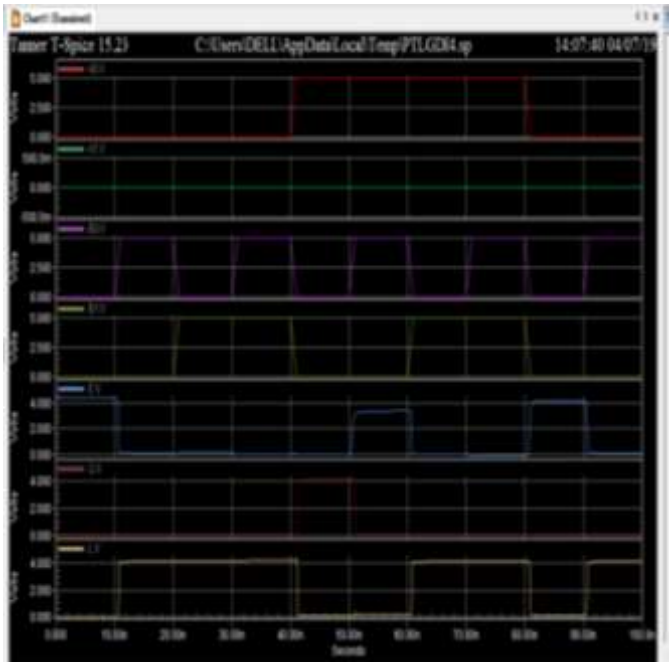

Fig -10 Waveform of 2 bit magnitude comparator

5.2 COMPARISON OF POWER, DELAY AND POWER DELAY PRODUCT

As far as electronic circuits are concerned, power consumption is a major bottleneck of system performance. The main source is the dynamic power consumption. As long as there are a number of dynamic power reduction techniques, the system performance can also be enhanced by reducing the leakage power consumption. Along with that, the most effective leakage power reduction method i.e. SVL can be incorporated with the design. When comparing the performance and power with different hybrid designs, the design incorporating SVL shows better reduction in the total power.

Table -2: Comparison of power, delay and PDP

Magnitude Comparator	Power	Power with SVL	Delay	PDP (Wps)
GDI-CMOS	37.14e-004	14.22e-004	123.7 p	0.17 59
PTL-GDI 1	6.517e-004	4.543e-004	20.14 n	9.14 9
PTL-GDI 2	17.82e-004	11.13e-004	25.93 p	0.02 88
PTL-GDI 3	7.679e-004	5.441e-004	25.93 p	0.01 4
PTL-GDI 4	5.802e-004	2.61e-004	10.47 n	2.73 26

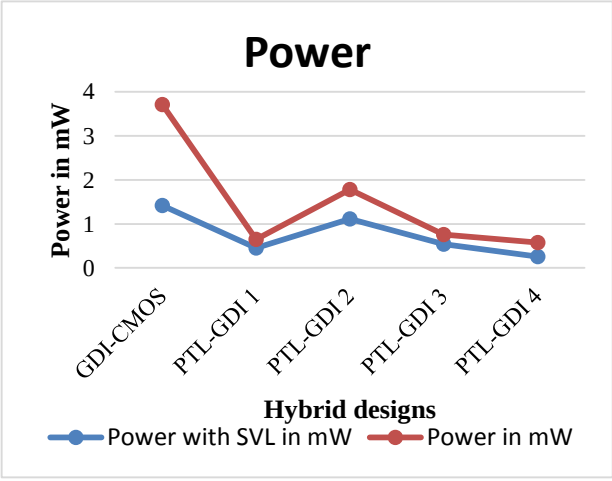

Chart -1: Power Comparison

Chart 1 is the portrayal power consumption of various proposed hybrid designs of 2 bit magnitude comparator. It is very obvious that when the designed 2 bit hybrid magnitude comparator circuits are incorporated with the power reduction technique SVL, a tremendous reduction in power dissipation is observed. With precise evaluation the proposed PTL-GDI 4 design dissipates comparatively much less power than the conventional circuits.

The proposed designs when consolidated with SVL, enhances the performance by lowering the propagation delay. The same is outlined as a graph in Chart 2 which illustrates that the proposed PTL-GDI designs exhibit better performance in terms of delay.

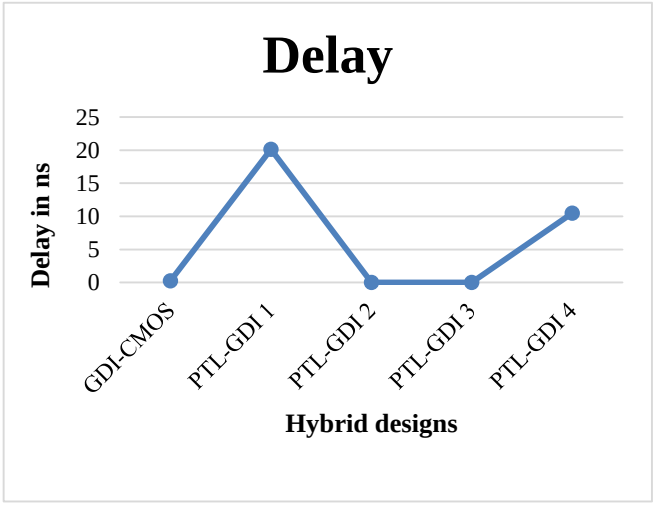

Chart -2: Delay Comparison

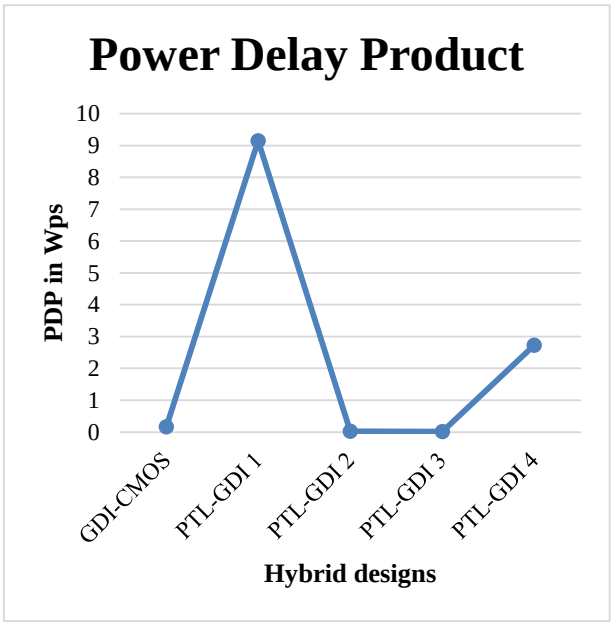

Chart-3 Power Delay Report

The Chart-3 represents the power delay product of various proposed hybrid designs. From the surveillance, PTL-GDI designs provide better performance in terms of PDP.

6. CONCLUSION

A 2-bit hybrid magnitude comparator circuit is designed using different logic styles such as GDI, PTL, CMOS and SVL. Simulations are carried out and the power analysis of the circuits have been performed. From the observations it is evident that PTL-GDI 4 is the efficient design with minimum power consumption. Thus by combining the existing technologies an efficient hybrid circuit of a 2- bit magnitude comparator is designed. It ensures low power consumption, propagation delay, and area of digital circuits while maintaining low complexity of design when compared with the existing comparator circuit using traditional logic styles.

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