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Design and Simulation of Comparator Architectures for Various ADC Applications

Disha Gaude[1], Bathini Poornima[2], K. M. Sudharshan[3], Prashant V. Joshi[4]

[1,2,3,4]*Dept. of Electronics and communication Engineering, REVA University, Bengaluru, India*

Abstract - *This paper presents design and simulation of different CMOS comparators. The designs are simulated and studied in 180 nm Technology with Cadence Virtuoso Tool with supply voltage 3.3 V and reference voltage of 3V. The clock used in comparator has a frequency of 1 M Hz. The comparators are mostly used in converting analog signals to digital signals for processing. Comparators are used in the applications requiring less power dissipation, good accuracy and high resolution.*

Key Words: comparator, Dynamic, Static, Latch, Clock Frequency, Pre amplifier, post amplifier.

Ⅰ. Introduction

Comparator is a circuit which compares two input voltages in which one is analog input and other is reference voltage and outputs binary 0 or 1 depending on comparison. It is basically a 1 bit analog to digital converter. In ADCs sample and hold circuit samples the analog input signal and the sampled signal is given to comparator, depending on reference voltage it produces digital output which is equivalent to analog input signal [1].

Comparators are used in all ADCs requiring less power dissipation, high speed, low noise, less offset voltage, good slew rate etc. Different types of comparators are available namely open loop comparator, regenerative comparator and combination of both open loop and regenerative comparator (cascaded comparators) [2]. Open loop compactors are basically single and two stage differential amplifiers without compensation and feedback loop. Regenerative comparators use positive feedback to improve the performance [3]. Comparator circuits can also be built by separating the comparators into number of cascaded stages. This helps in reducing the total propagation delay time and hence can be used in high speed applications like radar receivers and LAN interfaces.

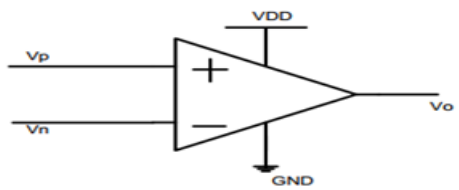

Fig -1. Symbol of comparator

Above figure shows the symbol of comparator. It is basically operational amplifier because every comparator has one or many of the same characteristics as a high gain amplifier. The voltage V_p applied to the positive terminal of the comparator gives output 1 if voltage V_n applied to negative terminal is less or equal to V_p or else the output of the comparator gives 0 [11].

Ⅱ. Characterization of a comparator

Static characteristics

Gain

The ideal aspect of this model is the way in which the output makes a transition between V_{OL} and $V_{OH.}$ The output changes states for an input change of ΔV, where ΔV approaches zero [4]. The gain is given as

$$\text{Gain} = A_V = \lim_{\Delta V \to 0} \cdot \frac{VOH - VOL}{\Delta V}$$

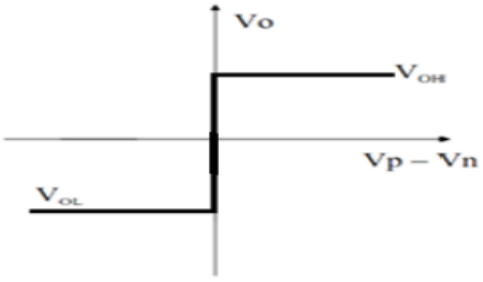

Fig -2. Ideal transfer curve

Offset Voltage

A mismatch in the threshold voltages and the trans conductance parameters of the transistor generates offset voltage in comparator. If the output did not change until the input difference reached a value of V_{OS} then the difference would be defined as the offset voltage [5].

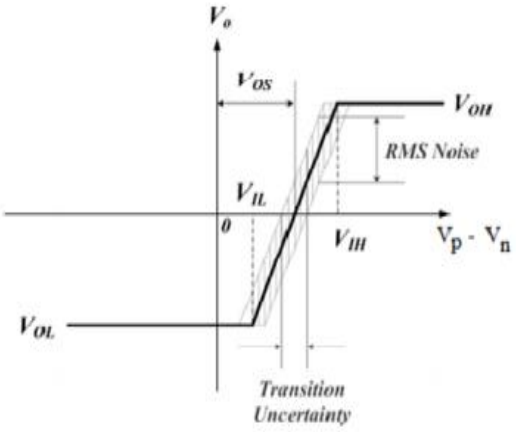

Fig -3. Transfer curve of a comparator including offset voltage and noise

Dynamic characteristics

Propagation Delay

Propagation delay is defined as at how much speed the amplifier responds with applied input [6].

Propagation delay time = (rising propagation delay time + falling propagation delay time)/2

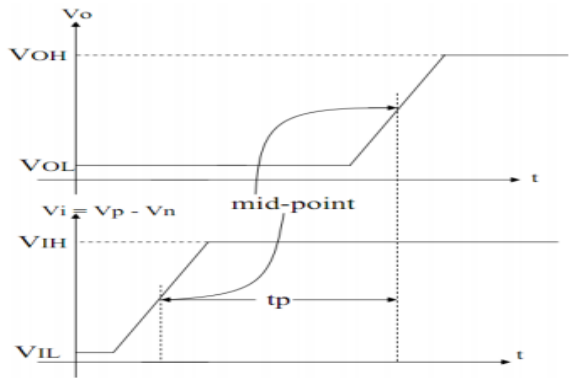

Fig -4. Propagation delay curve

Ⅲ Comparator Topologies

A. Two stage open loop comparator

Comparator requires differential input and high gain to achieve desirable resolution. As a result two stage operational amplifiers can be used as a comparator. Comparator requires large bandwidth as possible so that faster response can be achieved. This is done by making two stage operational amplifiers as an open loop mode, thus no compensation is required [7].The advantage of this comparator is to provide high gain, large output voltage swing and disadvantage is that it consumes more power. Hence, it is not suitable for high speed and low power applications.

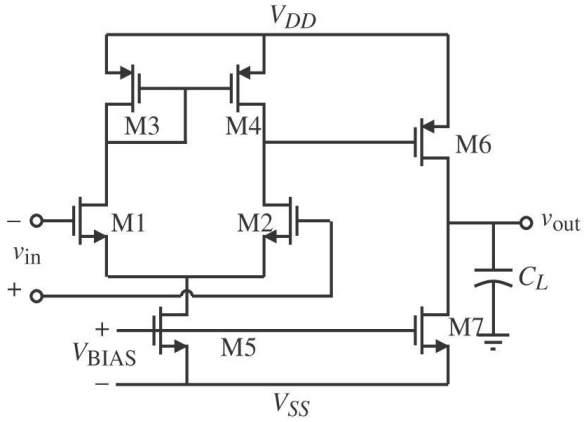

Fig -5. Open loop comparator

Small signal gain of the comparator as given by

$$A_V = \left(\frac{gm1}{gds2+gds4}\right)\left(\frac{gm6}{gds6+gds7}\right)$$

Two stage comparator consists of two pole, first and second stage output poles P1 and P2 respectively are given as

$$P1 = -\frac{(gds2+gds4)}{CI}$$

Where C_I is the sum of capacitance connected to the output of first stage.

$$P2 = \frac{(gds6+gds7)}{CII}$$

Where C_{II} is the sum of capacitance connected to the output of second stage.

B. Regenerative comparator

Regenerative comparators use positive feedback to accomplish the comparison of two signals. The regenerative comparator is also called a latch or bistable. The simplest form of a latch is shown below

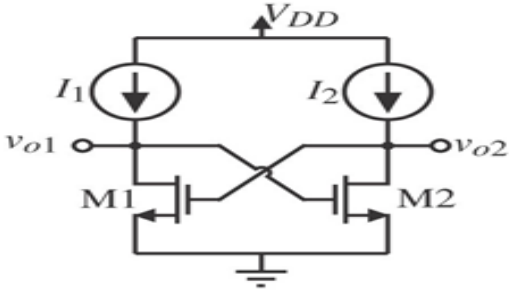

Fig -6. NMOS Latch

Normally, the latch has two modes of operation. The first mode disables the positive feedback and applies the input signal to the terminals as V_{01} and V_{02}. The initial voltages applied during this mode will be as V_{01}^1 and V_{01}^2. The second mode enables the latch and depending on the relative values of V_{01}^1 and V_{01}^2, one of the outputs will go high and the other will go low. A two phase clock is used to determine the modes of operation [10].

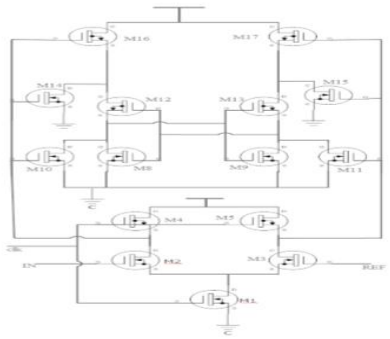

Fig -7. Dynamic latch

C. High speed comparator

High speed comparators should have a propagation delay time as small as possible. To achieve this goal, one must understand the requirement for fast comparator. This is best understood by separating the comparator into a number of cascading stages. So, this three cascading stages consists of input pre amplification stage, latch stage and output post amplification stage [8].

Pre amplification stage consists of current mirror single stage differential amplifier with high gain and low slew rate. This stage improves sensitivity of the comparator by isolating input from kickback noise and amplifying the smallest minimum input voltage. Latch is basically positive feedback circuit which determines the difference of the two input signals. Post amplification stage consists of self-biased differential amplifier followed by inverter. This stage helps in driving the high load and inters parasitic capacitance [9].

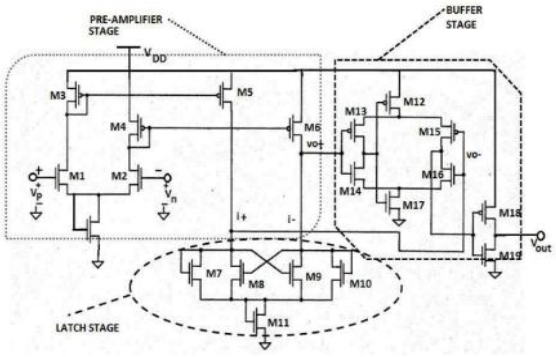

Fig -8. High speed comparator

VI Simulation Results

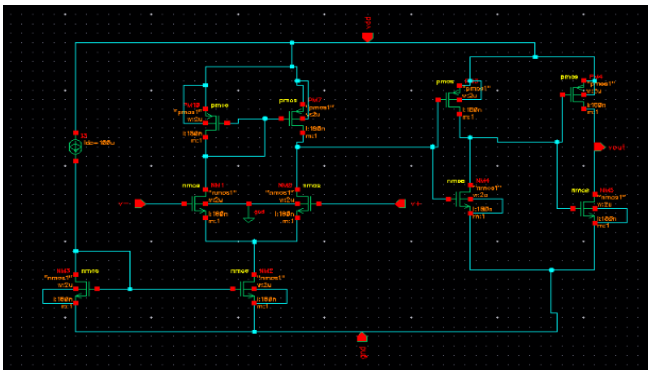

Fig -9. Schematic of two stage uncompensated comparator

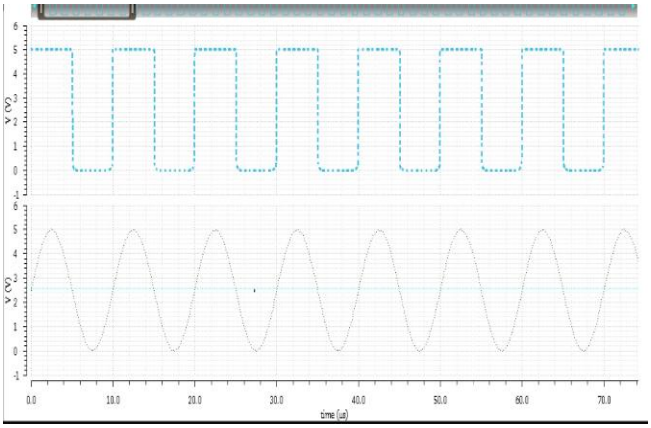

Fig -10. Output waveforms of two stage uncompensated comparator

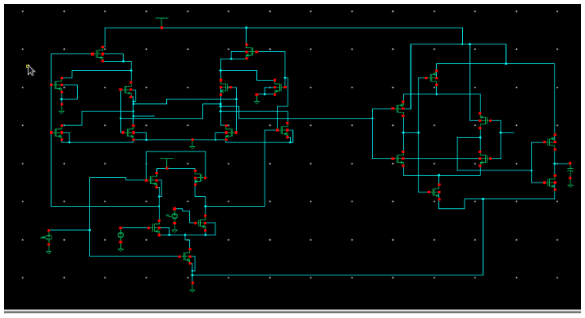

Fig -11. Schematic of dynamic latch

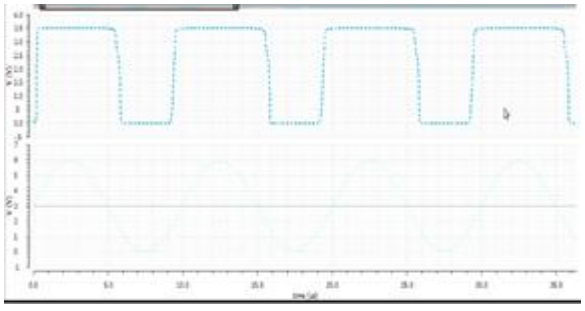

Fig -12. Output waveforms of dynamic latch

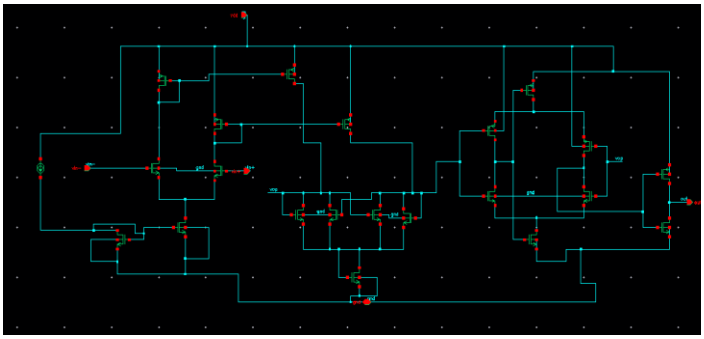

Fig -13. Schematic of high speed comparator

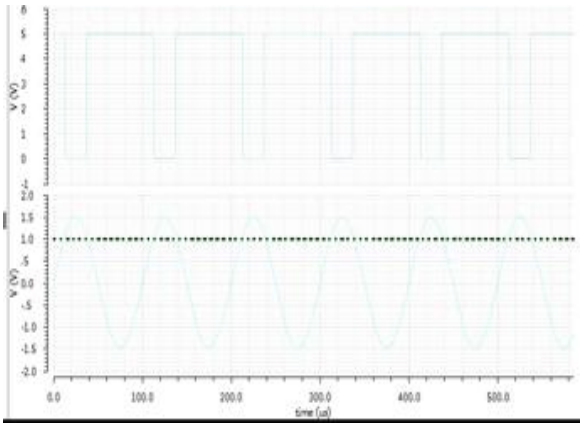

Fig -14. Output waveforms of comparator

Table -1. Comparision of different types of comparator parameters

Comparator	Power Dissipation [uW]	Propagation Delay [ps]	Speed [GHz]
Two satge uncompensated comparator	101.5	57.12	7.507
Regenarative Comparaor	19.57	186.5	5.3619
High Speed Comparator	2.121	11.9	84.03

V. Conclusion

In this paper two stage uncompensated comparator, dynamic latch, regenerative comparator and high speed comparator with cascaded stages are implemented and simulated and simulation is carried out using Cadence tools, with gpdk 180nm. It is also verified with LT-SPICE using tsmc180nm technology file. The power dissipation, total propagation delay and speed are compared and calculated for different types of comparators with supply voltage 5 V.

VI. Acknowledgement

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