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Design and Analysis of Single Phase Modified Quasi-Z-Source Cascaded Hybrid Three Level Inverter

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Abstract - *This paper proposes combination of a novel single-stage quasi cascaded H-bridge three-level boost inverter. It proposes the combination of a novel modified quasi-Z-source (MqZS) inverter with a single- phase symmetrical hybrid three-level inverter in order to boost the inverter three-level output voltage. The proposed quasi cascaded h-bridge three-level boost inverter has the advantages over the cascaded H- bridge quasi-Z-source inverter in cutting down passive components. The single-phase MqZS hybrid inverter provides a higher boost ability and reduces the number of inductors in the source impedance, compared with both the single-phase three-level neural-point clamped (NPC) MqZSI and the single-phase quasi-Z source cascaded multilevel inverter (CMI). The performances of both the proposed MqZS-CHI and the modulation techniques are verified through simulation and experimental results. Simulation and experimental results are presented to demonstrate the expected representations. Consequently, size, cost, and weight of the proposed inverter are reduced. A capacitor with low voltage rating is added to the proposed topology to remove an offset voltage of the output AC voltage when the input voltages of two modules are unbalanced.*

Key Words: **cascaded, clamped, H-bridge, hybrid, inverter, modulation, quasi.**

1. INTRODUCTION

Traditional voltage source inverters (VSIs), the obtainable ac output voltage is limited to less than the dc input voltage, and thus an additional stage, consisting of a dc-dc boost converter, is required to obtain the desired ac output voltage. The additional dc-dc boost converter increases the cost and decreases the efficiency of the overall power converter. In order to overcome the limitations of traditional VSIs, both the Z-source inverter (ZSI) and the quasi ZSI (qZSI), in which the traditional dc-link is replaced with the Z-source impedance network, have been developed [1]-[5]. The ZSI/qZSI can boost the dc-link voltage by using the shoot-through state of the inverter bridge with a single power conversion stage. Therefore, it can reduce the component count and enhance the reliability. However, because the shoot-through state can only be regulated within a zero state, the practical boost factor of the qZSI/ZSI is usually restricted. This may limit further applications of the qZSI/ZSI in some areas that require high voltage gain for low-voltage energy sources, such as fuel-cell stacks and batteries.

Multilevel inverters are suited for high-voltage and high-power applications because they are designed to naturally share the total dc voltage between cascaded power semiconductors. By increasing the number of inverter voltage levels, it becomes possible to achieve high- voltage and low-distortion ac waveforms, as well as reduce the blocking voltage requirement of individual switching devices.

The integration techniques of the Z-source energy conversion concept applied to various multilevel inverters have been introduced to combine the advantages of both the Z-source inverter and the multilevel inverter. A dual Z- source inverter with reduced common-mode switching and voltage buck-boost capability has been designed. However, an ac output transformer connected to dual-bridge ac outputs of dual ZSI is required to provide a five-level ac output voltage. The three-level Z-source neural-point clamped (NPC) inverter and dc-link cascaded inverter are implemented by using a single impedance network and a single dc source. They can reduce the system cost due to the lower numbers of Z-source impedance networks and dc sources. However, their boost ability is limited, as with the classic ZSI. In, the operation analysis and modulation techniques based on the phase disposition (PD) scheme of the three-level NPC ZSI are presented to achieve voltage boosting, better output voltage quality, and the minimal commutation count. Because those are accomplished by adding the triple offset and shoot-through time to the sinusoidal references, its implementation is quite complex. The closed-loop control of both the capacitor voltage and the load current for a three-level NPC ZSI is discussed in [15] in order to obtain the desired dynamic response. The operation and modulation techniques for controlling the five-level NPC Z-source inverter, combining the two Z-source impedance networks with a separate dc source and the

five-level NPC inverter, are analyzed.

Similarly, a three-level NPC quasi-ZSI is discussed, where a quasi-Z-source impedance network is combined with an NPC structure. It can provide a continuous dc source current and multilevel output voltage. In spite of the fact that the three-level NPC qZSI has two identical quasi Z- source networks, its boost factor is the same as a traditional qZSI. The work focuses on the control method and analytic model design of a quasi-Z source cascaded multilevel inverter (qZS-CMI) for photovoltaic (PV) power generation systems. This approach includes distributed maximum power point tracking, voltage balance control, and the grid- current control strategy. Because each PV array connects to a separate qZS H-bridge module at the qZS-CMI, an additional qZS H-bridge module is required as the number of ac output voltage level increases by one step. The work in presents an inverter topology based on a cascaded Z-source impedance with two switching devices and one H-bridge unit, where the number of power semiconductor switches can be reduced with respect to traditional multilevel inverters. However, three Z-source impedances and three separate dc sources are required in order to generate the output voltage with seven voltage levels. The switching algorithms for five-level quasi-ZSI, combining the quasi-ZSI and the five-level inverter using a coupling inductor, are developed in. The three-level LC-switching-based boost NPC inverter presented in utilizes a lower number of passive reactive components as well as a single split dc source, and it needs the two extra switching devices. Most existing topologies including both the NPC ZSI/qZSI and the qZS-CMI require a large number of components for producing the boosted ac output voltage with five/nine voltage levels. Their boost factor is also limited to the boost factor of a classic ZSI/qZSI. In order to reduce the number of components, especially inductors and raise the boost factor, this paper proposes a single-phase modified quasi-Z- source (MqZS) hybrid three-level inverter. In addition, a single-phase modified quasi-Z-source cascaded hybrid five- level inverter (MqZS-CHI) is designed by connecting two three-level PWM switching cells in series for producing a nine-level output voltage. The MqZS-CHI can be recommended for applications requiring a high output voltage with lower THD. A modified phase-shift modulation technique based on an alternative phase opposition disposition (APOD) scheme is proposed, in order to effectively control the shoot-through state for boosting the dc-link voltage. This modified modulation technique can offer a simple implementation and balance the two series capacitor voltages of the cascaded hybrid five-level inverter. Simulation and experimental results are carried out to verify the performances of the proposed topologies and modulation techniques.

1.1 Voltage Source Converter

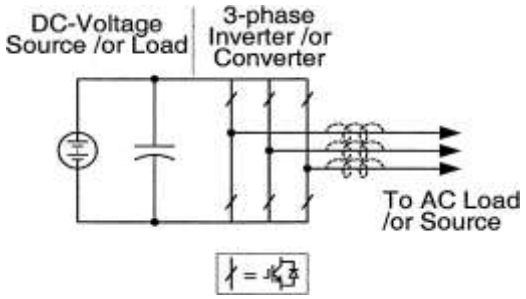

Fig.1 Traditional V-source converter.

Figure shows the traditional three-phase voltage-source converter (abbreviated as V-source converter) structure. A dc voltage source supported by a relatively large capacitor feeds the main converter circuit, a three-phase bridge. The dc voltage source can be a battery, fuel-cell stack, diode rectifier, and/or capacitor. Six switches are used in the main circuit; each is traditionally composed of a power transistor and an anti-parallel (or freewheeling) diode to provide bidirectional current flow and unidirectional voltage blocking capability. The V-source converter is widely used. It, however, has the following conceptual and theoretical barriers and limitations.

The ac output voltage is limited below and cannot exceed the dc-rail voltage or the dc-rail voltage has to be greater than the ac input voltage. Therefore, the V-source inverter is a buck (step-down) inverter for dc-to-ac power conversion and the V-source converter is a boost (step-up) rectifier (or boost converter) for ac-to-dc power conversion. For applications where over drive is desirable and the available dc voltage is limited, an additional dc-dc boost converter is needed to obtain a desired ac output. The additional power converter stage increases system cost and lowers efficiency.

The upper and lower devices of each phase leg cannot be gated on simultaneously either by purpose or by EMI noise.

Otherwise, a shoot-through would occur and destroy the devices. The shoot-through problem by electromagnetic interference (EMI) noise's misgating-on is a major killer to the converter's reliability. Dead time to block both upper and lower devices has to be provided in the V-source converter, which causes waveform distortion, etc.

An output LC filter is needed for providing a sinusoidal voltage compared with the current-source inverter, which causes additional power loss and control complexity.

1.2 Current Source Converter

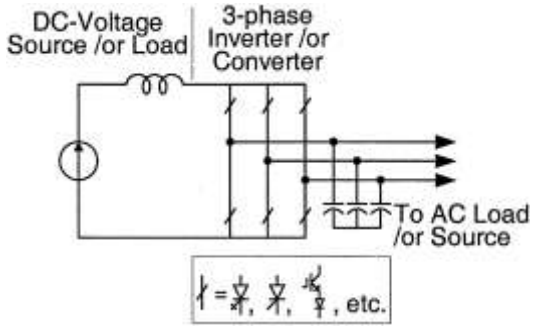

Fig.2 Traditional I-source converter

Figure shows the traditional three-phase current-source converter (abbreviated as I-source converter) structure. A dc current source feeds the main converter circuit, a three- phase bridge. The dc current source can be a relatively large dc inductor fed by a voltage source such as a battery, fuel-cell stack, diode rectifier, or thyristor converter. Six switches are used in the main circuit, each is traditionally composed of a semiconductor switching device with reverse block capability such as a gate-turn-off thyristor (GTO) and SCR or a power transistor with a series diode to provide unidirectional current flow and bidirectional voltage blocking. However, the I-source converter has the following conceptual and theoretical barriers and limitations.

The ac output voltage has to be greater than the original dc voltage that feeds the dc inductor or the dc voltage produced is always smaller than the ac input voltage. Therefore, the I-source inverter is a boost inverter for dc- to-ac power conversion and the I-source converter is a buck rectifier (or buck converter) for ac-to-dc power conversion. For applications where a wide voltage range is desirable, an additional dc–dc buck (or boost) converter is needed. The additional power conversion stage increases system cost and lowers efficiency.

At least one of the upper devices and one of the lower devices have to be gated on and maintained on at any time. Otherwise, an open circuit of the dc inductor would occur and destroy the devices. The open-circuit problem by EMI noise's misgating-off is a major concern of the converter's reliability. Overlap time for safe current commutation is needed in the I-source converter, which also causes waveform distortion, etc.

The main switches of the I-source converter have to block reverse voltage that requires a series diode to be used in combination with high-speed and high-performance transistors such as insulated gate bipolar transistors (IGBTs). This prevents the direct use of low-cost and high- performance IGBT modules and intelligent power modules.

In addition, both the V-source converter and the I-source converter have the following common problems.

- They are either a boost or a buck converter and cannot be a buck–boost converter. voltage range is limited to either greater or smaller than the input voltage.
- Their main circuits cannot be interchangeable. In other words, neither the V-source converter main circuit can be used for the I-source converter, nor vice versa
- They are vulnerable to EMI noise in terms of reliability.

1.3 Modified Quasi Z source cascaded with Multilevel Inverter

The ZSI/qZSI can boost the dc-link voltage by using the shoot-through state of the inverter bridge with a single power conversion stage. Therefore, it can reduce the component count and enhance the reliability. However, because the shoot through state can only be regulated within a zero state, the practical boost factor of the qZSI/ZSI is usually restricted. This may limit further applications of the qZSI/ZSI in some areas that require high voltage gain for low-voltage energy sources, such as fuel-cell stacks and batteries

Multilevel inverters are suited for high-voltage and high-power applications because they are designed to naturally share the total dc voltage between cascaded power semiconductors. By increasing the number of inverter voltage levels, it becomes possible to achieve high- voltage and low-distortion ac waveforms, as well as reduce the blocking voltage requirement of individual switching devices

The integration techniques of the Z-source energy conversion concept applied to various multilevel inverters have been introduced to combine the advantages of both the Z-source inverter and the multilevel inverter.

The three-level Z-source neural-point clamped (NPC) inverter and dc-link cascaded inverter are implemented by using a single impedance network and a single dc source. They can reduce the system cost due to the lower numbers of Z-source impedance networks and dc sources. However, their boost ability is limited, as with the classic ZSI.

Similarly, a three-level NPC quasi-ZSI is discussed in, where a quasi-Z-source impedance network is combined with an NPC structure. It can provide a continuous dc source current and multilevel output voltage. In spite of the fact that the three-level NPC qZSI has two identical quasi Z- source networks, its boost factor is the same as a traditional qZSI.

An inverter topology based on a cascaded Z-source impedance with two switching devices and one H-bridge unit, where the number of power semiconductor switches can be reduced with respect to traditional multilevel inverters. However, three Z-source impedances and three separate dc sources are required in order to generate the output voltage with seven voltage levels.

The three-level LC-switching-based boost NPC inverter presented in utilizes a lower number of passive reactive components as well as a single split dc source, and it needs the two extra switching devices.

Most existing topologies including both the NPC ZSI/qZSI and the qZS-CMI require a large number of components for producing the boosted ac output voltage with three/nine voltage levels. Their boost factor is also limited to the boost factor of a classic ZSI/qZSI.

In order to reduce the number of components, especially inductors and raise the boost factor, this paper proposes a single-phase modified quasi-Z-source (MqZS) hybrid three-level inverter.

In addition, a single-phase modified quasi-Z-source cascaded hybrid five-level inverter (MqZS-CHI) is designed by connecting two three-level PWM switching cells in series for producing a nine-level output voltage.

1.4Z-Source Converter

To overcome the above problems of the traditional V- source and I-source converters, this paper presents an impedance-source (or impedance-fed) power converter (abbreviated as Z-source converter) and its control method for implementing dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. Fig. 3 shows the general Z-source converter structure proposed. It employs a unique impedance network (or circuit) to couple the converter main circuit to the power source, load, or another converter, for providing unique features that cannot be observed in the traditional V- and I-source converters where a capacitor and inductor are used, respectively. The Z-source converter overcomes the above-mentioned conceptual and theoretical barriers and limitations of the traditional V-source converter and I-source converter and provides a novel power conversion concept.

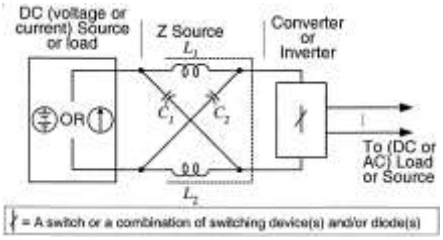

Figure Z source converter

2 LITERATURE REVIEW

In [1] Anh-Vu Ho and Tae-Won Chun proposes the combination of a novel modified quasi-Z-source (MqZS) inverter with a single-phase symmetrical hybrid three-level inverter in order to boost the inverter three-level output voltage. The proposed single-phase MqZS hybrid three- level inverter provides a higher boost ability and reduces the number of inductors in the source impedance, compared with both the single-phase three-level neural- point clamped (NPC) qZSI and the single-phase quasi-Z source cascaded multilevel inverter (CMI). Additionally, it can be extended to obtain the nine-level output voltage by cascading two three-level PWM switching cells with a separate MqZS and dc source, which herein is called a single-phase MqZS cascaded hybrid five-level inverter (MqZS-CHI). A modified modulation technique based on an alternative phase opposition disposition (APOD) scheme is suggested to effectively control the shoot-through state for boosting the dc-link voltage and balancing the two series capacitor voltages of the MqZS. The performances of both the proposed MqZS-CHI and the modulation techniques are verified through simulation and experimental results.

In [2] F.Z. Peng etl proposed an impedance-source (or impedance-fed) power converter (abbreviated as Z-source converter) and its control method for implementing dc-to- ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. The Z-source converter employs a unique impedance network (or circuit) to couple the converter main circuit to the power source, thus providing unique features that cannot be obtained in the traditional voltage-source (or voltage-fed) and current-source (or current-fed) converters where a capacitor and inductor are used, respectively. The Z-source converter overcomes the conceptual and theoretical barriers and limitations of the traditional voltage-source converter (abbreviated as V-source converter) and current- source converter (abbreviated as I-source converter) and provides a novel power conversion concept. The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. To describe the operating principle and control, this paper focuses on an example: a Z- source inverter for dc-ac power conversion needed in fuel cell applications. Simulation and experimental results will be presented to demonstrate the new features.

In [4] M. Mamatha and V.Chandrashekar presents the NNPC inverter is a newly developed four-level voltage source inverter for medium-voltage applications with properties such as operating over a wide range of voltages (2.4–7.2 kV) without the need for connecting power semiconductor in series and high-quality output voltage. The NNPC topology has two flying capacitors in each leg. In order to ensure that the inverter can operate normally and all switching devices share identical voltage stress, the voltage across each capacitor should be controlled and maintained at one-third of dc bus voltage. The proposed capacitor voltage-balancing method takes advantage of redundancy in phase switching states to control and balance flying capacitor voltages. Simple and effective logic tables are developed for the balancing control.

In [6] Mariusz Malinowski and etl proposes Cascaded multilevel inverters synthesize a medium voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. Due to these features, the cascaded multilevel inverter has been recognized as an important alternative in the medium-voltage inverter market. This paper presents a survey of different topologies, control strategies and modulation techniques used by these inverters. Regenerative and advanced topologies are also discussed. Applications where the mentioned features play a key role are shown. Finally, future developments are addressed.

3 PROPOSED METHOD

3.2 Single-Phase Modified Quasi-Z- Source Hybrid Three-Level Inverter

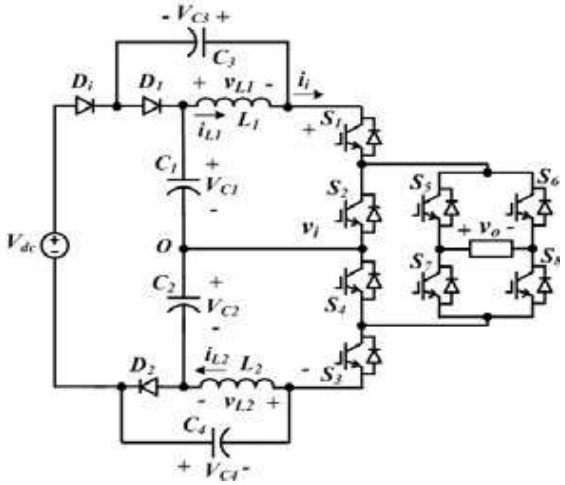

Fig.3 A single-phase MqZS hybrid three-level inverter

Figure shows the topology of a single-phase MqZS hybrid three-level inverter, where a MqZS can be implemented by removing two inductors of the quasi-Z- source impedance network and connecting a single diode between the dc voltage source and the upper impedance network, and it is incorporated with a symmetrical hybrid three-level inverter proposed in. A symmetrical hybrid three-level PWM switching cell is linked to a single-phase full-bridge (SPFB) inverter with a low switching frequency, which consists of switches S5 to S8. The pairs S5/S8 and S6/S7 are turned on complementarily according the polarity of the sinusoidal switches S5 to S8. The pairs S5/S8 and S6/S7 are turned on complementarily according the polarity of the sinusoidal.

The proposed impedance network consists of two inductors, four capacitors, and three diodes, whereas a conventional three-level quasi-Z-source NPC inverter utilizes four inductors, four capacitors, and two diodes in the q-source impedance, as discussed in. Its dc-link voltage vi can be boosted to a level twice as high as a quasi-Z- source NPC inverter. We assume VC1 =VC2 and VC3 =VC4 due to the symmetry of the impedance network.

3.3 Operation of The Single-Phase Modified Quasi-Z- Source Hybrid Three-Level Inverter

The proposed single-phase MqZS hybrid three-level inverter has two operation modes: the shoot-through state and the non-shoot-through state. The operations of the two operating states are only discussed when the output voltage is positive by conducting the switching devices S5 and S8.

1. Shoot-Through State

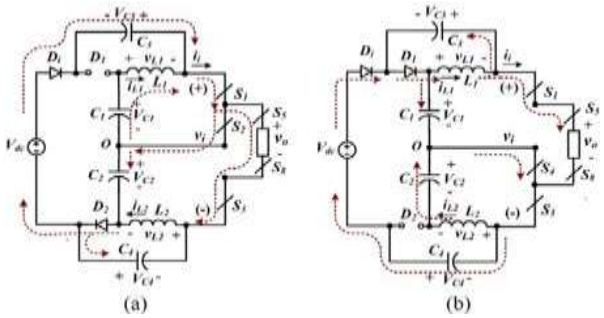

Fig.4 Equivalent circuits of the MqZS hybrid three-level inverter: (a)upper shoot-through state, (b) lower shoot- through state.

Due to the neutral-point O at the mid-point between the two series capacitors, the MqZS three-level inverter has two kinds of shoot-through state modes, an upper shoot- through state (U_ST) and a lower shoot-through state (L_ST). Figure shows the equivalent circuits of the MqZS three-level inverter in the upper shoot-through state and lower shoot-through state. In the upper shoot-through state for the interval of Tsh, the switching devices S1, S2, and S3 are turned on and the diodes Di and D2 are on, whereas diode D1 is off, as shown in Figure (a). The inductor L1 stores energy from capacitor C1 through S1 and S2, and the dc voltage source and capacitor C3 supply the energy to the load and capacitor C2. The switching devices S5 and S8 are turned on in order to generate a positive output voltage.

Two inductor voltages V_{L1} and Z, and dc-link voltage vi can be written as,

$$V_{L1} = [-V_{DC}] - V_{C3} + V_{C1} + V_{C2},$$

$$V_{L2} = [-V_{C4}]$$

$$V_i = V_{C2} + V_{C4}$$

In the lower shoot-through state for the interval of Tsh, the switching devices S1, S3, and S4 are turned on and the diodes Di and D1 are on, whereas diode D2 is off, as shown in Figure (b). The inductor L2 stores energy from capacitor C2 through S3 and S4, and the dc voltage source and capacitor C4 supply the energy to the load and capacitor C1.

Two inductor voltages vL1 and vL2, and the dc-link voltage vi can be written as,

$$V_{L1} = -V_{C3}$$

$$V_{L2} = [-V_{DC}] - V_{C4} + V_{C1} + V_{C2} = V_{C2}$$

$$V_i = V_{C1} + V_{C3}$$

2. Non-Shoot-Through State

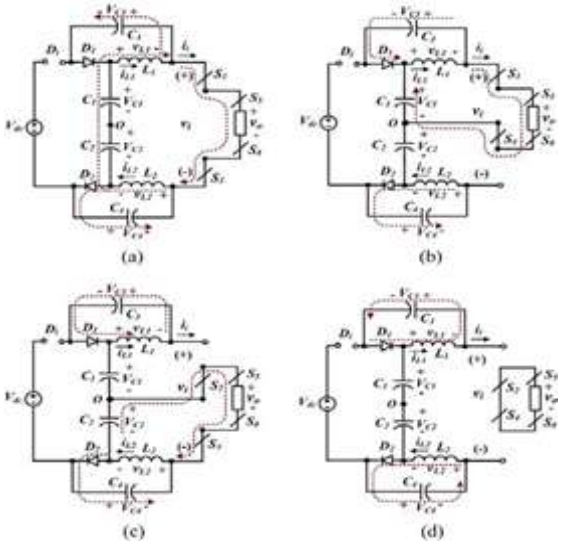

Fig.5 Equivalent circuits in the non-shoot-through state: (a) active state I, (b) active state II, (c) active state III, (d) zero state

In the non-shoot-through state for the interval of Ta, diodes D1 and D2 are on whereas diode Di is off. The non-shoot through state is divided into active state I (AS-I), active state II (AS- II), active state III (AS-III), and the zero state (ZS). Figure shows the equivalent circuits in the non- shoot-through state. In active state I, the switching devices S1 and S3 are turned on, and the maximum dc-link voltage v is supplied to the load terminal.

In active state II, the switching devices S1 and S4 are turned on, as shown in Figure (b). Both the capacitor C1 and inductor L1 transfer energy to the inverter. In active state III, the switching devices S2 and S3 are turned on, as shown in

Figure (c). Both the capacitor C2 and inductor L2 transfer energy to the inverter. Inactive states II and III, half of the maximum dc-link voltage is supplied to the load terminal, and the energies stored in the inductors L1 and L2 charge the capacitors C3 and C4, respectively. In the zero state, a zero voltage is available at the load terminal, as shown in Figure (d).

The two inductor voltages and dc-link voltage vi for the non-shoot-through state, and the output voltage vo for the four operating states can be written as

$V_{L1} = V_{C2}$

$V_{L2} = V_{C4}$

$V_i = \overline{V_i} = V_{C1} + V_{C2} + V_{C3} + V_{C4}$

$V_o = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \overline{V_i}$ for active state I

$V_o = V_{C1} + V_{C2} = 0.5\ \overline{V_i}$ for active state II

$V_o = V_{C3} + V_{C4} = 0.5\ \overline{V_i}$ for active state III

$V_o = 0$ for zero state

3. Advantage of proposed system

- High-frequency current ripple is less
- Increase the efficiency
- Reduced number of components
- Reduce in cost

4. Results

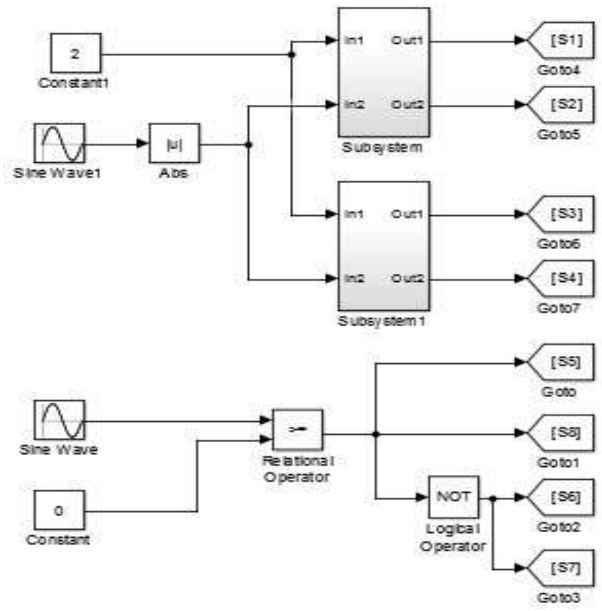

Fig.6 Simulation of PWM Generation for Three Level Inverter

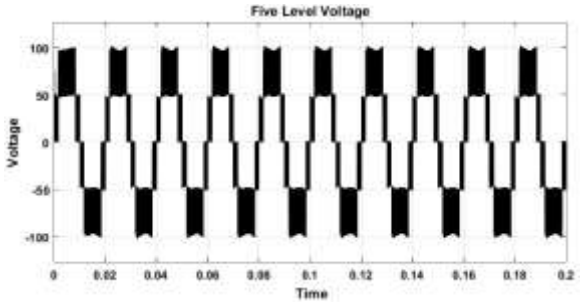

Fig.7 Vout for Three Level Inverter

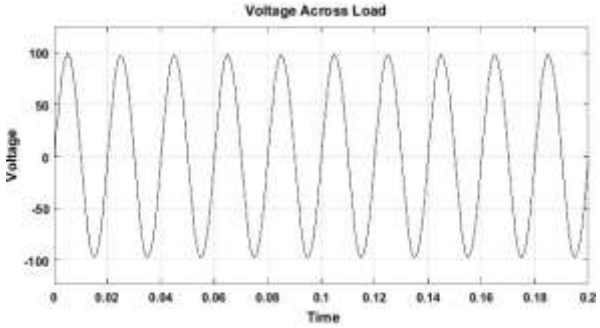

Fig.8 Vout across the Filter

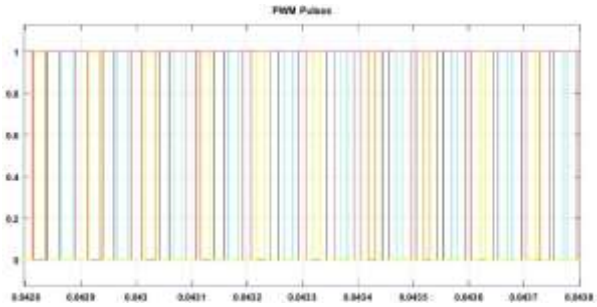

Fig.9 PWM pulses for three level Inverter

5. Conclusion

Here we proposed two novel topologies for a single- phase MqZS hybrid three-level inverter and a single-phase MqZS-CHI designed by cascading two three-level PWM switching cells in order to obtain the output voltage with nine voltage levels. Comparing with both the three-level NPC qZSI and the three-level qZS-CMI, the proposed MqZS hybrid three-level inverter reduces the number of inductors by two. Its boost factor is higher by a factor of two relative to that of the NPC qZSI, although dc source current is discontinuous. However, the voltage stress across the four low-frequency switches is twice or four times higher than that of the high-frequency switches. On the other hand, the four switches in the SPFB can be implemented with the low-frequency high-voltage switching devices, and the switching loss can be reduced.

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