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DESIGN AND IMPLEMENTATION OF HIGH SPEED, LOW POWER CHARGE SHARED RESET METHOD BASED DYNAMIC LATCH COMPARATOR USING 45nm CMOS TECHNOLOGY

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Abstract - *An analog to digital converter (ADC) is an essential building block to run the semiconductor industry. Comparator is an important component of ADCs. The high speed, low voltage, area efficient, and low power optimized comparators are very important to enhance the performance of the ADCs. This paper presents Charge shared reset method based dynamic comparator design using Cadence virtuoso 45nm technology. The main aim of the project is to design low power, high speed, optimized Dynamic latch comparator which is very useful for the electronic industries where low power and optimized performance are the prime concerns. In the proposed comparator architecture, outputs of the comparator will not go below the threshold voltage during the reset phase of the clock which will be held at a constant voltage level. Hence quicker comparison of the signals can be achieved at the start of the evaluation phase. This will significantly reduce power and delay in the design.*

Key Words: **ADC, Dynamic Comparator, Low power design, Delay, minimum area, Cadence virtuoso 45nm technology.**

1. INTRODUCTION

The continuous improvement in CMOS technology allows the researchers to manufacture completely on-chip devices without trading off the performance parameters. The comparator is the fundamental component of the ADCs. The function of the comparator circuit is to compare two same or dissimilar electrical signals. Comparators are used in wide variety of the applications such as RF communications, ADCs, memory detecting circuits, testing oscilloscope, in switching power regulators, and signal recognition systems etc. These days, where interest for portable battery operated devices is expanding, a noteworthy significance is given towards low power designs for high speed applications. Comparator is the decision making circuits which has crucial influence on the performance of high speed applications. The proposed comparator architecture is based on shared charge reset technique. The proposed architecture is a dynamic latch comparator, where output voltage level will not go less than the threshold voltage during reset phase of clock. This is a low voltage, high speed optimized comparator through which we can achieve quicker comparison between two signals. The circuit area is also optimized by using Cadence virtuoso 45nm technology. The symbol of a comparator is shown in Fig -1. The cmos comparator is well known as a decision making circuit.

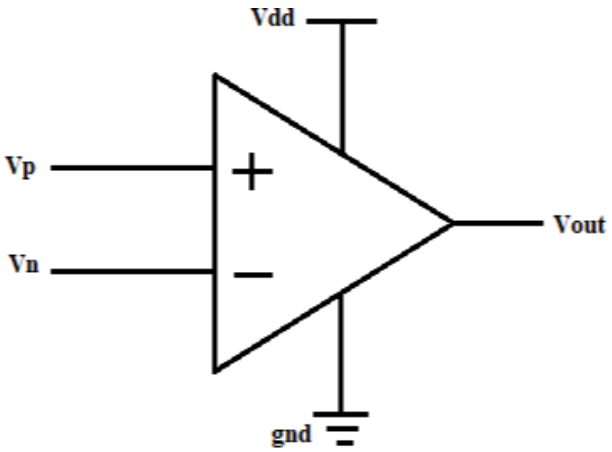

Fig -1: Comparator symbol

If Vp>Vn then the output, Vout = Vdd =logic1. If Vp<Vn then the output, Vout = ground= logic 0. The comparator converts analog input signal into digital output signal hence, comparator has vital effect on the performance of high speed applications. The low power, high speed comparators will improve the performance of ADCs. An optimized design for dynamic comparator is proposed in this project focusing on main performance parameters such as silicon area, delay, PDP, and power consumption management.

2. LITERATURE SURVEY

The variety of comparator circuits were focused from various leading technical papers are studied and discussed in this section. Sagar Kumar Vinodiya and R S Gamad [1] proposed a high speed comparator which has a differential input stage along with a latch stage. Here comparator design is optimized to get minimum power and delay. The dynamic latch comparator has delay of 0.56ns and power consumption of 96.5pw. But this comparator requires more area as it has many transistors in the circuit. The circuit was designed and tested using SCL 180nm technology by using ADE tool of Cadence. Shabi Tabassum and Anush Bekal [2] proposed a comparator, which consists of preamplifier and latch stage. This comparator architecture which helps to remove the kickback noise and dc offset voltage. The average power consumed in the design was 70μW. This design was

made in 180nm CMOS technology with the low voltage of 1V. The proposed architecture is used in Successive Approximation ADCs. Vijay Savani and N. M. Devashrayee [3] analyzed different types of dynamic latch comparators and listed various types of performance parameters. The Single tail dynamic latch comparator has high impedance at input stage and minimum static power dissipation. But this has high power dissipation and low speed of operation. The double tail current dynamic latched comparator architecture provides low offset and minimum delay. The layout of this comparator occupies more silicon area. The shared charge reset technique comparator has minimum delay and power consumption in the circuit. This comparator architecture is implemented in 90nm technology using gpdk90 technology in cadence tool which has delay of 50.9ps and power consumption of 31.80 µW. Anil Khatak, Manoj Kumar, and Sanjeev Dhull [4] introduced a Comparator with two cross-coupled Inverters for ADCs using 90nm technology. This comparator was designed using SPICE in 90 nm technology with minimum delay and power consumption. The two Cross-Coupled Inverters implemented in this comparator architecture has zero static power dissipation. This Comparator is utilized in successive approximation ADCs. Ms. Aayisa Banu S and Mr. Ramesh K [5] designed a comparator which acts as the quantizer in the ADCs applications. The proposed architecture uses CMOS Operational Amplifier design technique. The parasitic effects limits the performance the comparators, hence the parasitic effects are greatly minimized in this design. This comparator is designed by using gpdk180 technology library in Cadence tool. B.B.A. Fouzy and Bhuiyan [6] proposed pre-amplifier-latch based comparator using 0.13µm CMOS process in Design IC of Mentor Graphics environment. In order to get high speed comparator the combination of an amplifier stage and latch circuit is implemented in this comparator. The proposed comparator architecture has 0.65ns of delay, 1.5nW of power and occupies 256µm^2 of silicon space. This comparator is mainly used in area efficient, very low-power, and rapid ADCs.

2. SCHEMATIC DIAGRAM AND OPEARTION OF PROPOSED COMPARATOR

The proposed project is implemented using Cadence virtuoso 45nm tool. In all other dynamic latch comparator, during reset phase the output terminal either charged to Vdd or discharged to ground GND. In this proposed comparator uses new reset technique, in which charge is retained during reset phase. The circuit diagram of Charge shared dynamic comparator is shown in Fig -2.

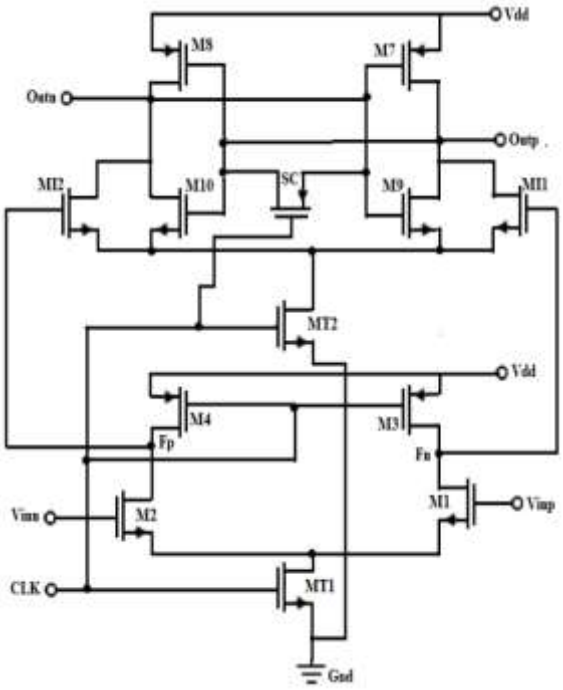

Fig -2: Circuit diagram of proposed comparator

The proposed comparator operates during reset phase (CLK=0) and evaluation phase (CLK=1) of the clock signal. When CLK = 0, the transistors MT1 and MT2 are turned OFF and both Fn and Fp terminals will be charged to Vdd through M3 and M4. Then the transistors MI1 and MI2 are turned ON. The pass transistor SC shorts the output terminals Outp and Outn during the reset phase. The pass transistor SC shares the charge between two output terminals Outp and Outn, as one of the output terminal will be at Vdd and other at Gnd after the previous evaluation phase. Hence output terminals will be held at constant voltage level. When CLK = 1, the transistors MT2 and MT1 are ON and transistors M3 and M4 are OFF. Both Fn and Fp terminals will discharge at different speed which depends on the inputs applied to the circuit. If Vinp > Vinn, the terminal Fn discharges faster than Fp and vice versa. If the potential at terminals Fp or Fn, becomes less than the threshold voltage of transistor (MI2 or MI1), the transistor MI2 or MI1 turns OFF. The latch stage of the comparator drives, one output to Vdd and other output to ground. Thus input signals can be compared at quickly during evaluation phase. This greatly reduces the delay and power consumption in the circuit.

3. IMPLEMENTATION

The comparator circuit schematic is designed and tested using Cadence Virtuoso 45nm tool is shown in Fig -3. The circuit has two input terminals (Vinp, Vinn), two output terminals (Outp, Outn), high frequency clock signal, and supply voltage of 1V. The proposed comparator is tested with different input parameters and verified for correct output. The transient response of the comparator architecture is observed by using ADE (Analog Design Environment) tool is shown in Fig -4.

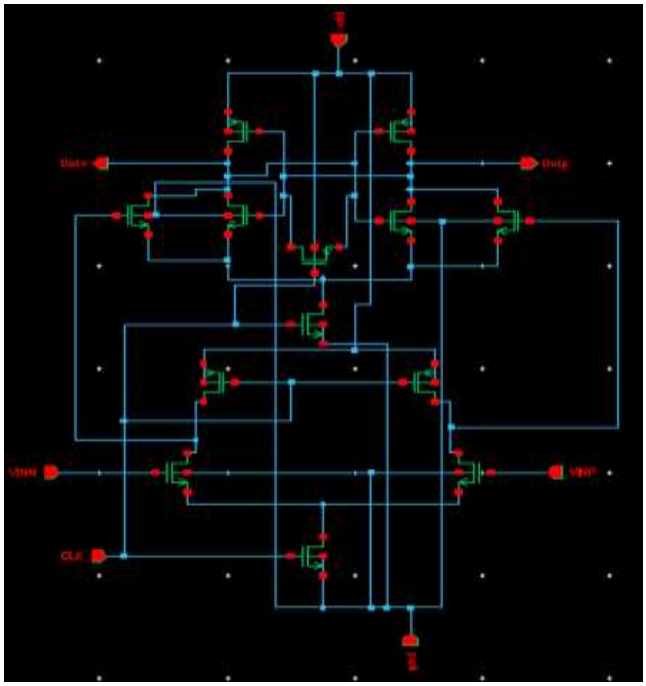

Fig -3: Circuit schematic in 45nm Cadence Virtuoso tool

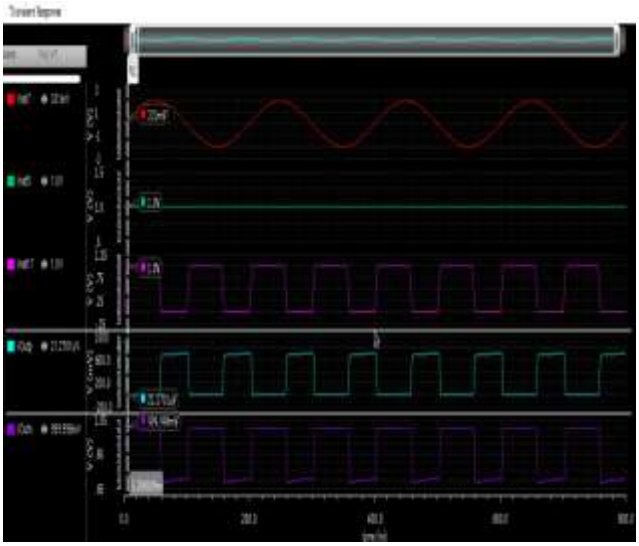

Fig -4: Transient Response of the proposed comparator

Layout of the comparator is designed using Cadence virtuoso Layout XL tool. All the layouts components need to be arranged and connected properly in order to manage the area. The layout is checked for Design Rule Check errors, made error free and Layout Versus Schematic is matched. The silicon area of this layout design is 21.56μm² is shown in Fig -5**.** Thus proposed comparator occupies minimum area when compared to other conventional comparators.

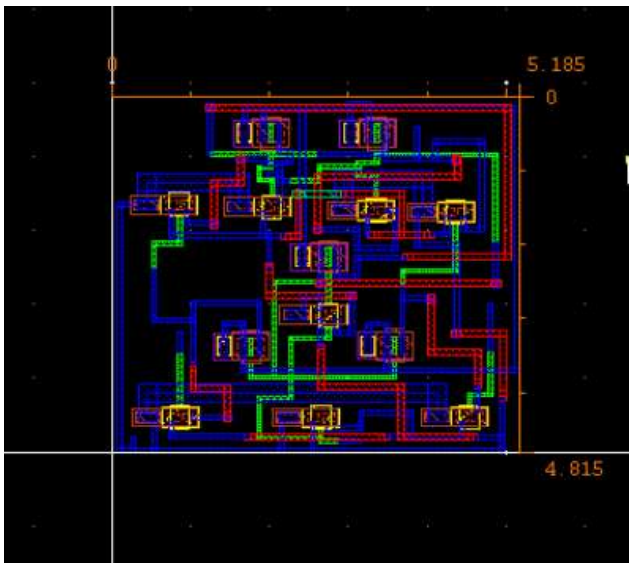

Fig -5: Layout design of the proposed comparator circuit schematic using cadence virtuoso 45nm tool

4. OUTCOME

The proposed optimized comparator has an efficient layout area, minimum delay, and power consumption when compared to other existing comparator architecture. The proposed comparator has power consumption of 128nW and delay of 22.8 ps. It operates with the low supply voltage of 1V. The comparison between the existing approaches and the proposed design is listed in Table -1

Table -1: Comparisons between existing approaches and proposed design.

Parameters	[6]	[1]	[3]	[2]	[4]	[5]	Proposed work
Technology (nm)	130	180	90	180	90	180	45
Supply voltage (V)	1.2	1.2	1	1	700 m	1	1
Average Power (W)	1.5n	96.5 p	31.8 µ	70µ	13.8 µ	0.95 µ	128.6 n
Delay (s)	0.62 n	0.56 n	50.9 p	-	1.12 µ	1.56 n	22.8p
Clock Frequency (Hz)	100 M	250 M	1G	-	-	-	10G
PDP (fJ)	0.00093	0.00005	1.62	-	-	1.48	0.0029
Area (μm²)	256	-	58.32	-	-	-	21.56

5. CONCLUSION

The proposed comparator enhances the performance of ADC and it is highly improved for high speed applications. The proposed comparator circuit is designed and tested using Cadence virtuoso 45nm technology, which has efficient layout area of 21.56 μm^2. This comparator has low power consumption of 128.6nW. Thus performance parameters are improved in the proposed design.

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