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A Fully Digital Front-End Architecture for ECG Acquisition System with Low Voltage Supply

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Abstract - *The proposed architecture presents a compact, low-power, digitally-assisted sensor interface for biomedical applications. It exploits oversampling and mixed-signal feedback to reduce system area and power, while making the system more robust to interferers. Anti-aliasing is achieved using a charge-sampling filter with a sinc frequency response and programmable gain. A mixed-signal feedback loop creates a sharp, programmable notch for interference cancellation. A prototype was implemented in a CMOS process.*

Key Words*: *anti-aliasing; mixed signal feedback loop; charge sampling

1. INTRODUCTION

Biomedical devices are becoming more popular. This is due to the rapid advancement of integrated circuit (IC) fabrication. Such devices are being used as wearable or implantable gadgets as well as monitoring equipment. Electrocardiograms (ECG), electroencephalograms (EEG), and electromyograms (EMG) are common bio-potential signals measured non-invasively or minimally invasively. Neural field potentials, in contrast, are measured using medical implants. In most cases, an analog front- end (AFE) comprising an instrumentation amplifier (IAMP) and an anti-aliasing filter is used to process these signals. Bio-potential signals can be as small as a few microvolt in magnitude, and typically reside between in frequency. This method describes a digitally-assisted sensor interface that uses a mixed-signal feedback scheme to cancel interference right of the system, while doing so in a low-power, area-efficient manner.

An area-efficient anti-aliasing filter based on charge-sampling is also presented. The overall system leverages oversampling and digital design to reduce system area and power. In fig.1.2.circuit, many of the functions that are typically implemented by analog blocks are performed by digital circuits. Using this digitally enhanced approach can help increase the flexibility of the system in removing unwanted interferences. Moreover, digital calibration techniques can be used more easily.

Eliminating the interferences at the input of the system, before substantial gain is applied, can relax the dynamic range requirements and minimize the supply voltage. This can lead to reduce the overall power consumption and area; both of which are critical for implantable and multi electrode systems. This is achieved using mixed signal feedback and digital blocks. Hence, it appears that the use of digital techniques in the implementation of these systems can lead to a better performance and better compatibility with digital CMOS technology. As can be seen, the amplifier; the only analog block that is used, consumes most of the power.

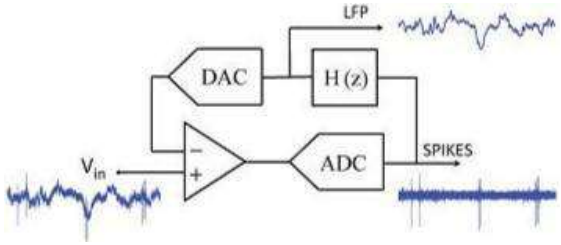


Fig-1.1 Mixed signal feedback architecture.

Hence, if we can replace the amplifier with an appropriate digital block, the circuit will be more efficient in terms of power. However, there are other issues that should be addressed before moving toward fully digital implementation. Two of these issues are as follows.

1. Removing the DC Offset Voltage of Electrodes without P*assive Elements:* In these systems, a dc offset voltage as large as 50 mV is associated with the electrodes. Typically this offset is removed by ac coupling the instrumentation amplifier with the electrode. This is not very desirable, since it requires large capacitors.

2. Providing a Solution for Anti aliasing Filter: Anti aliasing is typically done by low-pass analog filters. Box car sampling technique can be a solution for the fully digital implementation.

Motivated by the above-mentioned issues, we have designed a compact, low-power, digitally-assisted sensor interface for biomedical applications.

It exploits oversampling and mixed-signal feedback to reduce system area and power, while making the system more robust to interferers. Anti-aliasing is achieved using a charge-sampling filter with a *sinc* frequency response and programmable gain. A mixed-signal feedback loop creates a sharp, programmable notch for interference cancellation.

2. TECHNIQUES

In the proposed method we used the system of a compact, low-power, digitally-assisted sensor interface for biomedical applications is presented. It exploits oversampling and mixed-signal feedback to reduce system area and power.

2.1. Oversampling

In signal processing, oversampling is the process of sampling a signal with a sampling frequency significantly higher than the Nyquist rate. Theoretically a bandwidth-limited signal can be perfectly reconstructed if sampled above the Nyquist rate, which is twice the highest frequency in the signal. Oversampling improves resolution, reduces noise and helps avoid aliasing and phase distortion by relaxing anti-aliasing filter performance requirements. A signal is said to be oversampled by a factor of N if it is sampled at N times the Nyquist rate. There are three main reasons for performing oversampling

- Anti-aliasing

Oversampling can make it easier to realize analog anti - aliasing filters. Without oversampling, it is very difficult to implement filters with the sharp cutoff necessary to maximize use of the available bandwidth without exceeding the Nyquist limit. By increasing the bandwidth of the sampled signal, design constraints for the anti-aliasing filter may be relaxed. Once sampled, the signal can be digitally filtered and down sampled to the desired sampling frequency. In modern integrated circuit technology, digital filters are easier to implement than comparable analog filters.

- Resolution

In practice, oversampling is implemented in order to achieve cheaper higher resolution A/D and D/A conversion. For instance, to implement a 24-bit converter, it is sufficient to use a 20-bit converter that can run at 256 times the target sampling rate. Combining 256 consecutive 20-bit samples can increase the signal-to-noise ratio at the voltage level by a factor of 16 (the square root of the number of samples averaged), effectively adding 4 bits to the resolution and producing a single sample with 24-bit resolution.

- Noise

If multiple samples are taken of the same quantity with uncorrelated noise added to each sample, then averaging *N* samples reduces the noise power by a factor of 1/*N*.[4] If, for example, we oversample by a factor of 4, the signal-to-noise ratio in terms of power improves by factor of 4 which corresponds to a factor of 2 improvement in terms of voltage. Certain kinds of A/D converters known as delta-sigma converters produce disproportionately more quantization noise in the upper portion of their output spectrum. By running these converters at some multiple of the target sampling rate, and low-pass filtering the oversampled signal down to half the target sampling rate, a final result with *less* noise (over the entire band of the converter) can be obtained. Delta-sigma converters use a technique called noise shaping to move the quantization noise to the higher frequencies.

2.2 Mixed Signal Circuit

A mixed-signal integrated circuit is any integrated circuit that has both analog circuits and digital circuits on a single semiconductor die. In real-life applications mixed-signal designs are everywhere, for example, a smart mobile phone. However, it is more accurate to call them mixed-signal systems. Mixed-signal ICs also process both analog and digital signals together. For example, an analog-to-digital converter is a mixed-signal circuit. Mixed-signal circuits or systems are typically cost-effective solutions for building any modern consumer electronics applications. Mixed-signal system-on-a-chip (AMS-SoC) can be a combination of analog circuits, digital circuits, intrinsic mixed-signal circuits (like ADC), and Embedded Software. Integrated Circuits (ICs) are generally classified as digital (e.g. a microprocessors) or analog (e.g. an operational amplifier). Mixed-signal ICs are chips that contain both digital and analog circuits on the same chip. This category of chip has grown dramatically with the increased use of 3G cell phones and other portable technologies.

Mixed-signal ICs are often used to convert analog signals to digital signals so that digital devices can process them. For example, mixed-signal ICs are essential components for FM tuners in digital products such as media players, which have digital amplifiers. Any analog signal (such as an FM radio transmission, a light wave or a sound) can be digitized using a very basic analog-to-digital converter and the smallest and most energy efficient of these would be in the form of mixed-signal ICs. Mixed-signal ICs are more difficult to design and manufacture than analog-only or digital-only integrated circuits. For example, an efficient mixed-signal IC would have its digital and analog components share a common power supply.

However, as one can imagine, analog and digital components have very different power needs and consumption characteristics that make this a non-trivial goal in chip design.

2.3. Programmable-gain Amplifier

A programmable-gain amplifier (PGA) is an electronic amplifier (typically an operational amplifier) whose gain can be controlled by external digital or analog signals. The gain can be set from less than 1V/V to over 100V/V. Examples for the external digital signals can be SPI, I^2C while the latest PGAs can also be programmed for offset voltage trimming, as well as active output filters. Popular applications for these products are motor control, signal and sensor conditioning.

2.4. Sinc Anti-aliasing Filter

Modern biomedical systems usually digitize the signal of interest using an ADC. To avoid corrupting the desired signal, an anti-aliasing filter is used to attenuate aggressors and noise components that would otherwise be frequency translated to the discrete-time signal band through the sampling process. Since sharp digital filters are typically

more area and power efficient, it is not necessary to use analog filters to eliminate all aggressors before sampling. It *is* critical, however, to eliminate aggressors that would otherwise alias into the signal band. It illustrates a continuous-time (CT) filter frequency response that would eliminate *corrupting* aggressors, but not other broadband ones. The sinc frequency response created by charge sampling creates precisely this type of frequency response since the notches are placed where corrupting aggressors would lie. However, to make the notches wide enough such that sufficient attenuation is achieved on the entire signal bandwidth, oversampling is required. The main cost of oversampling is increased power consumption; particularly in the ADC. However, recent advances in ADC design have led to ultra-low energy-per-conversion step figures-of-merit (FOM) such that the ADC power consumption can be made significantly lower than other components in a typical narrowband biomedical system. In addition, for a given dynamic range requirement, a lower *effective number of bits* (ENOB) can be used when oversampling is employed.

Filter Architecture:

In this section we describe a sinc filter that provides programmable gain and achieves anti-aliasing by exploiting oversampling. It comprises a linear transconductor, two capacitor banks, and two reset switches. The input of the SAAF, is a differential continuous-time signal which is the output of the IAMP. The SAAF output, is a differential signal that is digitized by an external ADC through an on-chip ADC driver. Each period starts by quickly resetting the voltage across each capacitor to the common-mode voltage, such that the differential output voltage is zero. The transconductor converts the filter's input voltage to a current, and the current is integrated.

$$V_{\text{out}}(f) = \frac{T_s}{2T_{\text{int}}} V_a(f)\text{sinc}(\pi f T_s) e^{-\pi f T_s}$$

The notches of the *sinc* filter lands at integer multiples of, which is precisely what an anti-aliasing filter. In addition, the SAAF is a linear-phase, non-dispersive filter, so the only effect it has on the phase of the input signal is to impart a delay of the attenuation at multiples of is theoretically infinite, and is substantial in the vicinity of the notches. At, the amount of attenuation is approximately.

Filter Linear Range and Bias Current Selection:

Since the IAMP preceding the SAAF provides significant gain, the noise specifications of SAAF are greatly relaxed. The linearity requirements, however, require careful selection of the transconductor bias current. Generally, the transconductor Topology is very linear due to negative feedback. However, if an insufficient amount of bias current is used, clipping can occur that introduces distortion. To prevent current clipping, each of the four branches containing or should use a bias current, such that, Where represents the largest input signal peak differential amplitude expected. The gain of the SAAF, should be as large as possible, while satisfying this condition

$$G_\phi \leq \frac{\max(V_{\text{ADC}})}{\max(v_i)}.$$

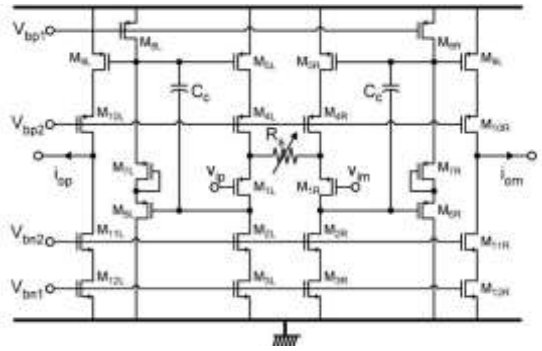


Fig-1.2(a). Front-end architecture.

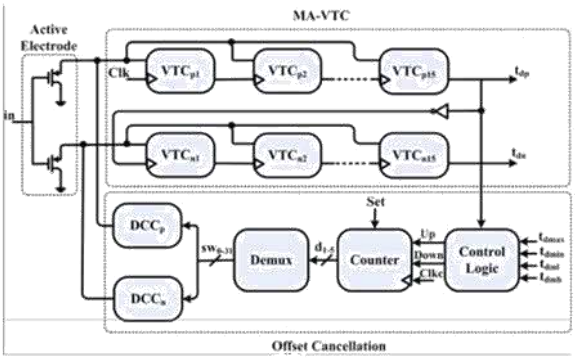


Fig-1.2(b). Digital front-end architecture.

2.5. Interference Cancellation

The Power consumption in a signal processing system is often determined by dynamic range requirements. The dynamic range is a measure of the ratio between the largest signal that can be handled by the system without significant distortion and the minimum detectable signal set by the input-referred noise. The specifications for the minimum detectable signal are typically set by the signal being measured, but the largest signal that must be handled is often set by interference. If the high end of the dynamic range is set by an interfering signal and is filtered out near the front end, the dynamic range requirements of subsequent stages can be relaxed and their power consumption reduced. These observations motivate the design of a system that filters out large interferers near the front-end, while minimally impacting the signal band of interest. We emphasize PLI as an important example, but other interferers may be present at different frequencies and of different bandwidths. It is therefore important for the interference cancellation method to be easily configurable.

3. RESULTS

3.1 SOFTWARE - TANNER EDA

Schematic design of Inverter: Schematic Design: There are many phases or progressions of a design. A common term you will hear when working with a Designer is "Schematic Design". This phase is early in the design process. Schematic Design establishes the general scope, conceptual ideas, the scale and relationship of the various program elements. The primary objective of schematic design is to arrive at a clearly defined feasible concept based on the most promising design solutions. Pre layout simulation: After schematic design you have to check whether your design match with the specification required or not. That's why you need to simulate the design which is called Pre layout simulation. For simulation go to>> tools>> T-spice>> 'ok'

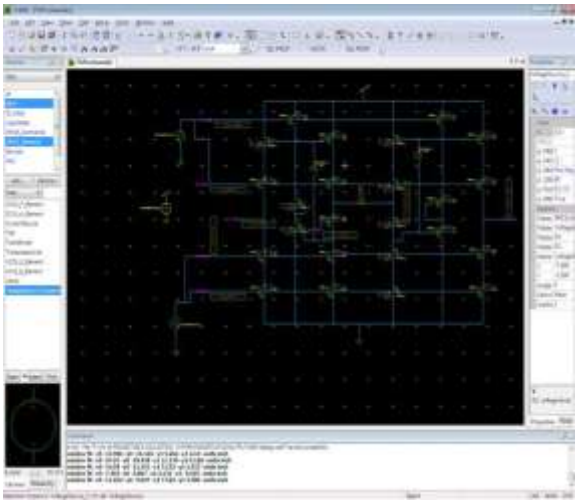
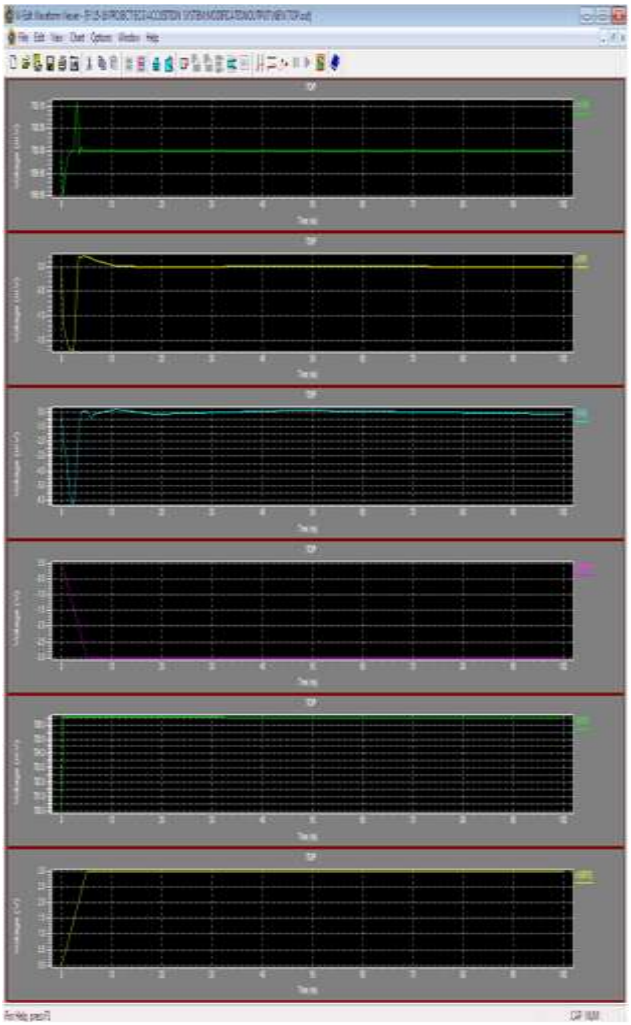


Fig 1.3. Circuit diagram

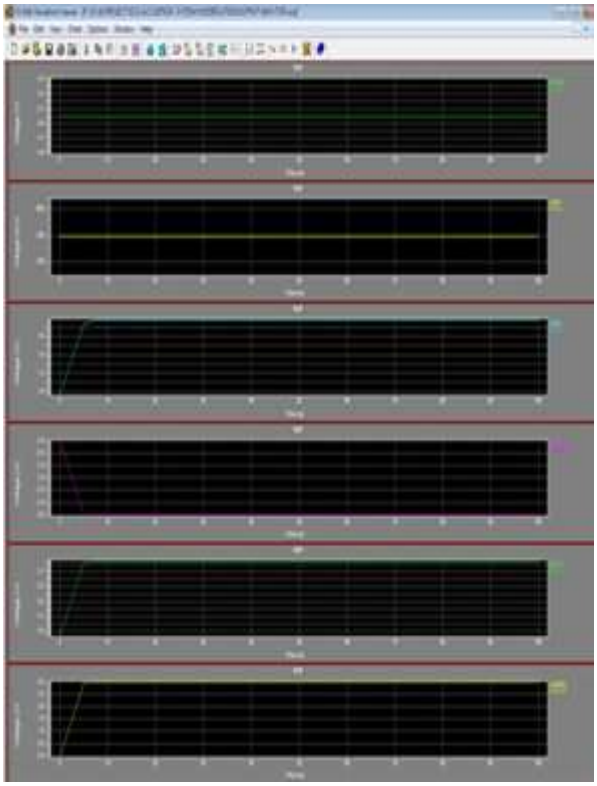
3.2 OUTPUT



S.N0	VOLTAGE	CURRENT	POWER
1	700.00000m	8.02X10^13uA	4.61W

HIGH INPUT VOLTAGE IS APPLIED:

S.NO	VOLTAGE	CURRENT	POWER
1	5.00000	13.48X10^13	6.7 W



4. CONCLUSION

This method presents a compact, digitally-assisted sensor interface for biomedical applications with interference cancellation capabilities. A custom chip comprising a low-power IAMP, *sinc* anti-aliasing filter and feedback DAC was used as part of the closed-loop system. The use of charge-sampling achieves substantial anti-aliasing in an area-efficient manner, while providing up to programmable gain and a frequency response that is independent of component parameters.

Finally, by canceling interferers at the system, the dynamic range requirements of the forward path blocks are relaxed, enabling power savings and low voltage operation.

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BIOGRAPHIES

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