

# A Digital Down Converter on Zynq SoC

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**Abstract** - A typical communication system requires a receiver consisting of a digital down converter which mixes and down samples the received high sampled data for easy processing. The DDC developed in this work is for Air Borne radar receivers. When compared to all the signal processing techniques involved in a radar receiver, the performance of a DDC is significant in extraction of target data. To maximize the performance of DDC, the implementation is done on a System on Chip (SoC) which meets the flexibility of a processor and programmability of a FPGA. In this work, a DDC is developed with two stage decimation and filtering. The order and type of the filters were optimally designed for efficient resource utilization. Additionally, a digital synthesizer is developed and taken as inputs for the DDC. This work presents a complete DDC model with optimized decimation and filtering stages in comparison with different implementations.

**Key Words:** Digital Down Converter, System On Chip, FPGA, LFM, Direct Digital Synthesizer, FIR filter

## 1. INTRODUCTION

A digital down converter takes a band limited high sample rate digitized signal, mixes to a lower frequency and down samples to a required sample rate with efficient filtering. The Digital Down Converter (DDC) has become the cornerstone technology for all the existing communication systems. Over the past several years, there was tremendous development in the digital signal processing systems in terms of flexibility, processing capability and power consumption. So the implementations of the DDCs have started on several platforms like DSPs, GPUs, ASICs and FPGAs by improving their performances. The work presented in [1] has developed a multi-channel IF signal processing DDC based on a DSP but has issue with signal synchronicity. The GPU based implementation [2] could not meet the speed and programmability. The ASIC based implementation [3] could achieve the advantages a FPGA. The novel architectures provided in [4], [5], [6], [7] and [8] are appreciated but they could not meet the specifications of air borne radars, where there is a requirement of compact on-field programmable devices. So the architecture designed and implemented in this paper consisted an optimal solution for the digital down conversion of air borne radar receivers. The model also presented a waveform generation which can be used as an input for the down conversion chain.

## 1.1 Digital Down Conversion Model

When compared to its analog counterpart, DDC is widely used in the recent radar receivers for its stability and consistency in amplitude and phase of the output signals. A DDC achieves this by Mixing to shift the signal spectrum from the selected carrier frequencies to baseband, Decimation to reduce the sample rate and Filtering to remove adjacent channels, minimize aliasing, and maximize the received signal-to-noise ratio (SNR)

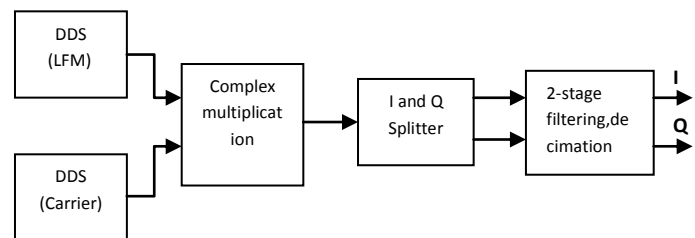


Fig -1: Proposed DDC Model

Generally, the IF received after LNA and IF amplification will be beaten with a carrier signal which is synchronized with transmitter pulse. The required baseband signal is extracted by this mixing operation and is given to a low pass filter to extract the desired down converted frequencies. The resultant signal is then decimated to a lower sampling rate with required decimation rate. But in this model, the high sampled IF is generated using a synthesizer to check the operation of the system. This synthesizer can be used in the transmitter part when it is typically implemented. The proposed architecture is the basic implementation model which used DDS, complex multiplier and FIR filter stages which included decimation.

## 1.2 Waveform Generation

In a radar system, the choice of a radar waveform plays an crucial role in detecting the target. The transmitter synthesizes the high bandwidth data with selected pulse compression techniques for efficient detection. The pulse compression technique used in this paper is Linear Frequency Modulated Wave (LFM). It is generated at a pass band with high sampling rate with the help of control logic developed in this work. In radar applications, linear chirp is the most typically used signals to achieve pulse compression. In LFM, the frequency linearly increases or decreases across the pulse. The instantaneous phase of the chirp signal is expressed as:

$$\Phi(t) = 2\pi(f_0t + \frac{1}{2}kt^2)$$

Where  $f_0$  is the carrier frequency and  $k$  is the frequency sweep rate related to pulse duration  $T_p$  and Bandwidth  $B$  as

$$K = B/T_p$$

The instantaneous frequency is given by

$$f(t) = d/dt(\Phi(t)) = f_0 + kt$$

The instantaneous frequency is a linear function of time, and hence is called as linear frequency modulation. So the difference in the frequencies in a pulse can be achieved by changing the phase of the signal. The compiler core which is used to generate the chirp waveform is the DDS Compiler Core which takes in the phase increment values and produces a frequency difference in the pulse for the required bandwidth, hence the chirp is obtained.

### 1.3 Mixing

The mixing operation for the DDC is one of the important factors which decide the precision of the output. It involves a complex multiplication, hence the bit growth and more resource utilization. For the received signal to bring down to the baseband, we require a synchronous carrier single tone to multiply with it. This mixing signal is generated by a local oscillator or more precisely, a numerically controlled oscillator (NCO). A frequency mixer accepts two signals, one input signal and one mixing signal that is generated by a local numerically controlled oscillator. The mixer then multiplies these signals together and output signals at the sum and the difference of the frequencies which are for the up and down conversions respectively. The down conversion only requires the difference term and the implementation is done accordingly.

### 1.3 Decimation and Filtering

After the mixing operation, the primary objective is to decrease the sampling rate of the signal for easier handling of the signal. Decimation is a technique used to reduce the number of samples in a system. It includes two steps: a low pass anti-aliasing filter and down sampling. As down sampling reduces the sampling frequency, it is important to make sure that the Nyquist sampling theorem is still satisfied otherwise aliasing will occur. For that reason, a low-pass filter as an anti-aliasing filter is utilized before the down sampling. This process determines the SNR and dynamic range of the system. Also, the order of the filter determines the resource utilization of the system. Hence, the filtering parameters has to be carefully determined.

## 2. IMPLEMENTATION

The hardware platform used in this work is Xilinx Zynq All Programmable System-on-Chip. The Zynq SoC integrates an ARM dual Cortex-A9 based processor system with Xilinx 7-series FPGA fabric and by doing so it provides the power, performance and capacity benefits of an ASIC combined with the hardware programmability benefits of an FPGA. The programmability of the logic is done on FPGA part (PL) in Xilinx Vivado IDE tool IP integrator, whereas the application is developed in Xilinx SDK. This work is developed as a bare metal application.

### 2.1 Block Design

The block design implemented in the IP integrator consists of the IPs which was provided by the Xilinx. The customization and control is done by the custom IPs in which the custom logic is developed for given specification.

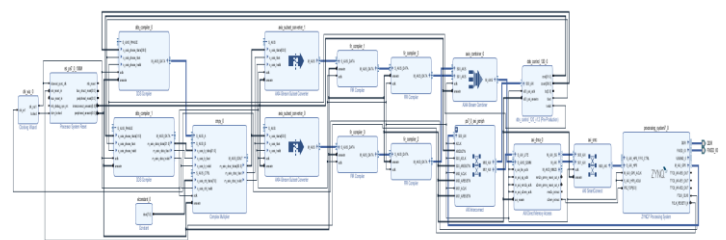


Fig -2: Proposed DDC Block design in Vivado

The design shown in the fig 2 is the optimized design with some of the customized IPs. The ddc chain takes the inputs from the DDS compilers and mixes using Complex multiplier compiler and then the resultant split I and Q components are decimated and filtered using the FIR compiler.

## 3. RESULTS

The results show the simulation and the implemented outputs. The simulation is observed in the Xilinx Vivado simulator and the implemented outputs are collected from the serial port of the SoC and are analyzed using MATLAB. The DDC chain is also designed in the MATLAB using available DSP toolkit and the results are compared.

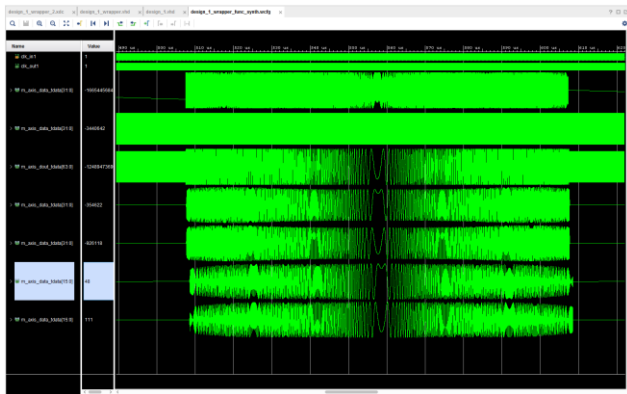


Fig -3: Simulation results at every stage

The prominent issue considering the down conversion is the bit slicing which has to be done in every stage. The outputs significantly lose its gain at every stage. Hence the re-quantization has to be done efficiently to avoid the loss. The resource utilization also varies according to the re-quantization which reduces the implementation cost

Table -1: Resource Utilization

RESOURCES	FULL PRECISION (48-bit)	RE-QUANTIZED (16-bit)
DRAM	1526	1490
BRAM	469	9
SRAM	402	390
DSP	77	77

The above results showed the drastic improvement in resource utilization in terms of BRAM which significantly contributes to the area utilization.

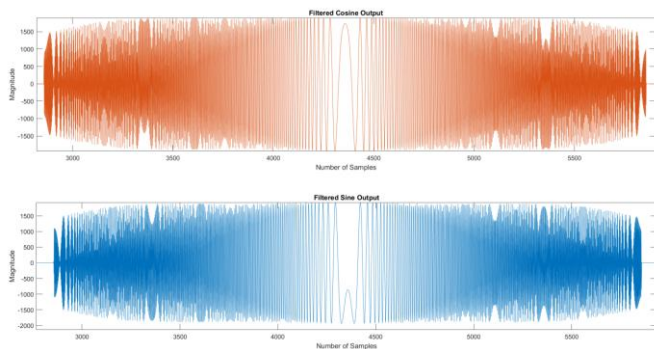


Fig -4: The optimized filter I and Q components

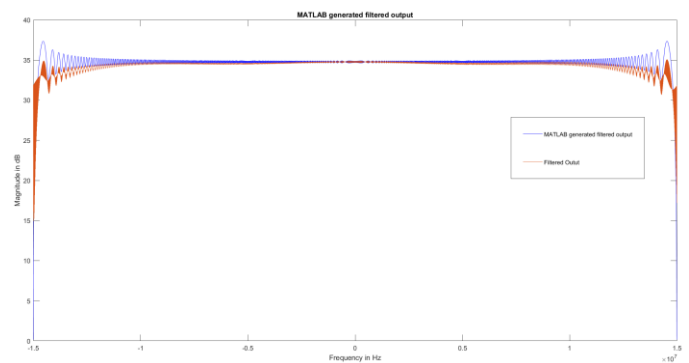


Fig -5: Frequency Spectrum Comparison of obtained and MATLAB generated

The figure 5 shows the comparison of the comparison frequency spectrum of the ideal and generated I and Q waveforms. The spectrum droop is comparatively is very less even though there is a tremendous bit slicing in the down conversion stages. The SFDR achieved is around 70 dB which is fair enough for the practical systems.

#### 4. CONCLUSIONS

This work showed the efficient way of implementing the Digital Down Converter and high bandwidth waveform generation with fair SFDR. To save hardware the design uses a cascade type design and re-quantization between the multiplication steps. The work shows that the re-quantization does not degrade the performance out of specification. The final conclusion is that the proposed architecture meets all requirements.

#### REFERENCES

[1] BoHuang, "Design and Implementation of Multi-channel Digital Down-converter Based on DSP", 2011 International Conference on Computer Science and Network Technology

[2] Xiao Ma, Lixia Deng, Yuping Zhao, "Implementation of a Digital Down Converter Using Graphics Processing Unit", Proceedings of ICCT2013

[3] Naagesh S. Bhat, "DESIGN AND ASIC IMPLEMENTATION OF DUC/DDCFOR COMMUNICATION SYSTEMS"

[4] Shyh-Jye Jou, Shou-Yang Wu, and Chorng-Kuang Wang "Low-Power Multirate Architecture for IF Digital Frequency Down Converter", IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: ANALOG AND DIGITAL SIGNAL PROCESSING, VOL. 45, NO. 11, NOVEMBER 1998

[5] Long Pang, Bocheng Zhu He Chen, Yizhuang Xie "A Highly Efficient Digital Down Converter in Wide Band Digital Radar Receiver", ICSP2012 Proceedings

[6] Hanyu Wang, Jinxiang Wang, Yu Lu, Fangfa Fu, " *An Efficient Low-cost Fixed-point Digital Down Converter with Modified Filter Bank*", 2013 IEEE

[7] Xue Liu, Xin-Xin Yan, "*Design and FPGA Implementation of a Reconfigurable Digital Down Converter for Wideband Applications*", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 25, NO. 12, DECEMBER 2017