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Design of CMOS LDO Regulator in LTspice using Miller Compensation Method

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Abstarct: *LDO regulator is a linear regulator which derives a small differential voltage, whose output voltage is very close to the supply voltage. An LDO is a DC regulator which gives a constant output voltage for a range of input voltages. In this paper, the design is simulated in LTspice for 180nm technology process. The main blocks to design an LDO regulator are error amplifier, a reference voltage block, potential divider and a pass element. The series pass element used in the design is the PMOS. The load used supports for the range from few micro amperes to 10mA. The proposed design is for 1.8V input with an output voltage 1.5V and the dropout voltage of 0.3V.*

Keywords: opamp, LDO, potential divider, reference voltage vref, vfb, vdropout and vout.

1. INTRODUCTION

In the past decades, the scaling down of device made us understand the emergence of power management circuits in many electrical or electronic circuits. Due to scaling of device parameters the IC's supply voltage's also need to be scaled down. Here the LDO regulator is made possible to use for one of the power converters in an integrated design. In such requirements the regulators play a very important role for shifting in voltages. Usually there are two types of regulators, the normal or unregulated linear regulator and the LDO regulator. For any IC chip design we choose the LDO regulator since which provides a constant output voltage that is sufficient and stable to make the device function in a normal way[1][2]. Whereas, the unregulated LDO regulator varies the voltage as the load varies which is not suitable to use since, it might damage the device IC's by exceeding the voltage range in low load condition and not function properly in large load conditions.

The error amplifier used in the design should have a large bandgap, so that the output voltage is constant for a range of inputs. The error amplifier is simply an differential amplifier/ opamp which is used to correct error between the feedback voltage and the reference voltage. Usually the design of opamp. Should have large gain to get an constant output voltage. The series pass element can be a MOSFET or BJT. Due to temperature sensitivity and a controlled device we choose the MOSFET. The enhancement type PMOS/NMOS can be used for the design of an LDO regulator[4]. The NMOS pass element as a voltage drop in it which doesn't provide strong1(VDD) instead it provides VDD-Vth. Additionally, when used, it gives the voltage drop across the Vds. In the proposed design we use a PMOS device as series pass element. The design should have a 1. The .Allowable range of input voltage for a constant output voltage. 2. It should give a very small dropout voltage. 3. The design should be applicable for large loads.

LTspice is a simulation software for analog circuits which is developed by linear technology and analog devices. It is a freeware used by all to perform simulation of MOSFET circuits for high performance. The LTspice software is helpful in developing a device model and using it in other design by importing it. Datasheets are available for various process technologies to know the minimum and maximum scale values for various components and the device supply.

2. BASIC LDO REGULATOR

LDO regulator are linear regulators which require very less voltage difference between its input and output legitimately manage the input voltage, the block diagram of basic LDO regulator is as shown in fig 1.The LDO block consists of an error amplifier commonly known as the differential amplifier, a pass element, the potential divider, reference voltage and the load. The LDO to work for large loads must consistently have a good bandgap[3].

3. DESIGN OF TWO STAGE OPAMP

The design of two stage opamp for 180nm technology is as shown in fig 2. All the MOSFETs are being operated in saturation region. M1 and M2 are the noninverting and inverting input terminals of opamp. The MOSFETs M3 and M4 act as the load for the input stage[9]. MOSFETs M5 and M8 are the used for biasing through current source I1. The Mosfet M6 and M7 act as the output stage, which is used to improve the gain of opamp at drains of M2 and M4.

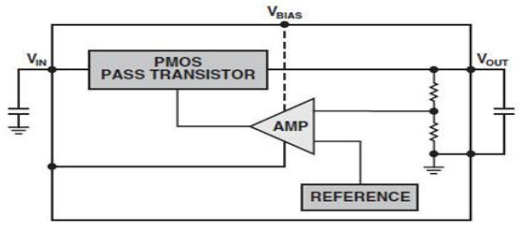

Fig1: Block diagram of LDO.

The capacitor C1 is the Miller capacitor which is .22 times of the load capacitance (C2). The length of all the MOSFETs is 1um. Supply voltage is 1.8V, the biasing current used is 5uA, C1 is 3pF and C2 is 20pF. The gain of 70db is obtained as shown in fig 5.

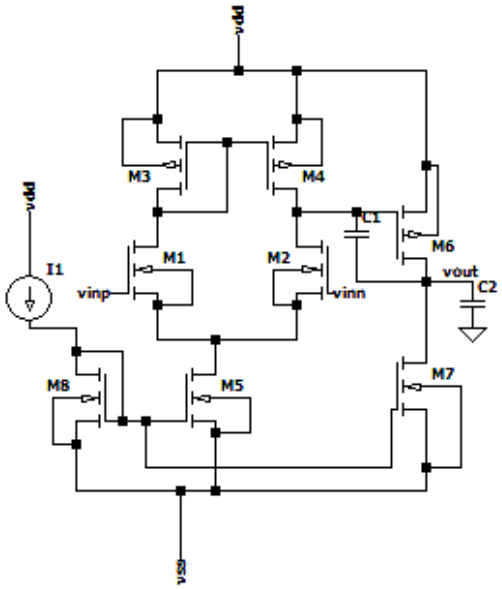

Fig 2: Design of pomp.

4. DESIGN OF LDO REGULATOR

In this paper, the design of LDO regulator is shown in fig 3. The above design differential amplifier/opamp as shown in fig 2 is used in main design of LDO. The MOSFET M9 is the pass element used in LDO. The different blocks of LDOs are as follows.

4.1THE VOLTAGE REFERENCE

The voltage reference sets the working point of the error amplifier, which is the beginning stage of all the controllers. The reference voltage is chosen to be 900mV. The reference voltage is given as one of the inputs for the error amplifier MOSFET(M1).

4.2 ERROR AMPLIFIER DESIGN

The opamp designed is to have a large bandgapand and amplify the difference of voltage from both the input terminals M1 and M2. The design of this block should draw less current. The Miller compensation method is used to improve the frequency bandwidth. The inverting input terminal takes the scaled value of the potential divider known to be feedback voltage.

$$C1 \geq 0.22CL.$$

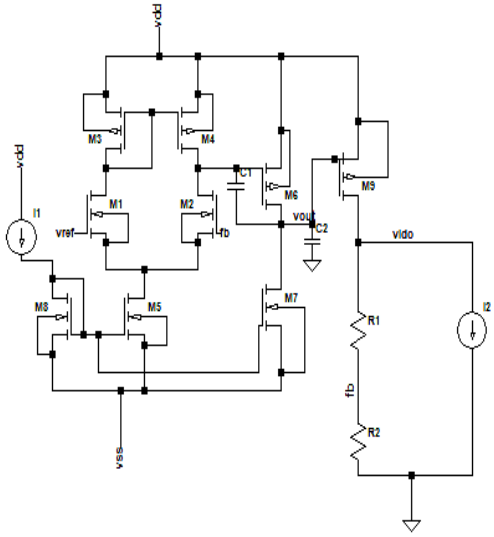

Fig3: Design of LDO Regulator.

4.3 FEEDBACK NETWORK

Resistive feedback network is used at the output of an LDO regulator to scale the output voltage for the examination against the reference voltage V_{ref} by the error amplifier.

The scaled voltage required is to be close to the reference voltage. Since the reference voltage is fixed. The feedback voltage scared is given as

$$\mathbf{Vfb = Vldo \times R2/(R1 + R2)}$$

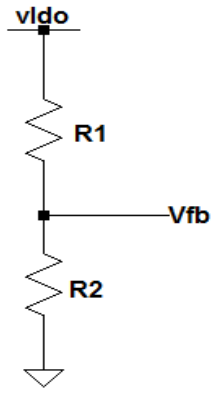

Fig4: potential divider.

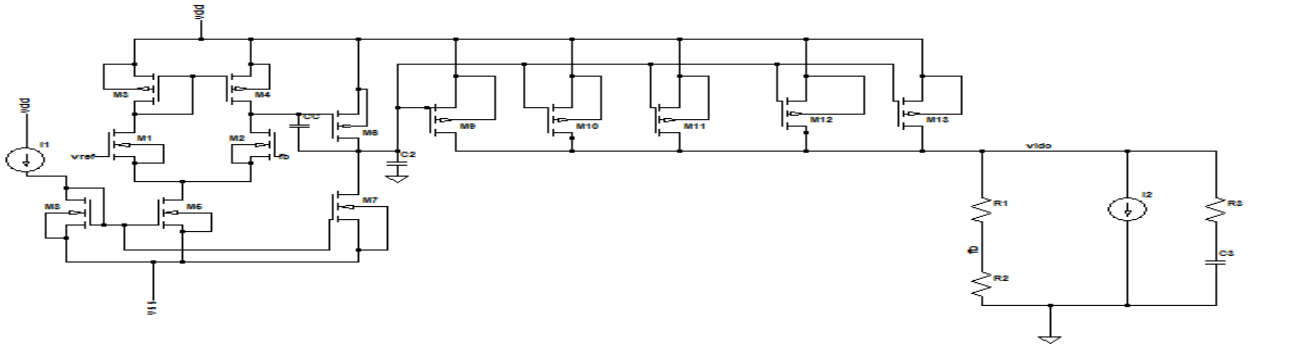

Fig 5: Design of LDO regulator for large loads.

4.4 SERIES PASS ELEMENT

The pass element is used to transfer the input signal to pass to the load. Pass element drives large currents to the load. In this design the pass element used is a PMOS device. Since the PMOS device has strong VDD when compared to NMOS devices.

The design of LDO regulator shown in fig 3 will give an output voltage vldo=1.5V for an load current source of 5mA. The supply voltage vdd=1.8V. The length of all mosfet's in the design is 1um. The design of the width is designed as per the equations of opamp[7]. The output voltage is constant for range of input voltages from 1.5-2.2V. Output voltage V_{LDO}=1.5V.

The LDO regulator gives an output volatge 1.5V which is cosntant for the cureent source load of few uA's to 5mA . To enechance the design for larger load the length of the MOSFET can be increased or the MOSFET can be connected in parallel to have a stable output for large loads upto 10mA curerent sourceas shown in fig 5.

5. Technology parameters

Parameters	Range (fig3)	Range (fig5)
Supply volatge	1.8V	1.8V
Input range	1.5-2.2V	1.5-2.2V
Load current	100uA-5mA	100uA-10mA
Bais current	5uA	5uA
Gate length	1um	1um
Output capacitor	20pF	20pF

Design values

Mosfets	W/L
M1	1.5µ/1µ
M2	1.5µ/1µ
M3	15µ/1µ
M4	15µ/1µ
M5	10µ/1µ
M6	60µ/1µ
M7	60µ/1µ
M8	10µ/1µ
M9	120µ/1µ
M10	120µ/1µ

M11	120µ/1µ
M12	120µ/1µ
M13	120µ/1µ
Miller Capacitor C_C	3pF

Comparison table

Parameters	Proposed design	2017[5]	2019[2]
Supply voltage	1.8V	1.8V	2.1-3.3V
Input voltage	1.8-2.2V	1.8-3.6V	2.1-3.3V
Output voltage	1.5V	1.8V	1.8V
Reference voltage	0.9V	1V	1.3V
Dropout voltage	0.3V	0.5-1.2V	0.4-0.6V
I_{load}	10mA	-	30-50mA
Miller capacitance	5pf		100pF

6. Results

The transient response of the error amplifier is shown in fig 6.The output voltage amplified from peak to peak of supply voltage. The gain of 70 db is obtained from the design as shown in fig 7.

The transient response of LDO regulator is as shown in fig 8 for 5mA current source load. The output voltage vldo obtained is 1.5V which is constant for a range of supply voltage. DC response of the proposed design is shown in fig 10. The power consumption of LDO regulator is as is shown in fig 11.

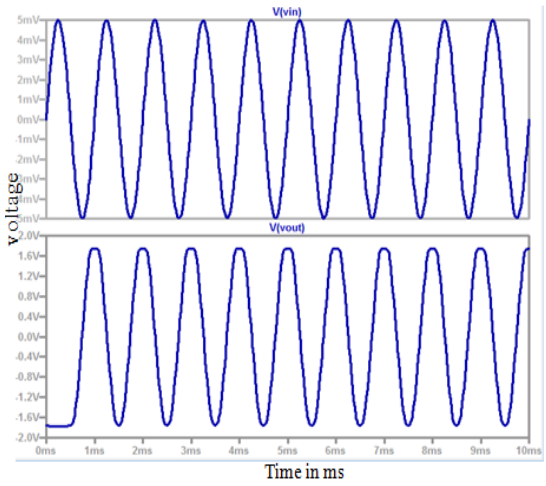

Fig6: Transient response of opamp.

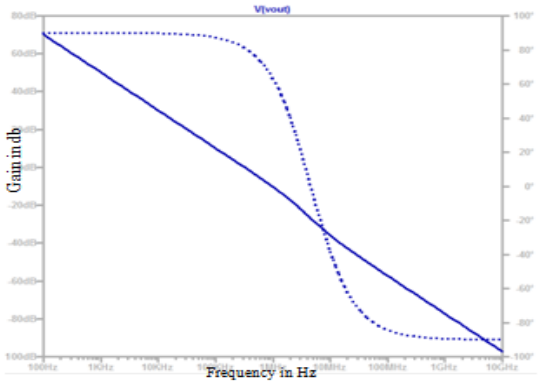

Fig7: Gain plot of opamp.

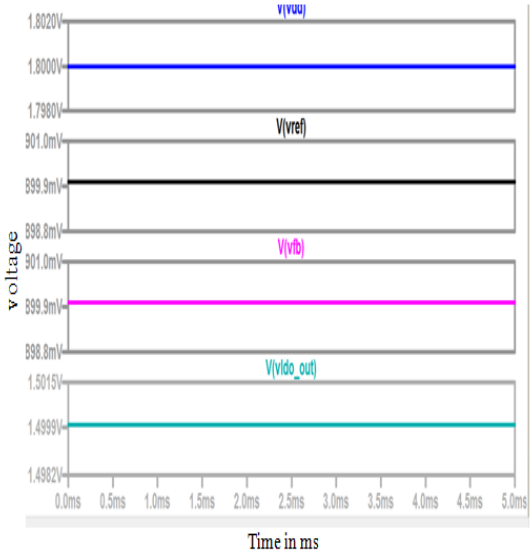

Fig8: Transient response of LDO Regulator for 5mA load.

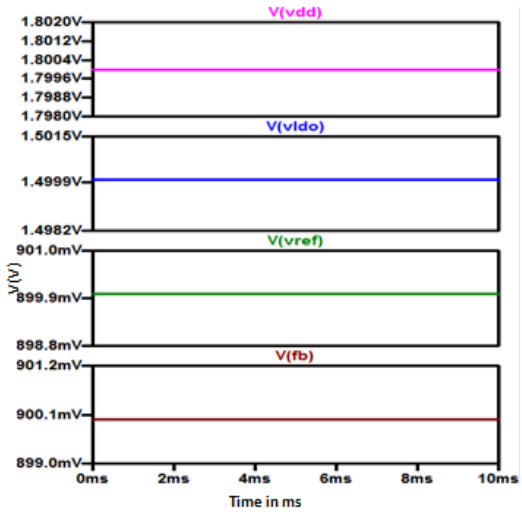

Fig 9:Transient response of LDO Regulator for 10mA load.

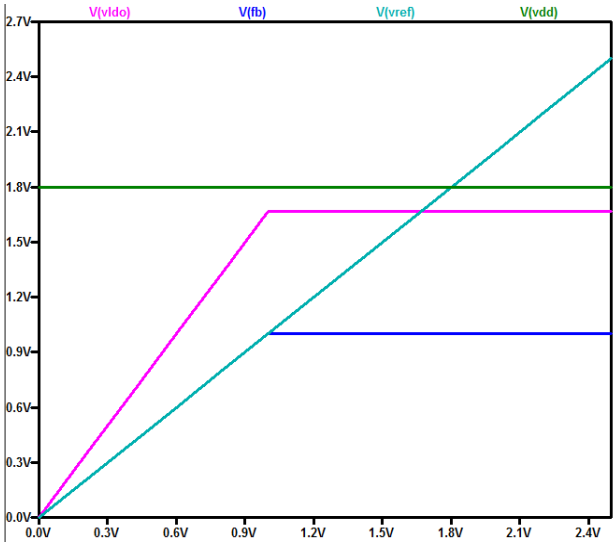

Fig10: DC response of LDO regulator.

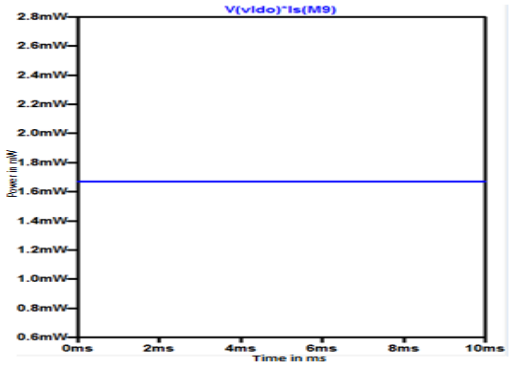

Fig11: power consumed by LDO regulator for 5mA load.

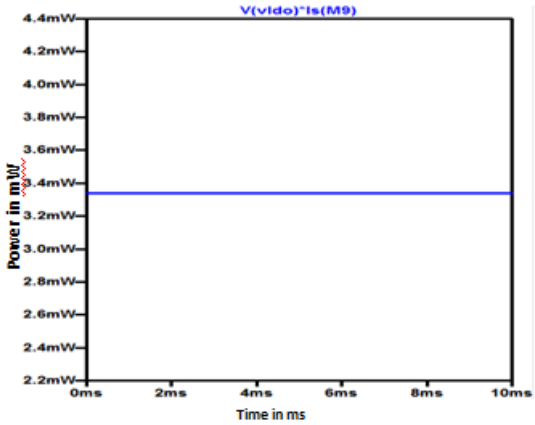

Fig 12: power consumed by LDO regulator for load 10mA.

The transient response for different current loads is shown in fig 8 and 9 were the output voltage is still 1.5V for 5mA load design in fig 3 and 10mA design in fig 5. The power consumption is more for 10mA laod is as shown in fig 12.

7. CONCLUSION

The design of LDO is being done in LTspice software for 180nm technology with supply voltage 1.8V. In this paper work the design is to achieve a low dropout voltage of 0.3V.The constant output of 1.5V is obtained for range of input voltage 1.5-2.2V for the load current of 10mA. The gain of the opamp for the LDO design obtained is 70db at load condition. The power consumed is 1.67mW for 5mA load and 3.35mW for 10mA current source load.

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