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HIGH SPEED ADDER WITH ULTRA LOW POWER CONSUMPTION USING XOR AND XNOR GATE

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Abstract - : *The recent trends in VLSI require low power and high performance Full adders. In this work, we designed different types of fast full adders based on XOR –XNOR circuits. With minimum of Power consumption, superior Speed and Power Delay Product (PDP). The full adders circuit have been employed with hybrid logic style, and are designed by XOR/XNOR or XOR-XNOR circuits. Here HFA-20T, HFA 17T, HFA-19T, HFA-B- 26T, HFA-NB-26T and HFA-22T are designed. The well-known four-transistor 2-1-mux structure is used to implement the hybrid full adder cells. Here designed various Hybrid adders and simulated the same and analysed its performance, Power Consumption, Delay and PDP. The designed adders by using XOR-XNOR and 2-1-MUX structures. Simulation Result based on 65-nm CMOS Process Technology Model, a new Transistor sizing method is presented to optimize the PDP of circuit.*

Key Words: Full Adder (FA), XOR-XNOR, PDP, Power, Delay

1. INTRODUCTION

TODAY, pervasive electronic frameworks are an indistinguishable some portion of regular day to day existence. Computerized circuits, e.g., microchips, advanced specialized gadgets and computerized signal processors, contain a huge piece of electronic frameworks. As the size of coordination expands, the ease of use of circuits is confined by the increasing measures of intensity and zone utilization. Along these lines, with the developing notoriety and interest for the battery-worked compact gadgets, for example, cell phones, tablets, and PCs, the architects attempt to diminish power utilization and zone of such frameworks while safeguarding their speed.

Enhancing the W/L proportion of transistors is one way to deal with decline the force postpone item (PDP) of the circuit while forestalling the issues came about because of decreasing the stock voltage [1]

2. Existing System

Half and Full adders are made of two modules, including 2-input XOR/XNOR (or concurrent XOR–XNOR) entryway and 2-to-1 multiplexer (2-1-MUX) gate[2]. The XOR/XNOR gate is the significant shopper of intensity in the FA cell. Along these lines, the force utilization of the FA cell can be diminished by ideal structuring of the XOR/XNOR gate. The XOR/XNOR gate has additionally numerous applications in computerized circuits plan. Numerous circuits have been proposed to actualize XOR/XNOR gate, which a couple of instances of the most productive ones are appeared in Fig-1(a) and (b). Fig-1(a) [3] Which shows the full-swing XOR/XNOR gate circuit planned by twofold pass-transistor rationale (DPL) style. This structure has eight transistors. The primary issue of this circuit is utilizing two high force utilization NOT entryways on the basic way of the circuit, in light of the fact that the NOT gate must drive the yield capacitance. In this manner, the size of the transistors in the NOT gate ought to be expanded to acquire lower basic way delay. Besides, it causes the making of a halfway hub with an enormous capacitance Clearly, this infers the NOT passages drives the yield of circuit through, for example, pass transistor or TG. Henceforth, Hence, the short out force and, along these lines, the complete force scattering of this circuit are generally expanded. Besides, in the ideal PDP circumstance, the basic way defer will likewise be expanded marginally.

Fig-1(b) shows another case of the full-swing XOR/XNOR gate, each made of six transistors. This circuit depends on the PTL rationale style, whose deferral and force utilization are superior to anything the circuit portrayed in Fig- 1(b). The main issue of this structure is utilizing a NOT gate on the basic way of the circuit. The XOR circuit of Figure 2 has the lower delay than its XNOR circuit, in light of the fact that the basic way of XOR circuit is included a NOT gate with an nMOS transistor (N3). In any case, the basic way of XNOR circuit is included a NOT doors and a pMOS transistor (P5) (pMOS transistor is more slow than nMOS transistor). Thusly, to improve the XNOR circuit speed, the size of pMOS transistor (P5) and NOT gate ought to be expanded.

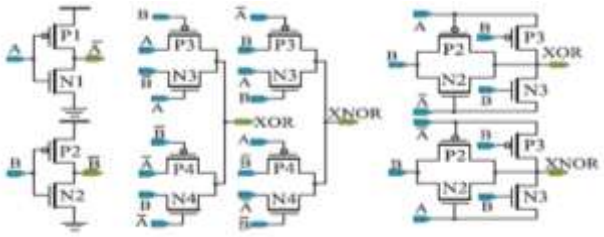

Fig- 1(a) and (b): Full –swing XOR/XNOR gate.

3. Proposed Framework:

3.1 XOR-XNOR Circuit.

The non full-swing XOR/XNOR circuit of Fig-2(a) [4] is proficient regarding the force and deferral. Moreover, this structure has a yield voltage drop issue for just one information intelligent worth. To take care of this issue and give an ideal structure to the XOR/XNOR gate, we propose the circuit appeared in Figure 2(b). For all conceivable information blends, the yield of this structure is full swing. The proposed framework have XOR/XNOR entryway doesn't have NOT gate on the basic way of the circuit. Hence, it will have the lower postponement and great driving capacity in examination with the structures of Fig- 1(a) and (b). In spite of the fact that the proposed XOR/XNOR gate has one more transistor than the structure of Fig- 1(b), it shows lower power dispersal and higher speed. The info An and B capacitances of the XOR circuit appeared in Fig- 2(b) are not symmetric, in light of the fact that one of these two ought to be associated with the contribution of NOT gate and another ought to be associated with the dissemination of n MOS transistor.

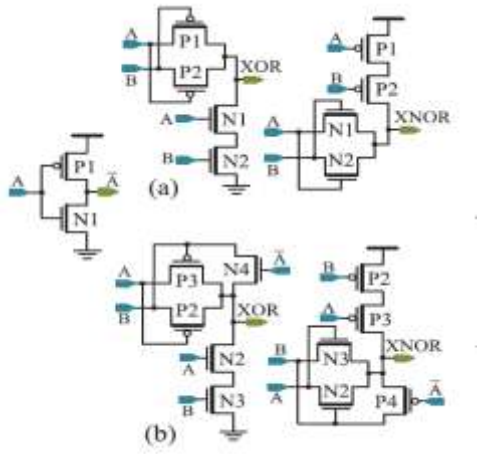

Fig-2:(a) Non full swing XOR/XNOR gate ,(b) Proposed Full swing XOR/XNOR gate.

Moreover, the info capacitances of transistors N2and N3 are not approach in the ideal circumstance (least PDP).Also, the request for input associations with transistors N2 and N3 won't influence the capacity of the circuit. In this way, it is smarter to interface the information A, which is additionally associated with the NOT gate, to the transistor with littler information capacitance. By doing this, the information capacitances are increasingly balanced, and therefore, the deferral and force utilization of the circuit will be diminished.

3.2 Proposed Full Adders

We proposed six new Full Adder circuits for different applications which have been appeared in Figure.3 Likewise, Figure.4 shows the circuit design of proposed FA cell appeared in Figure. 3(a). These new Full Adders have been utilized swith logic style, and every one of them is structured by utilizing the proposed XOR/XNOR or XOR–XNOR circuit.

Fig- 3(a) shows the circuit of first proposed half and half FA (HFA-20T) which is made by two 2-to-1 MUX gate and the XOR–XNOR gate. The circuit of HFA-20T has not high force utilization NOT gate on basic way and comprises of 20 transistors. The benefits of this structure are full-swing yield, low force scattering and extremely rapid, heartiness against supply voltage scaling, and transistor measuring. In the event that A ⊙ B = 1, at that point the yield Cout signal equivalents to the input signal A or B. In any case, to even out the information sources capacitance, both of the input signals A and B are utilized for execution and are associated with the transistors N9 and P10 [in Fig- 3(a)], separately. The main issue of HFA-20T is decrease of the yield driving capacity when it is utilized in the chain structure applications, for example, swell convey viper. Obviously, this issue exists in the circuits that utilization the transmission work hypothesis in their usage without buffering yield. Fig-4 shows the circuit format of proposed HFA-20T which intended for least force utilization [5].

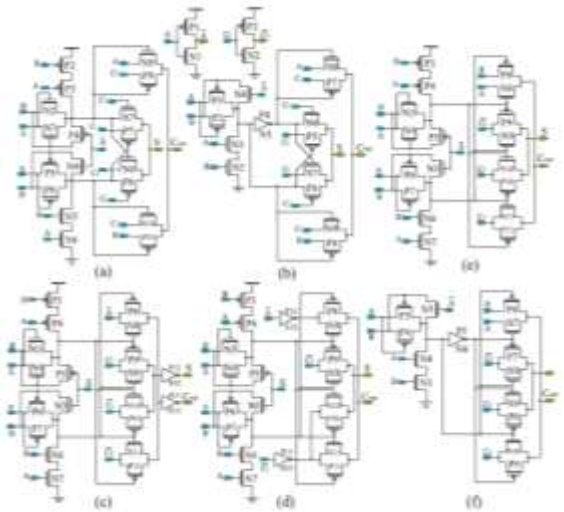

Fig- 3: Proposed Six new hybrid Full Adder circuits. (a)HFA-20T (b)HFA-17T (c)HFA-B-26T (d)HFA-NB-26T (e) HFA-22T (f)HFA-19T.

One approach to lessen the force utilization of the Full Adder structures is to utilize a XOR/XNOR entryway and a NOT gate to create the other XOR or XNOR signal. The proposed cross breed Full Adder cell (HFA-17T) appeared in Fig-3(b) is planned by utilizing the XOR gate of Fig-2(b). This structure is made by 17 transistors that has three transistors not exactly the HFA-20T. The deferral of HFA-17T is higher than that of HFA-20T because of the expansion of NOT gate on the basic way of the HFA-17T (for making The XNOR signal from the XOR signal). It might be normal that the force utilization of HFA-17T is not as much as that of HFA-20T because of the decrease in the quantity of transistors. Be that as it may the NOT gate on the basic way of the circuit expands the impede. So there is no huge decrease altogether power scattering of the HFA-17T. Additionally, the NOT gate will somewhat improve the yield driving capacity of the circuit.

As referenced before, utilizing the cushion on the yield of a circuit is practically obligatory, particularly in applications that the yield capacitance of each stage is high. By and by, the driving capacity of VLSI circuits is corrupted due to the formation of the parasitic capacitors and resistors during the creation, just as expanding the edge voltage of transistors over the time, yet the yield cushion improves this circumstance. Fig-3(c) presents the third proposed Full Adder with supports on the Sum and Cout yields (HFA-B-26T), furthermore, it is made with 26 transistors. There are XOR–XNOR gate, one 2-1-MUX gate, and NOT gate on the basic way of HFA-B-26T. The yield NOT gate are utilized to forestall the driving yield hubs by the contributions of the circuit and furthermore decrease the opposition from the yield hub of the circuit to the sources (VDD and GND). The force utilization and postponement of HFA-B-26T are more than that of HFA-20T and HFA-17T FAs. Fig- 3(d) shows another proposed Full Adder with new buffer (HFA-NB-26T), where they are set in the information contributions of 2-1-MUX gate as opposed to putting the supports in the yields. In the event that the info signs of An and C are delivered by the support, at that point for all conceivable information blends, the Sum and Cout yields are not driven by the contributions of the circuit. To do this work, three extra NOT gates are sufficient, in light of the fact that there was at that point the A flag and can be made the cushioned A signal with an extra NOT entryway. So the HFA-NB-26T Full Adder circuit is made up of 26 transistors. The information input hubs of 2-1-MUXs reach to their last worth (GND or VDD) before the XOR furthermore, XNOR signals are created. In this way, the basic way of HFA-NB-26T comprises of a XOR–XNOR gate and a 2-1-MUX gate, and its deferral is diminished contrasted and the HFA-B-26T.

The driving capacity of the HFA-NB-26T is somewhat not exactly that of HFA-B-26T because of existing the 2-1-MUX gate between the cradle and the yield hub [which builds the obstruction from the yield hub to the sources (VDD and GND)]. The circuits of HFA-20T and HFA-17T have been planned with the goal that the less number of transistors has been utilized.

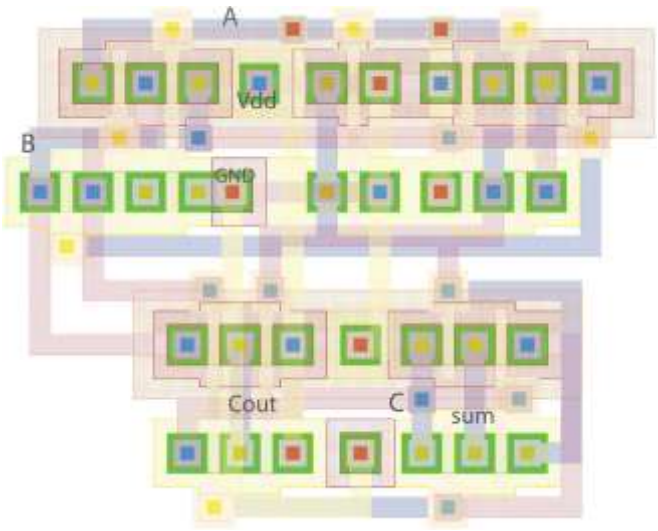

Fig-4: Circuit Layout of Proposed HFA-20T

To deliver the yield Sum signal, the XOR, XNOR, and C signals are as it were utilized so no extra NOT

gates needs to create the C signal, though if the C signal is likewise used to deliver the Sum yield, at that point XOR and XNOR signs won't drive the Sum yield through the TG multiplexer, yet just they will be associated to the information select lines of 2-1-MUX. So the capacitance of XOR .what's more, XNOR gate become littler, and the postponement of the circuit will be improved.

The circuits of Fig- 3(e) and (f) (named HFA-22T and HFA-19T, separately) have been made by applying the above plan to HFA-20T and HFA-17T, separately. It is normal that the force utilization and postponement of the HFA-22T and HFA-19T FA circuits are not as much as that of HFA-20T and HFA-17T, separately (in spite of having two more transistors), because of the less capacitance of XOR and XNOR gates. Additionally, by including the C signal, the driving ability of HFA-22T and HFA-19T will be superior to that of HFA-20T what's more, HFA-17T.

4. Simulation and Performance Analysis

Simulation results are talked about, and likewise the exhibition of the different referenced structures is thought about. In all reenactments, the size of transistors is picked so that the base PDP is accomplished for the circuit To show up now, the proposed procedure for transistor evaluating is used, the proposed technique for transistor estimating is utilized. we have detailed the normal power utilization, basic way postponement, PDP, and vitality delay item (EDP) measurements for various plans. Likewise, for better examination, the PDP and EDP enhancements of the structures contrasted and the 16T structure are given. The power conditions (MPCs), Cout and Sum yields regardless of having the nonfull-swing XOR–XNOR signals. The CPL Full Adder cell has the most power, due to having the high number of transistors, analyzed with different plans. In any case, it has great speed and great driving ability. In the MPC, the proposed HFA-22T recoveries the PDP of about 24%, 32%, 40%, 41%, 42%, and half contrasted and 16T, TFA, Mir-CMOS, TGA, New-HPSC, and DPL, separately.

4.1 Performance Analysis Against VDD

The delay, Power, and PDP of the Full Adder cells at supply voltage extend from 0.65 to 1.5 V .individually. The ostensible inventory voltage for the 65-nm TSMC CMOS process innovation is 1.2 V. additionally; the transistor sizes improved at 1.2 V are utilized for the recreation by any means supply voltage ranges. The reproduction results affirm that the proposed plans have predominant speed, force, and PDP than other Full Adder structures. The 14T, 16T, DPL, and New-HPSC FAs, because of the edge voltage drop issue, can as it were work at or more 0.95, 0.75, 0.7, and 0.7 V, separately. The delay of the 14T increments quicker with diminishing stock voltage than different FAs. For all stockpile voltage ranges from 0.65 to 1.5 V, the proposed HFA-22T has the least delay also, PDP contrasted and other FA circuits. The simulation results show that all Full Adder cells can work dependably at the stockpile voltage as low as 0.65 V. Regardless of having great speed, the CPL circuit expends extremely higher Power than different Full Adders in light of its double rail structure and the high transistor check New-HPSC, and 16T circuits have not appropriate execution against supply voltage varieties and are not suggested for use in the VLSI circuit. Hybrid Full Adder, HFA-20T, HFA-19T, HFA-22T, HFA-B-26T, and TGA has been accomplished at the stockpile voltage of 1.1 V.

4.2 Performance Analysis against Output Load

Full Adder cells against the yield load varieties running from FO4 to FO64. Fig-5(a)– (c) shows the reenactment results for the Power, Delay, and PDP of the FA circuits, individually, at FO4, FO8, mFO16, FO32, and FO64 yield loads. At the heap of FO64, the speed of the proposed HFA-B-26T FA is 39%, 41%, 15%, 14%, 10%, 5%, 25%, and 8% higher than the 16T, DPL, New-HPSC, M-CMOS, HFA-20T, HFA-22T, HFA-NB-26T, also, CPL, individually. The CPL and 16T expend the most elevated also, the least force, separately. The PDP of CPL FA at the heap of FO64 is equivalent to 20 fJ; be that as it may, to have better outline, the most extreme estimation of the PDP .The proposed HFA-22T cell has the least PDP. Other than the proposed HFA-B-26T has the most minimal PDP at the heap of FO64. Among the six proposed Full Adder cells, the HFA-NB-26T and HFA-22T have most minimal and most elevated normal PDP at different yield loads.

Figure 5(a)-

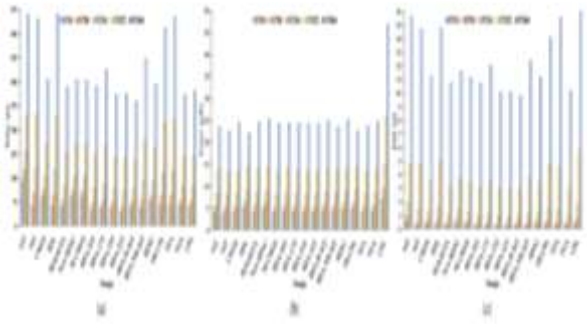

Fig 5: Simulation results of FAs versus load. (a) Delay. (b) Average power consumption. (c) PDP.

4.3 Feasible Environment

In applications where the FA cells are utilized for the fell arrange, yield driving capacity of the circuit is significant. To examine the exhibition of the FA circuits in a bigger structure (genuine and doable structure), all the thought about FA cells are implanted in a n-CFA with a word length of the n = 2, 4, 8, 16, 32, 64 bits. In the reenactment of n-CFA, no cradles have been utilized at middle of the road fell stages. A circuit may have a decent exhibition in the single mode be that as it may, when put in a bigger structure loses its focal points. Along these lines, to clarify the benefits and faults of the circuit, its exhibition must be investigated under various conditions.

4.4. PVT Variation

Simulation results for Full Adders against W, L, and Vth varieties of the transistors. These varieties have been applied to the circuit simultaneously, and the PDP of circuits has been separated. For better examination, the standardized PDP is determined. 14T, 16T, and New-HPSC FA cells are exceptionally touchy to the process varieties. For instance, the PDP of 14T is changed from −10% to +14%. The remainder of the FA circuits has lower affectability to the procedure varieties. The PDP of the FAs recreated in various procedure corners. Taking all things together corners, the proposed HFA-22T FA has the best execution contrasted and the remainder of the FAs.

5. Conclusion

The XOR/XNOR and XOR–XNOR circuits. The assessment uncovered that utilizing the NOT gate on the basic way of a circuit is a disadvantage. Another detriment of a circuit is to have a positive input on the yields of the XOR–XNOR entryway for repaying the yield voltage level. This input builds the deferral, yield capacitance, and, accordingly, vitality utilization of the circuit.

At that point, we proposed new XOR/XNOR and XOR–XNOR gates that try not to have the referenced burdens. At long last, by utilizing the proposed XOR and XOR–XNOR gates, we offered six new Full Adder cells for different applications. Too, a changed technique for transistor estimating in computerized circuits was proposed. The new strategy uses the numerical calculation PSO calculation to choose the proper size for transistors on a circuit and furthermore it has generally excellent speed, precision, what's more, union. Subsequent to reproducing the FA cells in various conditions, the outcomes exhibited that the proposed circuits have an excellent exhibition in totally reenacted conditions. Reenactment results show that the proposed HFA-22T cell spares PDP and EDP up to 23, 4% and 43.5%, individually, contrasted and its best partner. Likewise, this cell has better speed and vitality at all inventory voltages running from 0.65 to 1.5 V when is contrasted and other FA cells. The proposed HFA-22T has prevalent speed and vitality against other FA structures at all extraordinary procedure corners. All proposed Full Adders have typical affectability to PVT varieties.

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