

LOW POWER M-SEQUENCE CODE GENERATOR USING LFSR FOR BODY SENSOR NODE APPLICATIONS

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Abstract: Random numbers are required in the area of communication to provide security for information systems through pseudo random sequences. Designing a hardware device or software program to exploit this randomness and produce a bit sequence that is free of biases and correlation is difficult task. In this paper we present a linear feedback shift register (LFSR) which generates an arbitrary number based on XOR gates. This improves more randomness in runtime and also provides low power consumption.

Keywords: *Linear feedback shift register, XOR, m-sequence code.*

CHAPTER I

INTRODUCTION

Body sensor nodes (BSNs) are used in many area due to the development of wireless communication techniques. Recently, BSNs have been deployed in medical applications to improve and monitor human health as it can be placed in the human body. In medical sensor nodes, the transceiver design is faced with numerous challenges in terms of power dissipation, size restrictions and power supply. The use of large power supply (battery) will cause the node to be uncomfortable to wear, unlike the little battery, which obliges regular changing and decreases patient compliance. Thus, the need for an ultra-low power wireless transceivers becomes essential to overcome the limitations of conventional batteries and to be within the capabilities of existing harvesters. Spread spectrum is one of the common transmission techniques used in transceiver design to enhance the link quality by spreading the user's data to a wider bandwidth and to improve jamming resistance. Pseudo-noise (PN) codes have been used to spread the information signal by multiplying the PN code by the user data. However, the transceivers that deploy spread spectrum have a complex system structure and tend to consume large power. Thus, designing a low -power and complexity PN code generator can lead to enhanced efficiency. Moreover, the use of CMOS electronic circuits in such applications has boosted their performance and reduced their sizes and power consumption. Therefore, it is essential to analyze the power dissipation of CMOS implementations to investigate

the effect of variations of the supply voltage and switching frequency on power consumption. In this paper, we focus on the design and implementation of an m-sequence code generator circuit at a transistor level to operate at ultra-low power consumption that can be used in conjunction with a spread spectrum transceiver.

CHAPTER II

LINEAR FEEDBACK SHIFT REGISTER

A linear feedback shift register (LFSR) is shift register whose input bit is a linear function of its previous state. The only linear functions of single bits are xor and inverse-xor, thus it is a shift register whose input bit is driven by the exclusive or (xor) of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the sequence of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, a LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle. One of the two main parts of an LFSR is the shift register (the other is the feedback function). A shift register is a device whose identifying function is to shift its contents into adjacent positions within the register or, in the case of the position on the end, out of the register. The position on the other end is left empty unless some new content is shifted into the register. The feedback function in an LFSR has several names: XOR, odd parity, sum modulo 2. The bits contained in selected positions in the shift register are combined in some sort of function and the result is fed back into the register's input bit. By definition, the selected bit values are collected before the register is clocked and the result of the feedback function is inserted into the shift register during the shift, filling the position that is emptied as a result of the shift. The length of the sequence for a n-bit maximal LFSR is limited to 2^n-1 , whereas the length of the sequence for a n-bit binary counter is extended to 2^n . For example, If we want to divide an input clock by 16, a 4-bit binary counter would be sufficient, whereas a 4-bit LFSR would not be sufficient.

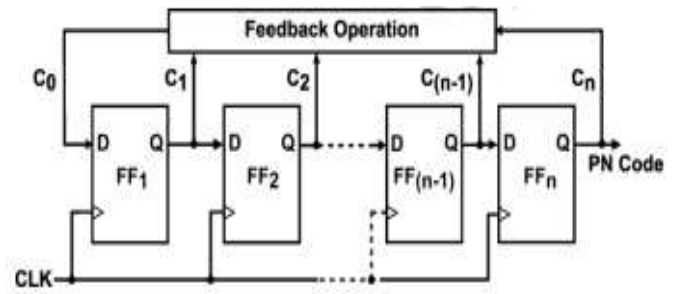
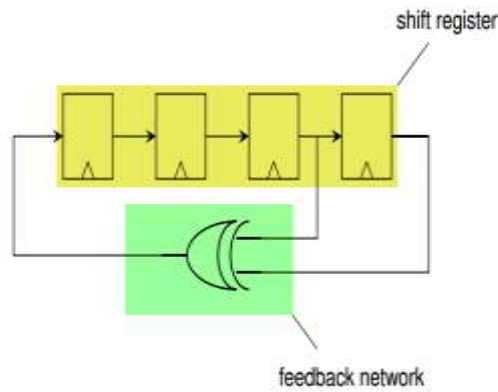


Figure 3.1 schematic of m-sequence code generator.

CHAPTER III

M-SEQUENCE CODE GENERATOR

The m-sequence codes are cyclic sequence which consists of binary numbers of 1's and 0's in a pseudo-random way. In practice, they are generated using flip-flop (FF) based LFSRs. Among the different FF types, the D-FF is used in this paper, where registers are connected linearly to form a shift register. The outputs of the FFs of the shift register are combined using an exclusive-OR (XOR) gate to provide feedback to input of the first FF, as shown in Fig. 3.1. Additionally, a clock distribution network is required that activates the FFs. The length of the resulting code depends on the number, N, of shift registers. A maximum code length of $L=2^N-1$ bits can be generated if the feedback connections are selected based on a primitive polynomial. There are two feedback shift register configurations for the m-sequence generator. For high-speed systems, XOR gates are placed between the FFs, while for low-speed systems, the XOR gates are in the feedback loop. The second architecture is the method of choice due its low power consumption. This selection does not affect the design as the m-sequence generator is placed before the modulator in the transmitter. Moreover, for small polynomials, this does not make a significant difference. The initial state of the LFSR, referred to as the seed, controls the code phase. All initial states are allowed, except the all zero state, as it leads to an all-zero bit sequence. Table shows feedback tap connections for different length sequences. scenarios, although performing exact computation requires large of resources, allowing bounded approximation can provide disproportionate gains in performance and energy, while still achieving acceptable result accuracy.

Number of stages N	Code length $L = 2^N - 1$	No. of possible codes	Feedback polynomials (octal form)
3	7	2	13
4	15	2	23,37
5	31	6	54,75
6	63	6	103,155
7	127	18	211,217
8	255	16	435,551
9	511	48	1021,1131
10	1023	60	2011,2415
11	2047	176	4005,4445
12	4095	144	10123

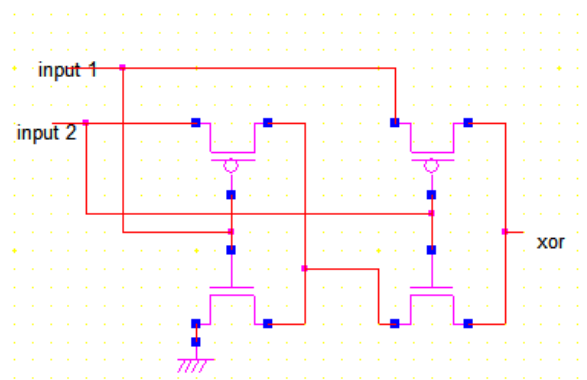
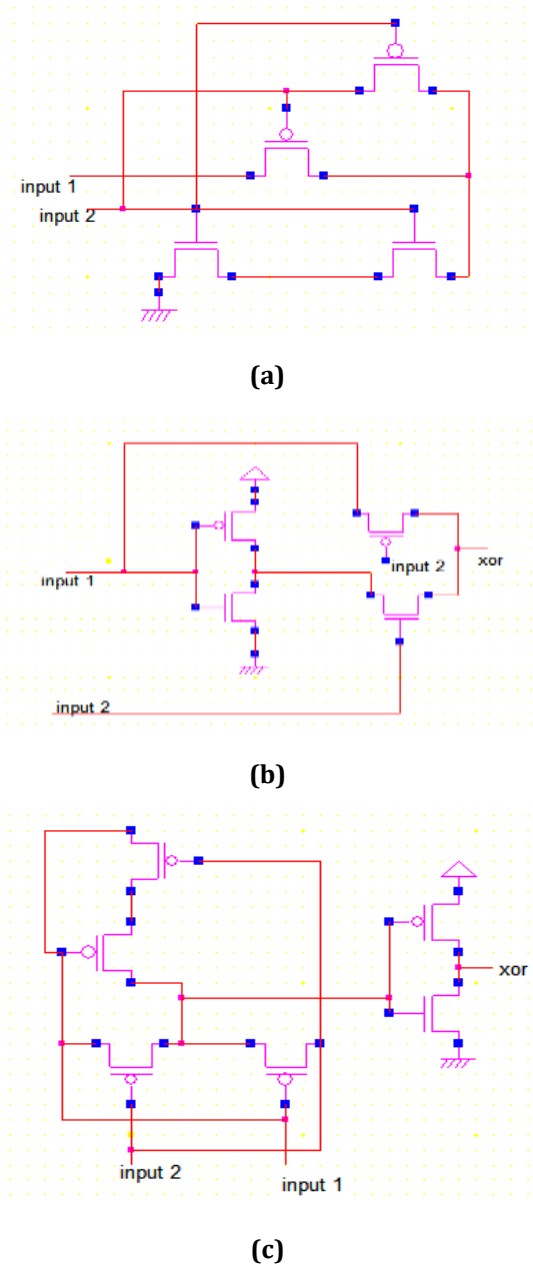
Table 3.1 some feedback taps of linear feedback shift register

CHAPTER IV

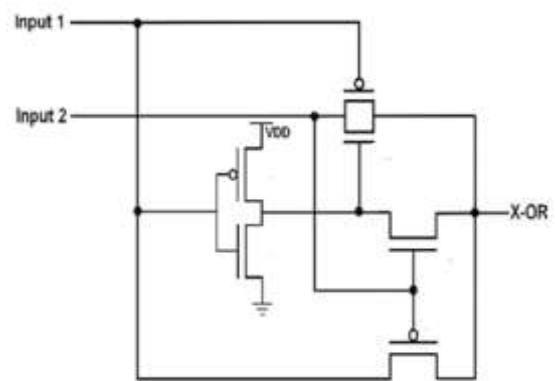
EXCLUSIVE -OR CMOS DESIGN

Two input XOR gates are required to perform the feedback operation of the m-sequence generator. In this paper, different designs of XOR circuits are compared and evaluated in terms of propagation delay and power consumption. In first one a pass transistor logic style is characterized by its low power consumption at low supply voltages, however, it produces a very poor output for some input combinations. A static inverter has been used in another design. Although the existence of a static inverter results in a good driving capability, the output waveform exhibits a poor logic 1 when the input pattern changes to 01 and a large delay when the input pattern is 00. A TG-based design is also shown that surpasses other designs in terms of low power consumption and good delay characteristics over all supply voltages, however, due to the use of an inverter, it requires larger circuit area. A design using 8 transistors is shown with a good output level at low voltages; however, the output deteriorates at higher voltages. In addition, it consumes more power than the other designs due to the availability of two static inverters. To overcome the problem of poor output level, a design of 6 transistors and good output level with driving capability is proposed, however, it is not efficient in terms of power and delay specifically at low voltages. Another design of 4 transistors based on pass style is presented, which is an efficient design in terms of power, nonetheless,

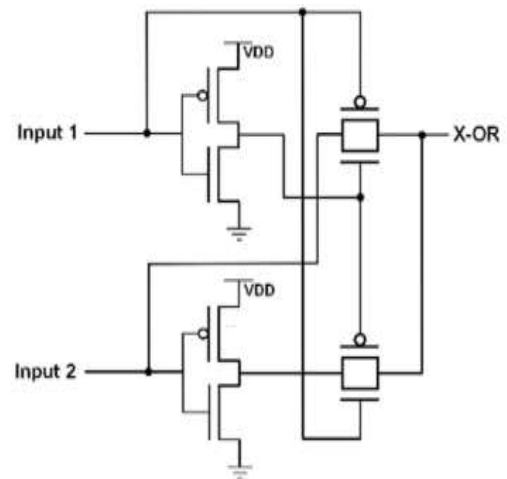
it suffers from the same problem of poor delay characteristics due to its limited driving capability. We can conclude that the TG-based design is consuming significantly less power than other designs for varying supply voltages. Our work as a feedback function for the m-sequence generator.



(d)



(e)



(f)

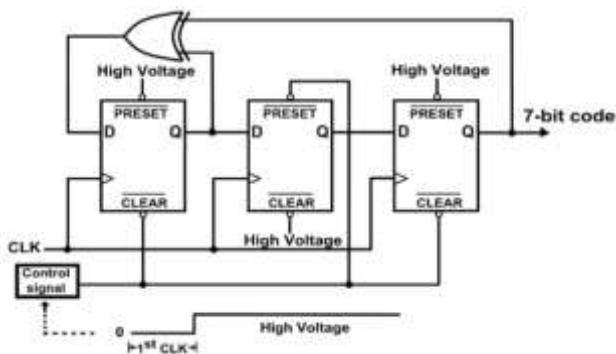
Figure 4.1 Different XOR designs

CHAPTER V

PROPOSED MODEL

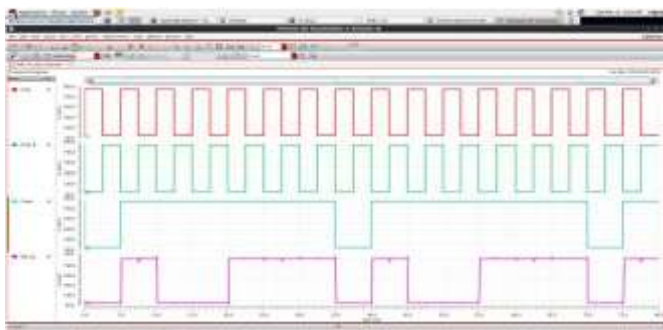
To generate a 7-bit m-sequence code, a 3-stages of LFSR are used as shown in Fig.3.6. According to the feedback polynomial described in (2), the activated feedback taps are c1 and c3. The phase of the generated code depends on the initial seed of the LFSR. The seed value can be

determined using PRESET and CLEAR, where both of them can be activated with low voltage. Control and high voltage signals are used to activate or deactivate the PRESET and CLEAR of each FF. The control signal is used to activate the PRESET and CLEAR, and to load the FF with a logic 1 or 0, respectively. The control signal consists of two states; the low voltage state is used for one clock period for activation purposes, while the high voltage state is utilized for deactivation. The control signal needs to be connected to CLEAR of the first and third FF, and to the PRESET of the second FF to generate the code 1001110. A modular design approach is used which requires the FF to have identical circuits. More importantly, when the code changes, the initial conditions of the FFs must be changed, and therefore, all the FFs need both PRESET and CLEAR terminals. This can be achieved by changing the connections to all the FFs from hard wire to a programmable structure. For analysis purposes, further code generators are required to determine the effect of the switching frequency and supply voltage on the power consumption of the circuit. Therefore, two more m-sequence generators of 31 and 511 bit-code lengths are implemented to assess the reliability of the codes produced as a function of the aforementioned constraints.



CHAPTER VI

SIMULATION



The simulated output of m-sequence code generator.

CHAPTER VII

CONCLUSION

So as to have low power consumption m-sequence code generator, in this paper a new XOR gate was proposed which is operated at different voltage levels. By using this method m sequence code generators that are used in many applications such as in body sensor networks can be designed with low power and high speed with less error tolerance. There are code generator designed in this proposed method, will have its own enhancement in the fields of area, power and speed. Using the section unit in the model conserves the time and is completely reduced. Thus, by using the above method VLSI designs major concerns which is the power utilization can be reduced significantly.

CHAPTER VIII

REFERENCES

[1] Q. Zhang, P. Feng, Z. Geng, X. Yan, N. Wu, A 2.4-GHz Energy-Efficient Transmitter for Wireless Medical Applications, IEEE Transactions on Biomedical Circuits and Systems, 5 (2011) 39 -47.

[2] S. Kim, R. Vyas, J. Bitto, K. Niotaki, A. Collado, A. Georgiadis, M.M. Tentzeris, Ambient RF Energy-Harvesting Technologies for Self-Sustainable Standalone Wireless Sensor Platforms, Proceedings of the IEEE, 102 (2014) 1649-1666.

[3] R.E. Ziemer, Fundamentals of Spread Spectrum Modulation, Synthesis Lectures on communications, 2 (2007) 1-79.

[4] H. Alrudainy, A. Mokhov, A. Yakovlev, A scalable physical model for Nano-Electro-Mechanical relays, in: Power and Timing Modeling, Optimization and Simulation (PATMOS), 2014 24th International Workshop on, 2014, pp. 1 -7.

[5] C. Chen, M. Sarrafzadeh, Simultaneous voltage scaling and gate sizing for low-power design, IEEE Transactions on Circuits and Systems II: Analog and digital signal processing, 49 (2002) 400-408.

[6] R. Vaddi, S. Dasgupta, R. Agarwal, Device and circuit co-design robustness studies in the subthreshold logic for ultralowpower applications for 32 nm CMOS, IEEE Transactions on Electron Devices, 57 (2010) 654 -664

[7] H. Ni, J. Hu, Near-threshold sequential circuits using Improved Clocked Adiabatic Logic in 45nm CMOS processes, in: 2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), IEEE, 2011, pp. 1-4.

[8] S. Henzler, Power management of digital circuits in deep sub-micron CMOS technologies, Springer Science & Business Media, 2006.

[9] S. Brueckner, K. Schubert, J. Fahlbusch, J. Schoebel, Generation of wideband m-sequences: A low-cost approach, in: 2014 IEEE International Conference on Ultra-WideBand (ICUWB), 2014.

[10] V.P. Ipatov, Spread spectrum and CDMA: principles and applications, John Wiley & Sons, 2005.

[11] T.F. Wong, Spread spectrum & CDMA, Multi-user Detection, (2001).

[12] M.-L. Wu, K.-A. Wen, C.-W. Haung, Efficient pseudonoise code design for spread spectrum wireless communication systems, IEEE Transactions on Circuits and systems II: Analog and Digital Signal Processing, 48 (2001) 606-613.

[13] A. Ba, M. Vidojkovic, K. Kanda, N.F. Kiyani, M. Lont, X. Huang, X. Wang, C. Zhou, Y.-H. Liu, M. Ding, A 0.33 nJ/bit IEEE802.15.6/proprietary mics/ism wireless transceiver with scalable data rate for medical implantable applications, IEEE journal of biomedical and health informatics, 19 (2015) 920 -929.

[14] H.W. Pflug, H.J. Visser, N.F. Kiyani, G. Dolmans, K. Philips, K. Kanda, M. Hamaminato, S. Masui, Radio channel characterization for 400 MHz implanted devices, in: Wireless Communications and Networking Conference (WCNC), 2014 IEEE, IEEE, 2014, pp. 293-298.

[15] A. Goldsmith, Wireless communications, Cambridge university press, 2005.