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AUGMENTED TANGIBLE STYLE USING 8051 MCU

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Abstract - *From the decades VLSI is performing a very vital role in the electronics area, with the aid of EDA tools, we plays inflation of the lap on 8051 microcontroller. For the most partake primitive 8051 microcontroller is negotiated at a clock frequency of 12 MHz, and the pattern is based on 3.5-µm process technology. Hence, the ploy is slow and the volume is giant. To reinforce the ploy performance and to lessen the die volume, we have used 90-nm technology in our style. We primarily played inflation when drafting the RTL codes with the 90 nm accepted cell libraries. Once the gate level net-list is generated, we progress the layout of the ploy by going through floor-planning, placement, and routing. We show that our innovation style which is able operating at frequency at 150 MHz (i.e., 12.5 times sooner than the primitive style), with a symbolic reduction in chip volume (i.e., the total area is77249.814850µm2). The power consumption of the chip is 593.9899 µw, which is no less than 32% lower than that of other8051 derivatives.*

Key Words*: *synthesis; floor*-planning*; placement; physical design, routing

1. INTRODUCTION

Despite being ,initiated by Intel more than three decades ago in 1980, the MCS-51 or better known as the 8051 microcontroller remains one of the most familiar frequent view microcontrollers in use until today. Numerous vendors have developed these microcontrollers and are still releasing updates for their reinforced binary sympathetic of8051 derivatives. This describes the continue recognition of the ploy. 8051 MCU has giant volume of applications such has huge volume of technical areas, including embedded systems, robotics, and telecommunications. The ploy, for example, only negotiates at 8-bit with a low clock frequency of 12MHz. Since the technology procedure of this ploy is 3.5 µm, it also has a big chip volume and can therefore only be fashioned in a dual-in-line package (DIP). The current applications of the primitive 8051 microcontroller are limited. It is mainly used as a guiding material in undergraduate engineering courses. To reinforce the performance of the primitive 8051 microcontroller, we complete inflation on VLSI circuit device. Here, we present amendment on the VLSI pattern of the 8051 microcontroller from its Register Transfer Language (RTL) code to its Graphic Database System II (GDSII) file. We precise by synthesizing the RTL codes based on an updated transistor technology and by re-pattern the layout of the chip, the performance of the device (i.e., its clock frequency) can be symbolic inflated and volume of the chip is minimized. By managing the power consumption when inflating the ploy, our innovation style postulates considerably lower power in contrast with its other derivatives

2. METHODOLOGY

Styling a complete chip from its organization specifications to its final layout is a strained procedure. At the front end, the style flow involves RTL style, style verification, logic synthesis, and static timing analysis (STA), whereas at the back end, it involves floor-planning, power network synthesis (PNS), clock tree synthesis (CTS), placement and routing, chip completing, and tangible corroboration. Although the flow may appear routine, some of these procedures are actually iterative, and therefore, they may have to be repeated multiple times. This is especially true when abuse– such as timing, style rule checks (DRC), layout versus schematic (LVS) violations are found during verifications. For our VLSI style, we applied Electronic pattern Automation (EDA) tools, i.e. pattern Compiler for synthesis and IC Compiler for tangible style here, we indicate in detail the essential procedures applied in our course reinforcement. The following are the steps followed in the style improvement

2.1 Synthesis 2.2 Floor planning
2.3 Placement and routing 2.4 Tangible-Corroborations

2.1 Synthesis

To reduce the style turn-around-time, by Intel 8051 equivalent RTL source code from Oregano organization will achieve. After compiling the RTL code and the level libraries and style checks, we synthesize the pattern with the 90-nm technology libraries. In the drafting process, we set the clock frequency to at 150 MHz and the die area to be minimum. Once the style synthesis all the analysis and meets all the style constraints, then

the gate stage net-list is been generated. The essential net-list is achieved in the tangible style level in order to expand the layout of the style.

2.2 Floor planning

In the tangible style, the libraries for floor planning are first set up. Later the core area and routing area are definite. The core utilization ratio is set to the proper value in order to provide margins for rout-ability. Once the floor plan is created, the basis cells are legally placed without any enrichment which is known as virtual flat placement. This is done in order to analyze the impact of the floor plan on timing and routing congestions as well as to map the power style. Routing congestions usually occur when a huge amount of wire nets are routed in a trivial area. The tool applies global routing methodology to check for routing congestions. In the global routing procedures, the tool divides the chip into global-route cells (GRCs). Each GRC consists of a restricted number of routing wire. The tool then calculates the ratio of the measure of routed nets to the number of accessible nets in each GRC. A ratio of more than one indicates that routing congestion exists in that specific cell which is in the form of grid. If the congestions are found to be unacceptable modification are performed on the top-level pads or ports, core aspect ratio and volume, as well as the power grid style.

The end status in floor mapping is power network synthesis (PNS). After the logical power and ground connections are dissimilar, and then the power rails along the standard cell placement rows are created. The current and resistance or IR drop plan is then used to study the power net work

2.3 Placement and Routing

The placement is ready when the pattern passes the PNS test, at this status; the EDA tool performs area, power, and timing inflations and also clock tree synthesis (CTS) on the style. Timing and congestion are later analyzed to check for breach. If breach is found, the path grouping approach is typically applied at the affected areas. After those paths are grouped based on the clocks, which control their endpoints, inflations and CTS are negotiated again. Once placement is finished, the tool negotiates global routing for the inaugural routing. This is followed by specific routing and inflation. DRC breach is commonly detected at this stage. Some of this breach could be fixed by running the Engineering Change Order (ECO) route. Very often, we may have to revert back to floor planning again to resolve the breach. Hence, these two procedures– floor planning and placement and routing would have to be executed in an iterative manner.

2.4 Tangible corroboration

LVS is negotiated at the final style stage to measure up the physical layout with the in flattered gate level net-list. This is to make sure that the logical descriptions of the style aren't altered during the tangible implementation procedures. Few final verification, such as CTS and final area analysis, are conducted before stream out the GDSII file. The GDSII file is essential for formulate the chip.

3. RESULTS AND DISCUSSION

Figure 1 view the inaugural floor plan created by the EDA tool. The tiny boxes in pink are the basis cells, while the green box in the left most of the figure indicates the terminals meant for the input and output (I/O) ports. The style consists of 5574 accepted cells. The similar utilization area is around 0.8. This means that 80% of the area is available for accepted cells, macros, and impasse placement. The remaining 20% of the area is reserved for routing. The gap between the terminals and the core area is about 10μm.

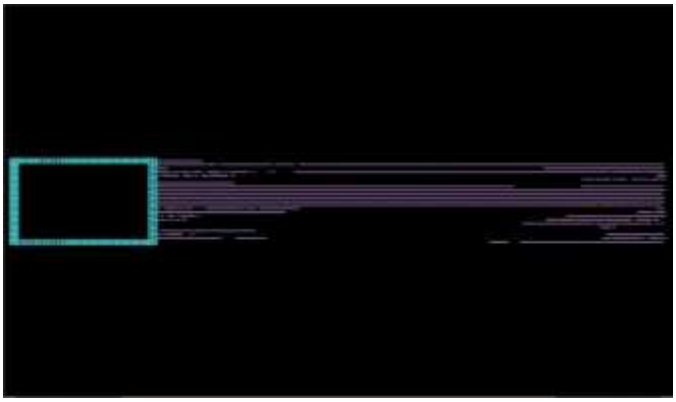

Fig -1: Floor plan of the proposed 8051 microcontroller

Figure 2 shows the virtual placement, which was created to check for routing congestions and timing breaches. As can be viewed from Figure 3, the virtual placement report indicates that the total number of cells violating the core area is 0.8. Thus breaches are detected and all cells can be placed into the core area,i.e.,80% of the total style area.

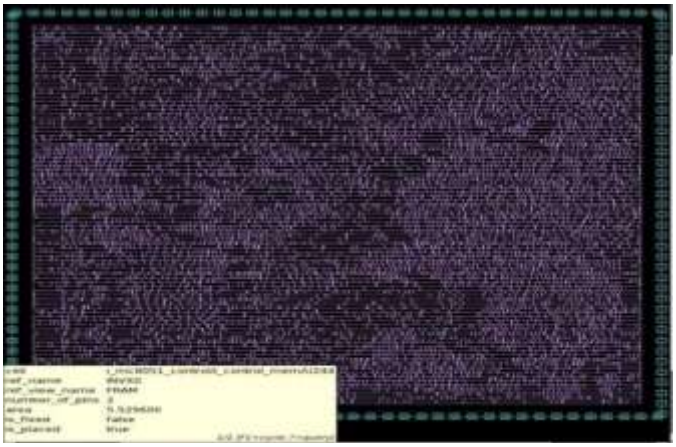

Fig -2: Virtual placement for the proposed 8051 microcontroller

```
Number of cells violating core area: 0
Total number of cells violating plan group or core area: 0
*** global placement done.
```

Fig -3: Virtual placement report

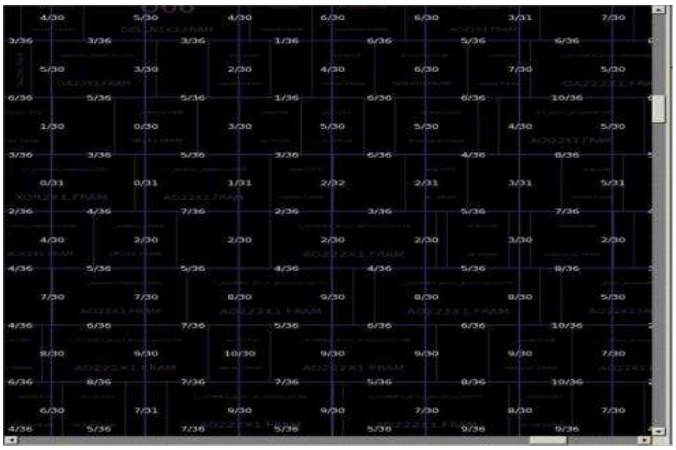

Fig -4: Congestion plan with GRC

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++++++++++++++++++++++++++++++++++++++++++++++++++
 Overall Congestion Map Data:
++++++++++++++++++++++++++++++++++++++++++++++++++
There are 10100 GRCs (Global Route Cell) in this design
**************************************************************
****************** GRC based congestion report ***************
**************************************************************
  0 GRCs with overflow: 0 with H overflow and 0 with V overflow
```

Fig -5: Congestion report

A portion of the congestion heat plan is shown in Figure 4. The congestion heat plan is used to visualize the cruelty of congestion in the global route cells (GRCs). As mentioned in the previous section, the EDA tool calculates the ratio of the measure for routed nets to the number of available nets in each GRC. As can be view from Figure 4, the ratios in the GRCs. The result suggests that there is no congestion in that specified portion. Figure 5 illustrates the conclusion of the congestion report. From the report, we can view that the total number of GRCs is 10100, and none of them experience overflows. In other words, there is no routing congestion in the style. From the report, we observe that the total number of GRCs is 10100, and none of them experience overflows. In other words, there is no routing congestion in the style.

Here the clock frequency is less when compared to before and after inflation. When compared to area it is decreased by 30%. The top hierarchical eyeshot of the final layout after routing and corroborations and a close view of the center of the layout are shown in Figures 6 and 7, respectively. The style is routed with nine metal layers. The bottom stage comprise of the accepted cells. The metal fillers and filler cells are inserted into the style to resolve the density breaches.

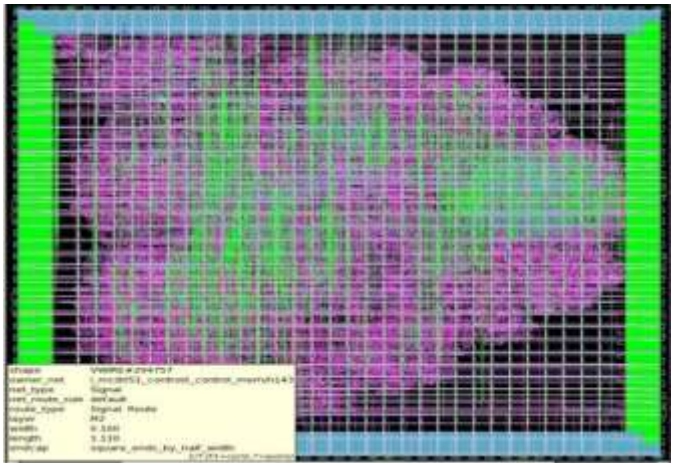

Fig -6: Final Layout

The total power consumption is 593.9899μW. As compared to the power consumptions of the 8051 derivatives reported, the inflatized 8051 microcontroller we styled. We consider requires at least 1.46 times less power to operate. In other words, power consumption has been reduced by at least 32%.After inflation propose at least 1.46 times power to negotiate. In other words, power consumption has been reduced by at least 32%. The feature volume of the transistors are implemented in our style is almost 40 times smaller than the proposed micro controller.

Table -1: Comparison Of Before and After Optimization of the Design

Parameters	Before Optimization	After Optimization
Clock Frequency	12MHZ	150 MHZ

Area	104984.540474 µm2(Based on 90nm_max	77249.81485µm2

The symbolic reduction in the suitable channel length authorize for an increase in the switching speed of the logic components and less power required to turn on the transistors. Furthermore, the Figure 7 describes the Centre of the layout, same number of transistors could be fashioned in a die with are smaller volume. By inflating the microcontroller using the 90-nm technology library, we show that our style can help which save much energy, apart from operating at a faster speed and having a smaller chip volume. It is interesting to find that the power consumption in our ploy using the 90-nm procedure technology is lower than in the ploy using the 45 nm process technology. We attribute this phenomenon to the careful planning played during floor planning and placement and routing. By carefully placing the cells and inflating the routing process, power consumption of the chip can be minimized.

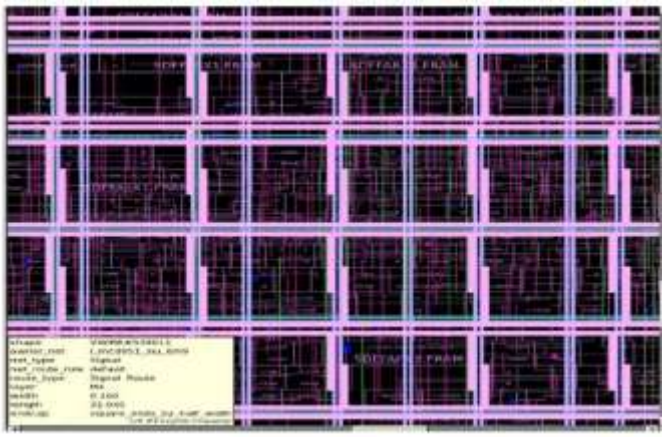

Fig-7: Center of the layout

4. CONCLUSIONS

In this paper, we have concluded that the style of the primitive 8051 microcontroller can be symbolically reinforced. By synthesizing the RTL code using libraries with the technology volume half of its primitive and by carefully styling its VLSI layout with the aid of Synopsys EDA tools, we were able to increase the clock frequency to 150 MHz and reduce the die volume to 77249.814850 µm2. The power consumption of our chip is 593.9899 µW, which is primitive to be at least 32% lesser than that of the 8051 derivatives.

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