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Design Optimization in Digital System Design

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Abstract – *In this paper, possibility of design and optimization of digital systems using EDA tools is presented. Design optimization deals with changing the design variables in order to obtain maximum benefits from minimum resources, which is actually a very idealistic and non-practical goal. Here we deal with two main things, optimization and digital design. Digital system design is basically setting up a device/circuit which can process a given digital input and give a digital output. Second part of the paper explains optimization, that includes three things to be optimized and they are: firstly, a device should be able to process the input at faster rate which provides the higher frequency required. Secondly, a device should consume very low area which helps to reduce the cost of the system. Thirdly, device should consume very low power.*

Key Words*: *Digital system design, Optimization, Area, Power, speed, design methodology, EDA tools, Logical optimization, Circuit miniaturization, etc.

INTRODUCTION

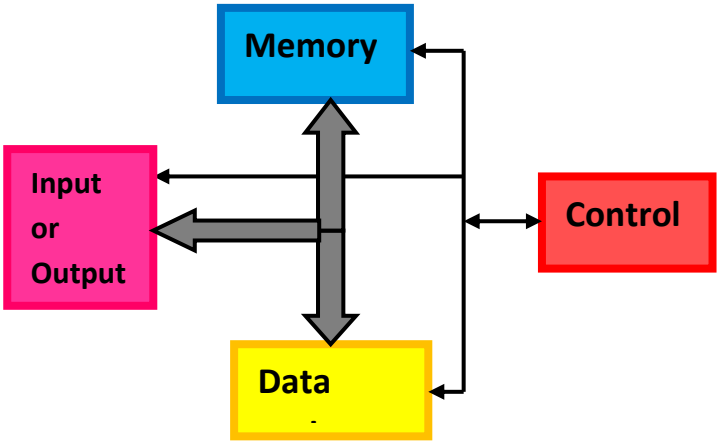
The extent of device integration on a single chip has shoot up vigorously since the semiconductor was originated. In reality, it has doubled about every two years for several decades. This development is customarily mentioned to as Moore's law entitled after Gorden Moore. Presently, it is feasible to integrate more than one billion transistors on a single die. There are predominantly two design obstacles that need to be reviewed as the level of integration increases. The first is related to reducing dimensions of on- chip components and the latter is relative increase in length of interconnection. As the components dimensions are decreased, physical strands which could formerly be dilapidated must now be appraised. The supplementary design challenge that becomes more tangled as component density increases is associated to design complexity. More efficient methods are mandatory as large number of transistors that can be integrated onto a single chip makes design very complex and it is challenging too.

The aspiration is that the finalized product should be as optimal as possible in terms of cost, performance and power consumption. The above mentioned purpose is gratified in this paper to optimize digital system design using CAD tools (algorithms).

What is DIGITAL SYSTEM?

A **digital system** is a system that stores data in a discrete way. Usually, digital systems store the information in a binary way; that is, every bit of information cannot have a value other than zero (off) or one (on). A typical Digital system has four basic functional elements: input-output equipment, main memory, control unit, and arithmetic-logic unit. Any of a number of devices is used to enter data and program instructions into a computer and to gain access to the results of the processing operation.

Examples of digital systems are mobile phones, radio, megaphones and many more.



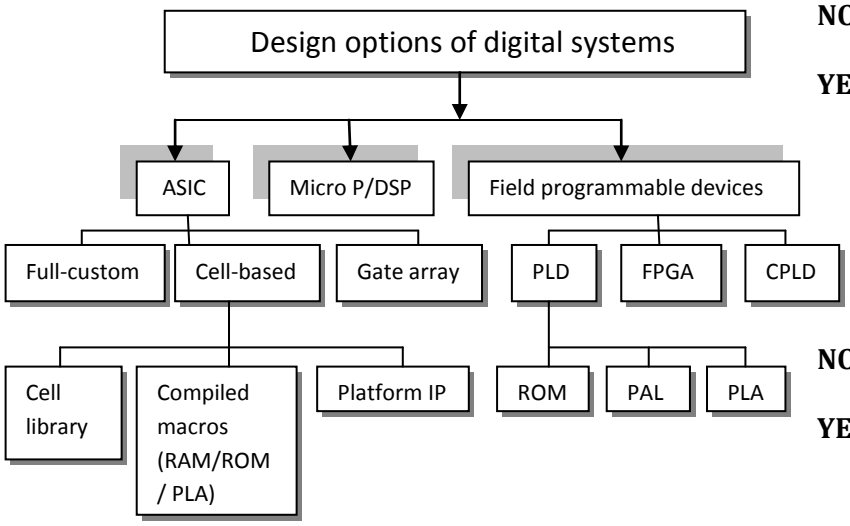
DIGITAL SYSTEM DESIGN

Digital System Design is the digital circuit design used in the Electronics industry especially in the **VLSI** field. It is the implementation of IC chips over several transistors. Digitization is now implemented in a wide range of applications, including information (computers), telecommunications, control systems, etc.

- Requires a systematic modular design methodology.
- Decompose system to define components to be designed.
- Defines information needed and produced.
- Defines relationships between components, dependencies and sequences.
- EDA tools.

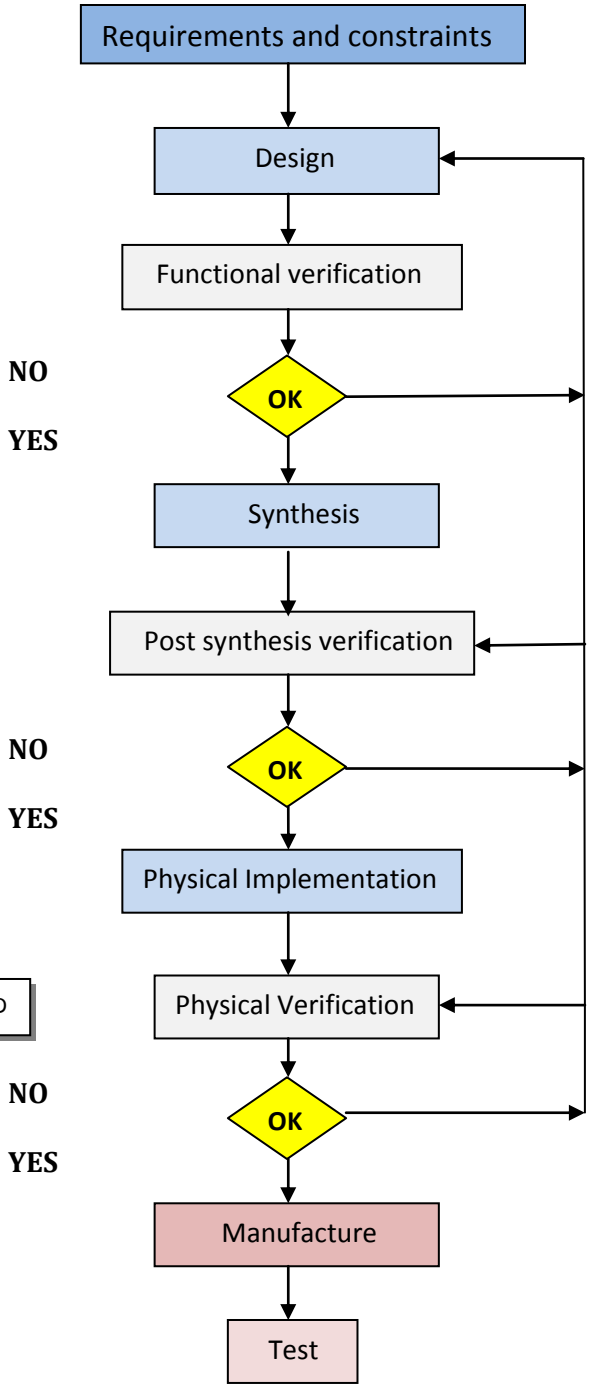
DESIGN PROCESS starts with a word problem, functional specifications and a block diagram.
Word problem: Design a circuit to select one of two inputs depending on the value of a control variable.
Functional specification: It is used to define inputs, outputs, control lines and also describes circuit functions.
Block diagram: It is pictorial and consists of major functional modules and interconnections.

THE VARIOUS DESIGN OPTIONS FOR DIGITAL SYSTEM



SIMPLE DESIGN METHODOLOGY

The first step in design methodology is collection of all requirements and constraints. Three principle works followed is: **Design, Synthesis** and **Physical implementation.** Each of this is followed by their respective verification processes. Once all the verification results come to be passed, the **manufacturing** of the product starts which is followed by **testing** the functioning of each and every component used in the product.



EDA TOOLS FOR DESIGN AND OPTIMIZATION

The term Electronic Design Automation (EDA) refers to the tools that are used to design and verify integrated circuits (ICs), printed circuit boards (PCBs), and electronic systems, in general. Over time, these early computer-aided drafting tools evolved into interactive programs that performed integrated circuit layout.

Other companies like Racal-Redac, SCI-Cards, and Telesis created equivalent layout programs for printed circuit boards. These integrated circuit and circuit board layout programs became known as Computer-Aided Design (CAD) tools. The companies promoting front-end tools for schematic capture and simulation classed them as Computer-Aided Engineering (CAE). The need for EDA software tools to design at higher levels of abstraction has clearly been recognized as the complexity of digital systems has continued to increase. System level EDA tools such as System Verilog and SystemC have been developed with cooperation by several companies to meet the need for system level EDA tools. It is also possible to design at the register transfer level (RTL) using the SystemC language and many systems have been designed using this approach. This approach has the advantage of making it easier to mix RTL descriptions of a part of a complex system with high level behavioral level descriptions of other parts of the system so that modeling and simulation can be done using a mixed level model.

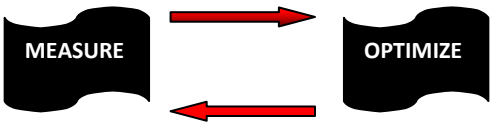
DESIGN OPTIMIZATION

Design optimization is an engineering design methodology using a mathematical formulation of a design problem to support selection of the optimal design. Design optimization involves the following stages:

~ Variables: Describe the design alternatives
~ Objective: Elected functional combination of variables (to be maximized or minimized)
~ Constraints: Combination of Variables expressed as equalities or inequalities that must be satisfied for any acceptable design alternative
~ Feasibility: Values for set of variables that satisfies all constraints and minimizes/maximizes Objective.

Optimization can provide either – a closed-form solution, or – a numerical solution.

• Numerical optimization systematically and efficiently adjusts the influencing variables to find the solution that has the best performance, satisfying given constraints.
• Frequently, the design objective, or cost function cannot be expressed in the form of simple algebra. Computer programs have to be used to carry out the evaluation on the design objective or costs.



Here, design optimization includes three things to be optimized and they are:
Firstly, a device should be able to **process** the **input** at **faster** rate which provides the higher frequency required.
Secondly, a device should consume very **low area** which helps to reduce the cost of the system.
Thirdly, device should consume **very low power** (LPC).

TIMING AND AREA OPTIMIZATION

The techniques for performance and area optimization of VLSI systems can be divided into two categories. One is to change the circuit structure by re-framing or re-timing the target system. The other is to change the transistor sizes of the circuit so that the driving and load conditions in the circuit are optimal. The latter approach does not involve any changes and is often referred to as "transistor sizing ".

Transistor sizing is to find a set of transistors of small sizes in a circuit so that the circuit performance and circuit area are optimized. The size of a transistor includes two components: the transistor channel length, L, and the channel width, W.

Since the transistor channel length is always fixed to its minimum value, optimization of area by varying transistor sizes can only be accomplished by varying the transistor widths.

Area optimization can also be done by **Logical optimization**.
Logical optimization: It is the process of finding an equivalent representation of the specified logic circuit under one or more specified constraints. Generally the circuit is constrained to minimum chip area meeting a pre-specified delay.

With the introduction of logic synthesis, one of the biggest challenges faced by the electronic design automation (EDA) industry was to find the best netlist representation of the given design description.

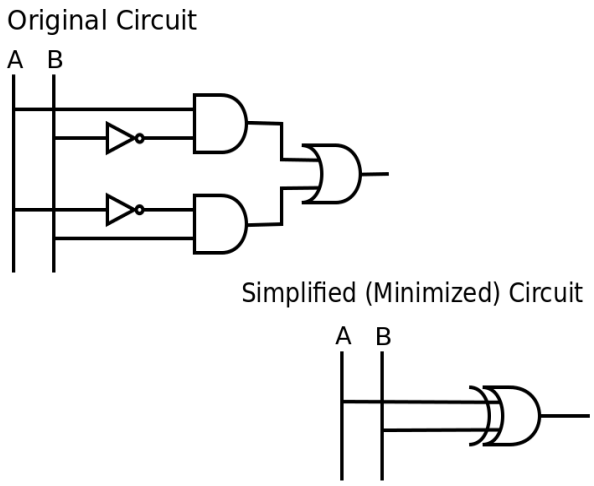
Today, logic optimization is divided into various categories:
Based on circuit representation
- Two-level logic optimization
- Multi-level logic optimization

Based on circuit characteristics
- Sequential logic optimization
- Combinational logic optimization

Based on type of execution

- Graphical optimization methods
- Tabular optimization methods
- Algebraic optimization methods

The problem with having a complicated circuit is that each element takes up physical space in its implementation and costs time and money to produce in itself. **Circuit minimization** may be one form of logic optimization used to reduce the area of complex logic in integrated circuits. While there are many ways to minimize a circuit, this is an example that minimizes a Boolean function. Consider the circuit used to represent some Boolean expression which includes two AND gates, one OR gate and two NOT gates, that can simplified by just using one XOR gate as shown in the below figure. This leads to less number of gates used in the circuit that results in area optimization (less space occupied) and **faster processing of input** i.e. speed is increased and consumes less time to deliver output which provides **higher frequency**.



Other optimizations which can be undertaken in order to increase system speed are:

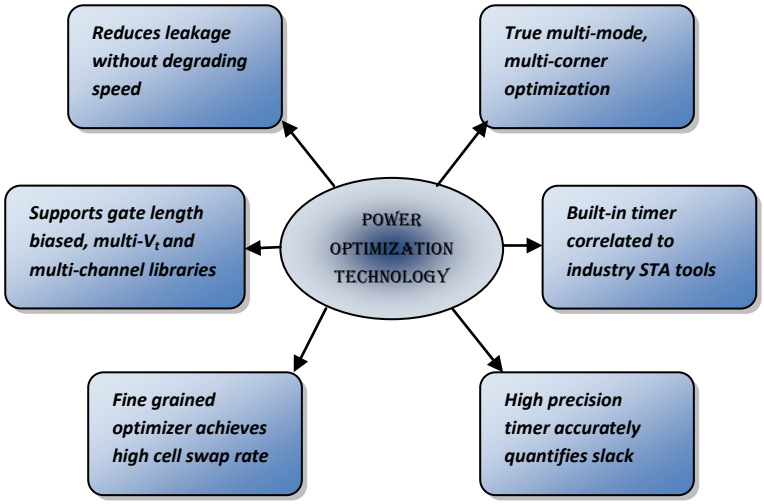
Throughput: amount of data that is processed per clock cycle expressed in Bits/second.

Latency: Time between data input and data output or just can be defined as a number of clock cycles.

POWER OPTIMIZATION

Electronic design automation tools are used to optimize the power consumption of a digital design system such as integrated circuit. There is a remarkable expansion in the power consumption of VLSI chips due to increase in speed and complexity of present design. Manual power optimization will be desperately slow and will have flaws for ICs with over 100 million transistors clocked at over 1GHz. Hence, computer aided design (CAD) tools and approaches are obligatory.

The large energy consumption of an IC at times became crystal clear due to increasing integration of more number of active elements per die area. The high level of power is unacceptable for economic and environmental cause. It also turns out the problem of heat dissipation due to which it may require expensive heat removal equipments.



Circuit level power optimization:

The different techniques used to truncate power consumption is

- *Transistor sizing*: The size of each gate or transistors is calibrated for minimum power.
- *Voltage scaling*: The inferior supply of voltage uses less power but go slower.
- *Voltage islands*: Different blocks run at different voltages which saves the power. When two blocks with different supply voltage liaise with each other, the design may need the use of level- shifter.
- *Multiple threshold voltage*: When combination of CMOS transistors with two or more different voltages are used, power can be saved. High V_t and low V_t are two threshold voltages. Use of high threshold transistors leak less but are slower.
- *Power gating*: It uses high threshold voltage sleep transistors which disconnect the circuit block when the block is not operating. The sleep transistor sizing is important design framework. This approach is known as MTCMOS (Multi threshold CMOS) decreasing leakage power.

- *Long channel transistors*: Transistors having more than minimum length leak less but are bigger and slower.

Logic synthesis for low power:

Following steps will have impressive influence on power optimization.

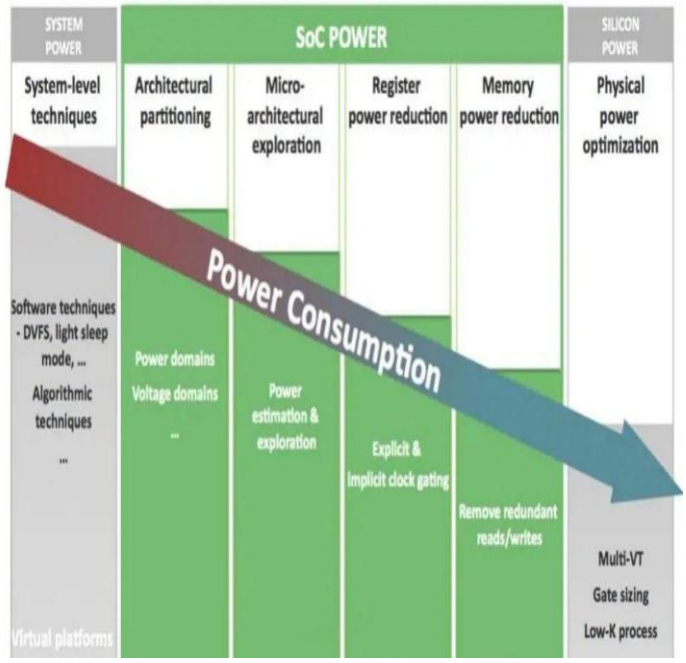
1. *Clock gating*: It is the technique where clock signals are withdrawn when the circuit is not in use in order to reduce dynamic power dissipation. Chips which intentionally work on batteries will implement several forms of clock gating. One is software makes the manual gating of clocks where a driver enables or disables the various clocks. Other is the hardware which detects and turns off a given clock if not in use called as automatic click gating. These forms communicate each other.

2. *Retiming*: Structural locations of a digital circuit is moved in order to improve the power characteristics. Simultaneously, the functional behaviour at the output is conserved.

3. *State encoding*: It is the method of assigning quirky pattern of ones and zeros to each defined state of finite state machine (FSM).

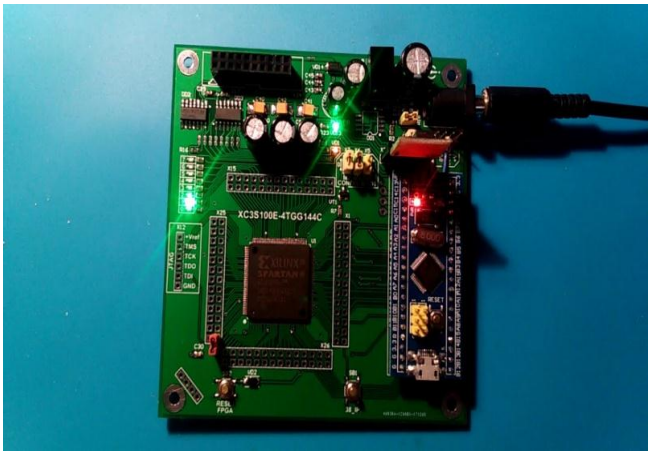
4. *Technology mapping*: Administering the sequential circuits using gates of particular technology library.

5. *Logic factorisation*: It is the form of introducing cost functions for sum of product and factored form representation of functions. These cost functions further guides the power optimization process.



FPGA PROGRAMMING

This project is implemented on FPGA Spartan 3 XC3S100E. Crystal oscillator generates the clock signal of 24MHz frequency, which is the clock source for FPGA. To define the behavior of the FPGA the user provides a hardware description language (HDL) or a schematic design. Common HDLs are VHDL and Verilog. Then, using an electronic design automation tool, a technology-mapped netlist is generated. The netlist can then be fitted to the actual FPGA architecture using a process called place-and-route, usually performed by the FPGA Company's proprietary place-and-route software. The user will validate the map, place and route results via timing analysis, simulation, and other verification methodologies. Once the design and validation process is complete, the binary file generated (also using the FPGA company's proprietary software) is used to reconfigure the FPGA device. To simplify the design of complex systems in FPGAs, there exist libraries of predefined complex functions and circuits that have been tested and optimized to speed up the design process. These predefined circuits are commonly called intellectual property blocks. In a typical design flow, an FPGA application developer will simulate the design at multiple stages throughout the design process.



Initially, the RTL description in VHDL or Verilog is simulated by creating test benches to stimulate the system and observe results. Then after the synthesis engine has mapped the design to a netlist, the netlist is translated to a gate-level description where simulation is repeated to confirm the synthesis proceeded without errors. Finally, the design is laid out in the FPGA at which point propagation delays can be added and the simulation run again with these values back-annotated onto the netlist.

ADVANTAGES OF DIGITAL SYSTEM

1. The effect of distortion, noise and interference is less.
2. It is more reliable.
3. Digital circuit are easy to design.
4. It is cheaper than analog circuit.
5. Easy to manipulate.
6. Less expensive.
7. Flexibility and compatibility.
8. Information storage can be easier in digital system.
9. Integrated networks.
10. It is also easier to transmit human audio and video signals into machine language.
11. There is a minimal electromagnetic interference in digital.
12. It enables multidirectional transmission.
13. It is more secure
14. Enables transmission of signals over a long distance.
15. Computer controller digital system can be controlled by software allowing new function to add without changing hardware.

DISADVANTAGES OF DIGITAL SYSTEM

1. Use more energy than analog to accomplish same task then it produces more heat.
2. In digital single piece of digital data is lost than related data can completely change.
3. Quantization error during analog signal sampling.
4. Digital communication requires greater bandwidth.
5. The detection of digital signal requires communication system to synchronise.
6. More expensive especially small quantities.
7. It can be reduced by designing a digital system for robustness, in this helps to detect and correct the error.

CONCLUSION

As the technology is going on developing day by day, we prefer things to be done automatically with less human interferences, so a cheap and effective way of getting things done can be implemented using this digital system which is advantageous in all the aspects due to support of optimization technologies which includes less power consumption, reduced area, higher speed, low latency, reduced delay, increased frequency and much more.

It has been tried sincerely how optimization problem can be formulated with EDA tools. Some more issues, such as a more system level and life cycle based approach to optimization are likely to be required for CAD tools to penetrate low end applications. In this we are using FPGA programming device with simple design methodology. Digital system designs used in VLSI technology are already on the verge of saturation in terms of frequency of operation and device size; hence industry has started focusing more on architecture based enhancements. There is always a room for improving digital solutions. Technology keeps changing, software and hardware keeps changing so are the trends of designing components.

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