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LEAKAGE POWER REDUCTION TECHNIQUES FOR NANOSCALE IN CMOS VLSI SYSTEMS USING MICROWIND EDA TOOL

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ABSTARCT-- *Low power design has become the major challenge for present designers. High power consumption leads to reduction in applications and affects reliability packaging and cooling cost. To increase the concert of device, three key factors are essential they are speed of the system, small area, low leakage power consumption. In CMOS submicron technologies Leakage power dissipation plays a significant role. In order to reduce this leakage power a comprehensive study is made for various techniques. By using LCPMOS technique the leakage power will be reduced. This paper focus the comparison among six different types of leakage power reduction techniques. Its functionality are implemented and verified using MICROWIND EDA tool. By using this tool we analysis the power dissipation, delay and efficiency of each techniques.*

keywords—CMOS, power consumption, leakage power, LCPMOS.

I. INTRODUCTION

The semiconductor evolution technology growth challenges to design low power micro electronic subsystems. While achieving the low power design, the area of the layout becomes overhead. The power consumed by the sub threshold currents and by reverse biased diodes in a CMOS transistor is considered as Leakage power. To maximize the battery life, the tremendous computational capacity of portable devices such as notebook computers, personal communication devices (mobile phones, pocket PCs, PDAs), hearing aids and implantable pacemakers has to be realized with very low power requirements. The power dissipation has become a very critical design metric due to device miniaturization and rapid growth towards wireless communication. The longer the battery lasts, the better is the device. The power dissipation has not diminished even with the scaling down of the supply voltage. The problem of heat removal and power dissipation is getting worse as the magnitude of power per unit area has kept growing.

II. POWER DISSIPATION

The two main components that constitute the power dissipation in a CMOS integrated circuit are static power and dynamic power.

Total Power dissipation=P_{static}+ $P_{dynamic}$

STATIC POWER DISSIPATION:

Static power is the power dissipated when the transistor is not in the switching mode and is generally determined by the formula,

Pstatic = I_{static} * Vdd

Where,

Vdd is the supply voltage,

I_{static} is the total current flowing through the device.

CMOS technology has been advantageous for its low static power. As devices battery life .In case of battery powered are scaled, gate oxide thicknesses is decreased and probability of tunnelling is increased, which results in very large leakage currents. This sub threshold leakage current is governed by thermodynamics, more specifically the Boltzmann distribution.

DYNAMIC POWER DISSIPATION:

Dynamic power is the sum of transient power consumption ($P_{transient}$) and capacitive load power (P_{cap}) consumption. $P_{transient}$ represents the amount of power consumed. when the device changes its logic states, 1 to 0 or 0 to 1. Putting these together we find that,

$P_{dynamic}=P_{cap}+P_{transient}=(C_L+C)(Vdd)^2 f N^3$.

Where,

C_L is the load capacitance,

C is the internal capacitance of the IC,

f is the frequency of operation,

N is the number of bits that are switching. This shows that as performance increases, due to increase of speed and frequency of the IC, the dynamic power also increases. Also we know that dynamic power is data dependent and is closely related to the number of transistors that change states. A more hidden component of dynamic power is the loss due to dynamic hazards.

III. LEAKAGE POWER

Two power components of a CMOS circuit are:

- Static Power
- Dynamic Power

Static power is the power consumed while the circuit is inactive or idle. all inputs are at held valid levels, there is no switching activity and and the circuit is not charging. However even in this steady state, there are some leakage currents in the device which contribute to the leakage power. This power dissipation doesn't depend on input conditions or load capacitance, but is dependent on the device.

There are many different contributing factors to leakage as mentioned below,

- PN-junction current
- Sub-threshold current
- Thin oxide gate tunneling
- Drain induced barrier lowering (DIBL)

IV. LEAKAGE POWER REDUCTION TECHNIQUES:

i. FORCED STACK TECHNIQUE:

The transistor stack is a leakage reduction technique which works both in active and stand-by mode. It is based on the observation that two off-state transistors connected in series cause significantly less leakage than a single device. However, in modern deep sub-micron devices the threshold voltage may decrease for longer channels due to the reverse short channel effect. Therefore, leakage reduction is less effective.

In this technique, every transistor in the network is duplicated with both the transistors bearing half the original transistor width. Duplicated transistors cause a slight reverse bias between the gate and source when both transistors are turnedoff. Because sub-threshold current is exponentially dependent on gate bias, it obtains substantial current reduction. It overcomes the limitation with sleep technique by retaining state but it takes more wakeup time

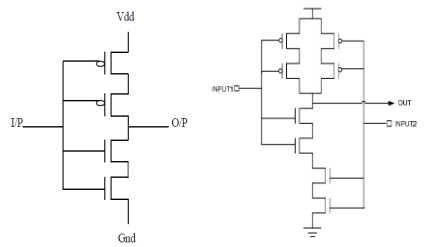


Figure 1.1 Forced Stack using NOT and NAND

ii. SLEEP TRANSISTOR TECHNIQUE:

One of the most commonly known traditional approaches for subthreshold leakage power reduction is the sleep approach. In the sleep approach, additional transistors (sleep transistors) are inserted in between the power supply and ground. An additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and an additional "sleep" NMOS transistor is placed between the pulldown network of the circuits and GND. During the standby mode these transistors are turned off and introduce large resistance in the conduction path so that leakage power is reduced in the circuit. By cutting off the power source, this technique can reduce leakage power effectively. [4]

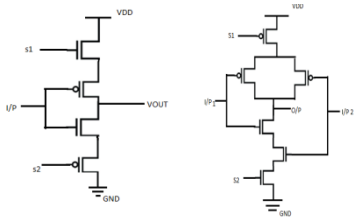


Figure 1.2 Sleep transistor using NOT and NAND

This is a State-destructive technique which cuts off either pull-up or pull-down or both the networks from supply voltage or ground or both using sleep transistors. This technique dramatically reduces leakage power during sleep mode. However, the area and delay are increased due to additional sleep transistors. During the sleep mode, the state will be lost as the pull-up and pull-down networks will have floating values.

iii. SLEEPY KEEPER TECHNIQUE:

Another leakage power reduction technique is the "sleepy keeper" approach. The structure of the sleepy keeper approach as well as its operation is described here. In sleep mode an additional single NMOS transistor placed in parallel to the pull-up sleep transistor connects VDD to the pull-up network [4].This NMOS transistor is the only source of VDD to the pull-up network since the sleep transistor is off. Then an additional single PMOS transistor placed in parallel to the pull-down sleep transistor is the only source of GND to the case pull-down network. For this approach to work, all that is needed is for the NMOS connected to VDD and the PMOS connected to GND to be able to maintain proper logic state.

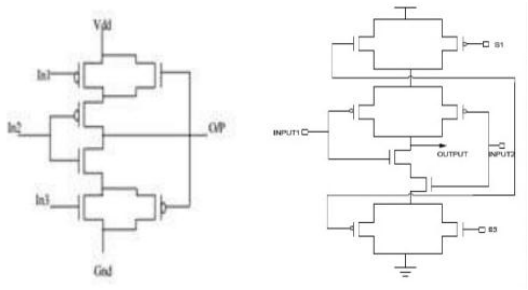


Figure 1.3 Sleepy keeper Using NOT and NAND

This technique consists of sleep transistors connected to the circuit with NMOS connected to Vdd and PMOS to Gnd. This creates virtual power and ground rails in the circuit, which affects the switching speed when the circuit is active .increasing the area requirement of the circuit. This additional circuit consumes power throughout the circuit operation to continuously monitor the circuit state and control the sleep transistors even though the circuit is in an idle state.

iv. LECTOR TECHNIQUE-(LEakage Control TransistOR Technique)

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation that "a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path". In this technique, two leakage control transistors are introduced between pull-up and pull-down network within the logic gate (one PMOS for pull-up and one NMOS for pull-down) for which the gate terminal of each leakage control transistor (LCT) is controlled by the source of the other. This arrangement ensures that one of the LCTs always operates in its near cut off region.

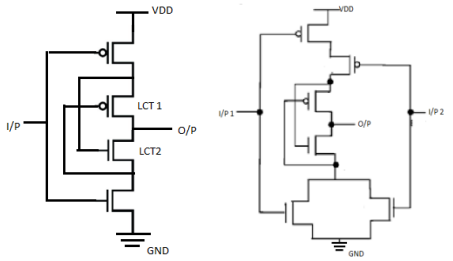


Figure 1.4 LECTOR method using NOT and NAND

This connection always keeps one of the two LCTs in its near cut off region for any input. The LECTOR technique works effectively in both active modes as well as in the standby mode.

v. MTCMOS TECHNIQUE:

Multi threshold voltage CMOS (MTCMOS) reduces the leakage by inserting high-threshold devices in series to low Vth circuitry. A sleep control scheme is introduced for efficient power management. In the active mode, SL is set low and sleep control high Vth transistors (MP and MN) are turned on. Since their on- resistances are small, the virtual supply voltages almost function as real power lines. In the standby mode, SL is set high, MN and MP are turned off, and the leakage current is low. In fact, only one type of high transistor is enough for leakage control .A high-threshold NMOS gating transistor is connected between the pull-down network and the ground, and low-threshold voltage transistors are used in the gate. In MTCMOS the gates in the critical path use low-threshold transistors and high-threshold transistors for gates in non- critical path.

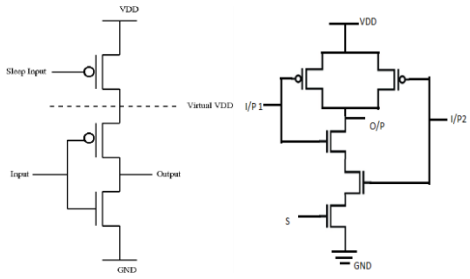


Figure 1.5 MTCMOS method using NOT and NAND

The techniques also suffer from turning-on latency i.e., the idle circuit cannot be used immediately after reactivated since sometime is needed to return to normal operating condition. When the circuit is active, these techniques are not effective in controlling the leakage power.

vi. Leakage Control PMOS(LCPMOS) Technique:

In this proposed technique, a single leakage control transistor is introduced within the logic gate for which the gate terminal of leakage control transistor (LCT) is controlled by the output of the circuit itself. Which increases the resistance of the path from pull down network to ground thereby increasing the resistance from Vdd to ground, leading to significant decrease in leakage currents. The main advantage as compared to other techniques is that LCPMOS technique does not require any additional control and monitoring circuitry, thereby limits the area and also the power dissipation in active state. One LCTs are introduced between nodes N1 and Gnd. The gate terminal of LCT is controlled by the output of the circuit itself. As LCT is controlled by output, no external circuit is needed. Thereby the limitation with the other techniques has been overcome. The introduction of LCT increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.

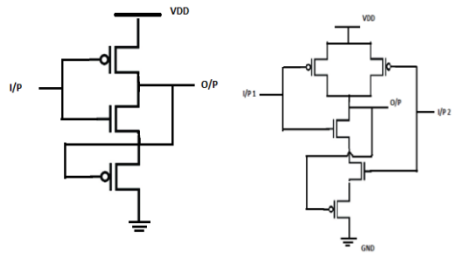


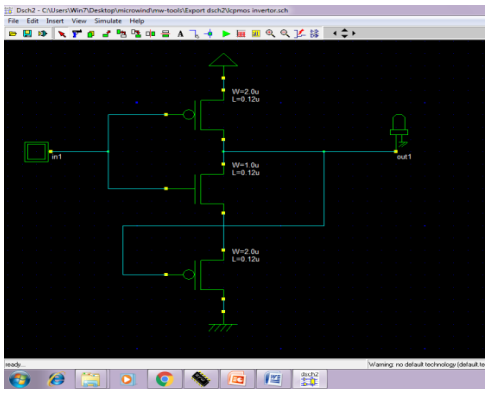
Figure 1.6 LCPMOS using NOT and NAND

TECHNIQUES	NOT	NAND
FORCED STACK	4	8
SLEEP TRANSISTOR	4	6
SLEEPY KEEPER	6	8
LECTOR	4	6
MTCMOS	3	5
LCPMOS	3	5

TABLE 1 No. of MOS transistors uses in the techiques

V. SIMULATION AND RESULTS

The LCPMOS technique is a efficient technique compared with the other leakage reduction techniques, thus this technique is implemented in dsch2 software and its power dissipation, delay and power efficiency are calculated in microwind2 tool.



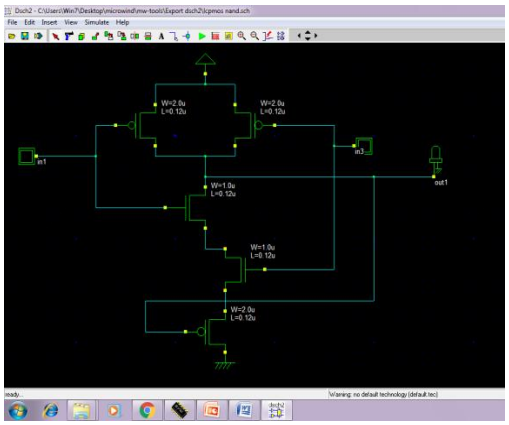
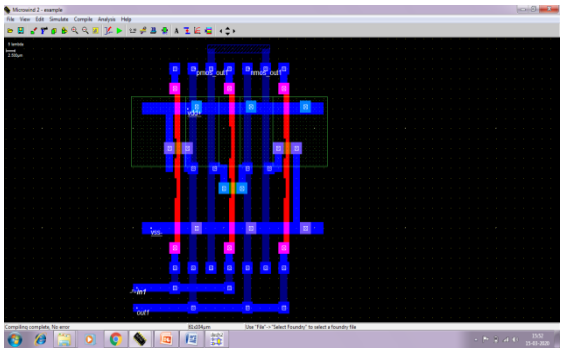


Figure 7 Implementation of LCPMOS NOT and NAND using dsch2 tool

The LCPMOS NOT and NAND circuits are implemented in DSCH2 software and then make its verilog files to compile in MICROWIND2 tool.



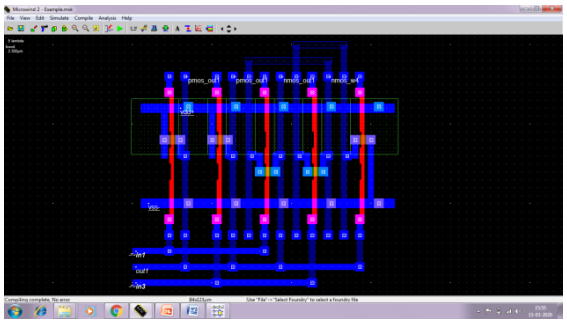


Figure 8 Layout diagram for LCPMOS NOT and NAND using microwind tool

The LCPMOS circuits are compiled in the microwind2 software using its verilog files, then the output waveform is found in simulating the layout diagram.

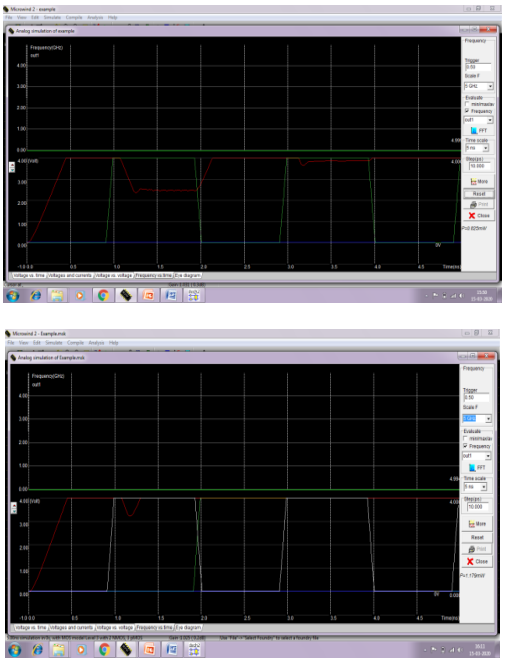


Figure 10 output waveform for LCPMOS NOT AND NAND circuit

TABLE 2 Comparison of power dissipation, delay and power efficiency in NOT

TECHNIQUE	POWER DISSIPATION (mW)	DELAY (ns)	EFFIECNCY %	AREA (um^2)
FOCRED STACK	0.625	0.621	62.1	34.4
SLEEP TRANSISTOR	0.250	0.225	22.0	33.9
SLEEPY KEEPER	0.3	0.340	33.8	38.6
LECTOR	0.209	0.212	21.4	27.4
MTCMOS	0.326	0.355	36.1	21.7
LCPMOS	0.344	0.355	35.2	21.7

TABLE 3 Comparison of power dissipation, delay and power efficiency in NAND

TECHNIQUE	POWER DISSIPATION (mW)	DELAY (ns)	EFFIECNCY %	AREA (um^2)
FOCRED STACK	0.313	0.325	31.5	17.3
SLEEP TRANSISTOR	0.117	0.112	11.2	21.7
SLEEPY KEEPER	0.121	0.120	11.7	36
LECTOR	0.110	0.112	11.3	26.3
MTCMOS	0.114	0.116	11.7	12.9
LCPMOS	0.2345	0.237	23.5	12.9

VI. CONCLUSION

The increase in leakage power because of the device dimensions, supply and threshold voltages to achieve high performance and low dynamic power dissipation, it becomes a great challenge to tackle the problem of leakage power. LCPMOS uses one LCT which is controlled by the output of circuit itself. LCPMOS achieves the reduction in leakage power compared to other leakage reduction techniques, such as Forced stacking, sleepy stack, sleepy keeper, lector, MTCMOS etc, along with the advantage of not affecting the dynamic power, and use of limited area requirement since this technique does not require any additional control and monitor circuitry and also in this technique. The LCPMOS technique when applied to generic logic circuits achieves leakage reduction over the respective conventional circuits without affecting the dynamic power. A tradeoff between Propagation delay and area overhead exists here.

VII. REFERENCES

[1] "A Survey on leakage Reduction on logic Gate in Deep submicron Technology",Md Tauseef,Sudeep Sharma,Rita Jain.2016 International journal of Engineering Trends and Technology (IJETT)

[2] "Leakage Power Reduction in CMOS VLSI" Subrat Mahalik,M.Bhanu Teja. 2014 International journal of Engineering Research and Technology (IJERT).

[3] "comparison of various leakage power reduction technique for CMOS circuit Design" hina malviya , prof. Murli manohar hinnwar 2013 International journal of engineering research & technology (IJERT)

[4] "Leakage power reduction by using Sleep methods",Vinay Kumar Madasu, B.Kedharnath. 2013 International journal of engineering and computer science.

[5] "Sleepy Stack – A new approach of low power VLSI logic and memory" J.C park 2005 Ph.d dissertation, school of Electrical and computer engineering, georgia institute of technology.

[6] H Narender and R Nagarajan "LECTOR A technique for leakage reduction in CMOS circuits" IEEE trans on VLSI systems , vol no 12, feb 2004.